Impact of Measurement Setup on Cryogenic CMOS FET Characterization

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***Abstract*— Accurate cryogenic device characterization is essential for developing compact models needed to realize scalable quantum control electronics. However, we observe abnormal current-voltage (I-V) characteristics in 16 nm and 28 nm FETs at cryogenic temperatures. It is shown that these abnormalities arise not only from intrinsic device behavior, but also from self-sustained oscillations induced by parasitic LC feedback present in nearly all standard measurements. These abnormalities are exacerbated at low temperatures (due to the increased device gain) and are especially prominent for low loss and high inductance configurations. SPICE simulations incorporating realistic parasitics, combined with high-resolution time-domain measurements, confirm the presence of these oscillations and their impact on the more commonly reported time-averaged I-V characteristics. We demonstrate that using ground-signal-ground (GSG) RF wafer probes effectively suppresses these artifacts by minimizing loop inductance, restoring true device behavior. These results highlight the need for careful test structure and measurement setup design to ensure reliable cryogenic CMOS characterization.**

***Index Terms*— Cryogenic CMOS, measurement induced artifacts, device characterization.**

I. Introduction

As CMOS technology is co-opted by emerging research domains such as cryogenic electronics to support quantum information science, the demand for accurate cryogenic CMOS FET models has intensified [1], [2], [3]. Cryogenic operation of commercial CMOS nodes, including 28 nm planar CMOS and 16 nm FinFET technologies, is particularly attractive for implementing scalable cryogenic control electronics integrated with quantum systems [4], [5]. Generating accurate models for cryogenic circuit design depends critically on precise FET characterization. However, standard cryogenic characterization of these devices assumes that DC (quasi-static) measurements are immune to high-frequency effects. We show this assumption fails in advanced nodes, where further-enhanced transconductances g_m at low temperatures [6] can trigger high-frequency instabilities, leading to unintended measurement artifacts.

We demonstrate that abnormal cryogenic current versus voltage (I-V) curves can stem from unintentional self-sustained oscillations due to the interaction between FETs and reactive parasitics in the measurement setup (distinct from the kink effect [7], [8], threshold bi-stability [9], or bimodal transconductance [10]). These measurement artifacts can appear even at room temperature in high-g_m FETs. We validate this behavior via SPICE simulation and high-resolution time-domain I-V measurements. Furthermore, we demonstrate that adopting ground-signal-ground (GSG) probes effectively suppresses the parasitic loop inductance in the setup, eliminating oscillations and enabling accurate DC I-V characterization.

These findings are directly relevant to the adoption of cryogenic electronics, where precise high-g_m device models are essential for reliable high-performance circuit design. Any inaccuracy in I-V measurements can lead to incorrect model extraction, resulting in critical circuit failures, overly conservative performance margins, or lengthy design iterations [11], [12]. Our results underscore the importance of metrology-aware test structures and measurement setups in cryogenic CMOS characterization, particularly as the field progresses toward integrated, high-fidelity control and readout electronics for scalable quantum computing.

II. Observation of I-V Distortions

Typical DC I_D-V_G measurements at cryogenic temperatures for 16 nm FinFET and 28 nm CMOS devices across various channel widths are shown in Figs. 1a and 1b. While narrower FETs exhibit the expected behavior, wider FETs display distinct distortions. Such abnormalities at low temperatures are not uncommon and have even been noted by other groups [13], though often attributed broadly to low-temperature effects without detailed analysis.

We observe similar anomalies even at 300 K in high-g_m FinFETs across two configurations: a cryogenic and a standard room-temperature probe station (Figs. 1c and 1d). The emergence of a pronounced 'bump' near threshold voltage depends on both FET dimensions and the specific setup. For instance, in the room-temperature setup, this feature appears only in FETs with widths of 16 μm or greater. In all cases, measured characteristics deviate remarkably from the smooth behavior predicted by DC simulations using validated 16 nm PDKs that exclude external parasitics. We will show that these

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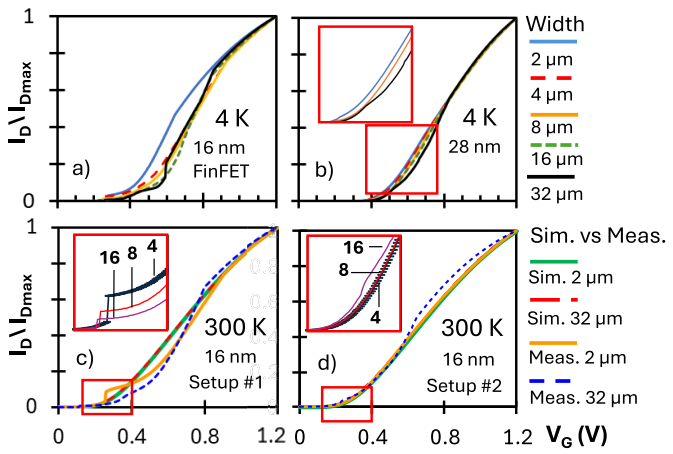

Fig. 1. Normalized $I_D/I_{D,\,max}$ vs. V_G characteristics for FETs with widths of 2 μm, 4 μm, 8 μm, 16 μm, and 32 μm at **4 K** for (a) 16 nm FinFET and (b) 28 nm planar technologies, with 16 nm and 28 nm length, and at **300 K** for 16 nm FinFET in (c) cryogenic probe station (Setup #1) and (d) room-temperature probe station (Setup #2), respectively.

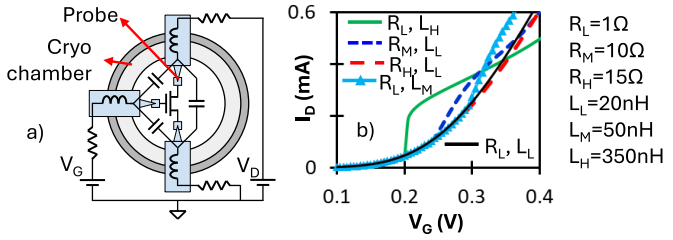

Fig. 2. (a) Diagram showing probe and cryo chamber along with parasitic inductance (L), capacitance (C) and resistance (R) present in the measurement system taken into account to simulate FET operation and (b) I_D-V_G characteristics from simulation for three different L values at fixed R_L = 1 Ω for each probe arm and for varying R at fixed L_H.

results confirm that the distortions stem from the interaction between high FET g_m and measurement setup parasitics, rather than intrinsic FET behavior.

III. Simulation and Fast Measurement of Distortions

To replicate the observed DC abnormalities, validated FET models were expanded to include the estimated inductance and resistance in the probes and cables of the probe station. The subsequent 300 K steady state simulation, with harmonic balance [14], is illustrated in the circuit diagram in Fig. 2a. The simulated I_D-V_G characteristics of a 4 μm x 16 nm nFET for three different inductance values at fixed resistance R_L and for varying resistance at fixed inductance L_H are shown in Fig. 2b. The results clearly indicate that increasing the inductance introduces abnormalities, while reducing the resistance exacerbates the effect. The lowest resistance and the highest inductance result in the maximum distortion.

Given the strong dependence on inductive parasitics, a time-domain analysis is conducted to gain further insight. In these simulations, we examine the I_D-V_G characteristics of a 4 μm x 16 nm nFET in which the gate voltage is swept from 0-1.2 V in 10 ms while V_D is held at 700 mV. The transient simulations reveal pronounced oscillations in I_D particularly at the bias point where FET transconductance

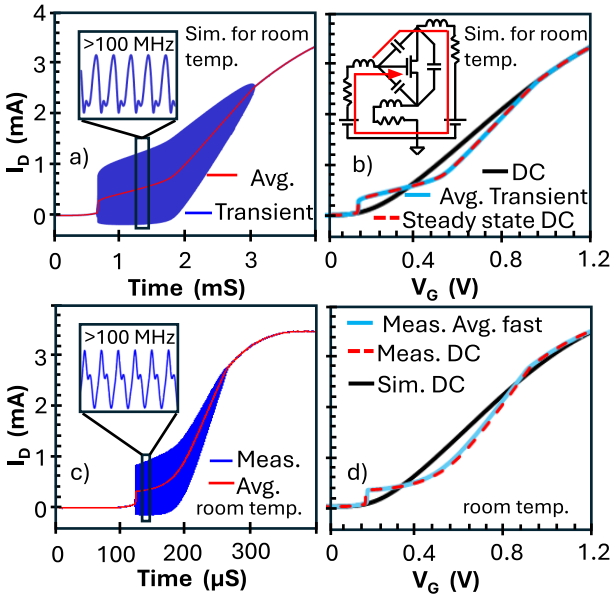

Fig. 3. (a) Transient simulation showing > 100 MHz oscillations with the moving average revealing the resulting bump; (b) comparison of sim. DC response (no oscillations), steady-state DC, and the moving average of the oscillating current, with the inset illustrating the Hartley-type oscillator formed by parasitic impedances; (c) time-domain measurements capturing oscillations; and (d) comparison of the measured moving-average current from (c), the meas. DC current for the same setup, and the sim. DC response without oscillations.

g_m is highest (Fig. 3a). The inset of Fig. 3a provides a zoomed-in view of the I_D waveform, revealing oscillations with a frequency of approximately 100 MHz. A moving average is applied to the oscillating I_D-V_G waveforms, and this averaged response shows excellent agreement with the steady-state DC simulation curve (Fig. 3b). This numerical result confirms that the oscillations drive the anomalous DC distortions, however counterintuitive the mechanism may initially appear.

These oscillations originate from an unintentional Hartley-type positive feedback loop [15], [16], [17] forming within the measurement setup, shown by the red arrows in the inset of Fig. 3b. When the FET g_m overcomes the loop's resistive losses and feedback attenuation, self-sustained oscillations are triggered [18]. These oscillations grow and modulate the FET's instantaneous operating point to the lower-g_m region, until the effective large-signal loop gain is compressed to unity. Due to the nonlinear I_D-V_G curve, these large-signal oscillations are rectified, generating a significant shift in time-averaged DC current. Given the reactive parasitic values in typical measurement setups, these oscillations occur in the 100 MHz to 1 GHz range, far beyond the bandwidth of standard DC instrumentation. Thus, the recorded DC I_D-V_G characteristics capture only the distorted, time-averaged values, as shown in Fig. 3b.

To experimentally validate the oscillation-induced distortion mechanism, we performed high-bandwidth I_D-V_G transient measurements on a 4 μm x 16 nm nFET in a DC setup with coaxial cables. The drain is held at 700 mV, and the gate is biased with a signal generator to provide a controlled quasi-static V_G sweep for waveform capture. The drain and gate are

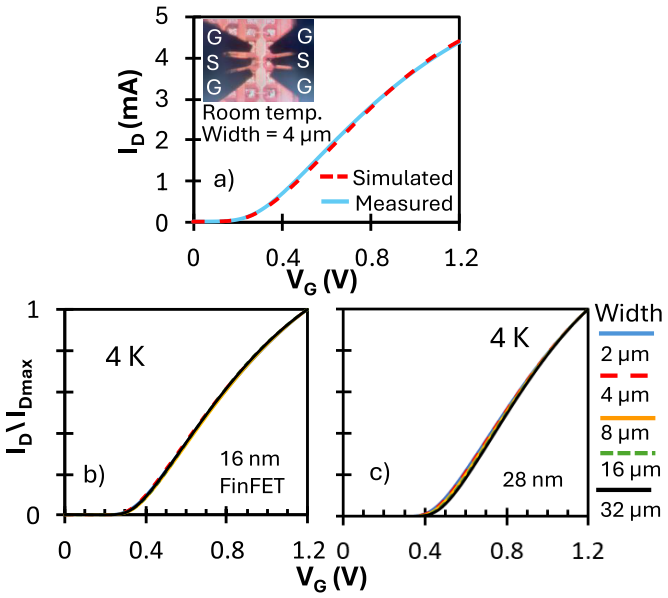

Fig. 4. Normalized I_D/I_{Dmax} vs. V_G characteristics at (a) 300 K and 4 K for FETs with widths of 2 μm, 4 μm, 8 μm, 16 μm, and 32 μm for (b) 16 nm FinFET and (c) 28 nm planar technologies using RF test structures.

monitored via the 1 MΩ input of an oscilloscope, and the I_D is monitored on the source side through a 50 Ω terminated input for signal integrity.

For a robust comparison of time-averaged I_D, the simulation duration was intentionally extended beyond the experimental window to ensure steady-state convergence, whereas the experimental window was chosen to maximize temporal resolution within the oscilloscope's memory depth. Fig. 3c shows the captured time-domain waveforms as well as the post-processed moving average of I_D, with the inset highlighting the captured oscillations in I_D. While the frequency differs slightly due to setup parasitic uncertainties, the oscillation amplitude closely matches the simulations (Fig. 3a). Fig. 3d compares the moving-average of transient data with the DC I_D-V_G measurement on the same FET in the same setup. The near-perfect agreement between these curves confirms that the anomalous DC distortions originate from these oscillations, consistent with our theoretical prediction.

Standard DC measurements are often presumed immune to high-frequency oscillations due to the low bandwidth of triaxial cabling. However, this assumption fails for nonlinear devices like MOSFETs. Unlike linear circuits where symmetrical oscillations average to zero, nonlinear FET characteristics rectify the signal and shift the measured DC value (Fig. 3d). The discrepancy between the I_D-V_G curves measured with and without oscillations underscores the critical need for an oscillation-free measurement environment, even for DC characterization.

IV. Suppressing Measurement-Induced Abnormities

To suppress these oscillations without noise or inaccuracy from resistive damping, minimizing loop inductance is the most effective strategy. Simulations indicate that maintaining measurement probe arm inductance below 20 nH is sufficient to ensure stable DC characterization (Fig. 2b). In conventional DC setups, inductance tends to be high due to discontinuities in the ground path, particularly in cryogenic systems designed for low-noise measurements using triaxial cables. For optimal results, RF probes with GSG-compatible test structures should be used (Fig. 4a inset), as they ensure the continuity of the ground path.

Fig. 4a shows the 300 K DC I_D-V_G characteristic of a 4 μm x 16 nm nFET identical to the device used in Fig. 1 with the sole difference being that GSG probes were used for the measurements instead of the DC probes. We note a remarkably close correspondence between the GSG measurements and the validated simulation of the DC I_D-V_G characteristic at 300 K. The 16 nm node at room temperature is chosen here as a representative case, since these FETs are well-characterized and validated models are available. This allows for a direct evaluation of how test structures and measurement setups influence observed device behavior. The comparison underscores the critical role of both probing architecture and measurement setup in achieving accurate device characterization, an essential foundation for building reliable compact models and ensuring predictive circuit design.

As established (Figs. 2 and 3), these artifacts are triggered whenever FET g_m exceeds the parasitic loop's high-frequency stability threshold. Our observation of similar anomalies in wide FinFETs at 300 K (Fig. 1c) identifies this as a fundamental measurement-system stability challenge. As technology scales toward high-g_m GAAFET [19], [20] and CFET [21], [22], the high-frequency stability margins in conventional DC setups will further erode, even at room temperature. Consequently, transitioning to RF-compatible metrology will become a requisite baseline for accurately characterizing any high-performance node in the high-g_m regime.

Finally, 4 K measurements of 28 nm and 16 nm nFETs using GSG probes (Figs. 4b and 4c) confirm the elimination of oscillation-induced abnormalities. These results demonstrate that low-inductance probing effectively restores accurate DC characteristics even in high-g_m regimes. Thus, GSG probing should be considered essential for characterizing high-g_m cryogenic devices for next-generation quantum control electronics.

V. Conclusion

This work identifies and resolves a critical source of error in cryogenic I_D–V_G measurements of advanced node FETs, namely, self-sustained oscillations arising from parasitic LC feedback in the measurement setup. These artifacts are often mistaken for intrinsic device behavior. Using both SPICE simulations and high temporal-resolution I_D–V_G measurements, we verified that these oscillations distort the measured DC current and demonstrated that they can be effectively suppressed by using GSG RF probes in place of conventional DC configurations. Our findings highlight the necessity of carefully engineered, metrology-aware test structures to ensure accurate device characterization when device transconductance is high. Such metrology-aware approaches are essential for developing reliable compact models and enabling the precise design of cryogenic electronics for scalable quantum systems.

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