Dielectric Encapsulated Niobium Films to Achieve Higher Processing Temperatures

Kirsten L. Lina, *Member, IEEE*, Anna E. Fox, *Senior Member, IEEE*, and Paul D. Dresselhaus

***Abstract*—To avoid degradation of circuit performance, fabrication processes for niobium-based superconductive electronics are typically limited to temperatures below 150 °C. In this study, we investigated protective dielectric capping layers that preserve the superconducting properties of Niobium (Nb) wiring at processing temperatures as high as 400 °C. To assess the thermal stability of Nb films, 400 nm thick Nb layers were deposited on oxidized silicon wafers and were either left uncapped or were intentionally capped with selected dielectric materials. The samples were subjected to postdeposition annealing in an argon atmosphere for comparison. Samples were annealed up to 450 °C, and changes in room temperature sheet resistance were used as a proxy for film degradation and checked with cryogenic measurements of samples annealed up to 400 °C. A sharp increase in room temperature sheet resistance, and a resulting decrease in residual resistivity ratio was observed in pristine Nb films above 300 °C. We found that the *ex-situ* deposition of insulating covering ("cap") reduces the onset of degradation. Notably, silicon oxide (SiO_x) capping shows significant improvement and silicon nitride (Si_xN_y) capped samples exhibit minimal changes in resistance across the full annealing range. These results suggest that Si_xN_y encapsulation as a dielectric "cap" preserves superconductive properties and offers an expanded thermal budget for Nb-based superconductive electronics, with implications for multilayer integration and scalable fabrication.**

***Index Terms*—Superconducting niobium fabrication.**

I. Introduction

NIOBIUM is a foundational material in superconductive electronics due to its high critical temperature (T_c = 9.2 K), favorable mechanical properties, compatibility with standard thin-film fabrication techniques, and ability to make high quality, high yielding Josephson junctions. Due to these advantages, Niobium is the basic superconducting material used in many low temperature superconducting (LTS) applications such as SQUIDS (superconducting quantum interference device) [1], superconducting detectors and readout [2], and voltage standard circuits [3]. Niobium thin films are also widely employed in superconducting integrated circuits such as qubit circuits [4], single flux quantum (SFQ) circuits [5], and Josephson junctions [6]; bulk Nb is used on radio-frequency (RF) cavities [7].

Received 5 February 2026; revised 16 April 2026; accepted 3 May 2026. Date of publication 7 May 2026; date of current version 4 June 2026. *(Corresponding author: Kirsten L. Lina.)*

The authors are with the National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: kirsten.lina@nist.gov; anna.fox@nist.gov; paul.dresselhaus@nist.gov).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2026.3691213.

Digital Object Identifier 10.1109/TASC.2026.3691213

Niobium's sensitivity to oxidation and structural degradation at modest thermal budgets [8], [9] limits its post-deposition processing to temperatures below 150 °C [10], [11], [12]. This limitation presents a challenge for multilayer integration, and high throughput manufacturing, particularly as superconducting technologies advance towards scalable, multilayer architectures [13]. Several studies recognize the mechanisms of Nb oxidation and the formation of resistive oxide layers post thermal and atmospheric exposure [14], [15], [16], [17], [18], [19]. These layers degrade electrical performance by increasing resistance of the Nb wiring and suppressing superconductivity. *In-situ* rf nitridation and vacuum annealing show promise in RF cavity performance improvement [9] and in Nb films [20], but these techniques have yet to be implemented in a scalable device fabrication stack-up.

Advanced Nb foundries are now typically fabricating 8 or 10 layer Nb devices, with intermixed Josephson junction layers and insulator layers as well as embedded resistor and inductor layers [13]. While these processes have impressive results, the circuit integration density remains many generations behind state-of-the-art semiconductor fabrication – partly caused by the inability to exploit the thermal budget needed to use advanced semiconductor tools and processes. This limitation is especially evident in Josephson junction technology, where the common barrier material, AlO_x, shares a similarly constrained thermal budget [21]. In contrast, amorphous-Silicon (α-Si) has achieved substantially higher critical current densities (J_c) with thermal treatment up to 300 °C without compromising junction quality [22], giving α-Si junction families an advantage over AlO_x barriers that are limited to 150 °C processing temperatures. Previous work to suppress oxide formation on the Nb surface and to prevent diffusion into the film demonstrated that surface passivation techniques can effectively eliminate surface oxides, including approaches such as *in-situ* nitride plasma passivation [20], Ar^+ ion milling [23], and encapsulation with thin metallic layers [24]. If Nb wiring layers can be stabilized against oxidation and diffusion at comparable temperatures, then integration with high performance α-Si junction families becomes practical. A robust dielectric cap that can suppress oxidation in Nb and preserve superconducting properties up to 400 °C directly supports junction stack integration and will help bridge the gap between foundry level superconducting and semiconducting fabrication capabilities.

While prior work has demonstrated improvements in Nb film stability using *in-situ* nitridation and vacuum annealing, these methods are difficult to scale for multilayer device

fabrication and do not address post-deposition processing compatibility. In this article, we study *ex-situ* encapsulation of two dielectric materials for Nb wiring to mitigate oxidation, and then measure the electrical and superconducting properties before and after thermal treatment. Unlike previous surface treatments, these standard thin-film fabrication workflows can be integrated into multilayer superconducting process stacks. We demonstrate that the encapsulated Nb structures maintain film integrity and superconducting performance up to 400 °C, far exceeding the traditional 150 °C processing thermal limit compared to samples with no encapsulation. These results establish a practical route for Nb-based superconducting electronics, enabling greater process flexibility and improved compatibility with emerging α-Si Josephson junction technologies.

II. Experimental Procedure

Three sample types were studied: unencapsulated Nb, Nb capped with SiO_x, and Nb capped with Si_xN_y. For this study, encapsulation was performed *ex-situ* in a plasma enhanced chemical vapor deposition (PECVD) system. All samples were measured for room temperature (RT) sheet resistance before thermal treatment, subjected to controlled thermal annealing, and finally characterized using room temperature and cryogenic electrical measurements.

A. Fabrication

Measurement structures were fabricated on high-purity, 76.2 mm diameter silicon substrates with 150 nm of thermal oxide. Lithography was performed using an i-line stepper with a critical dimension of less than 1 μm. Stress, layer thicknesses, and sheet resistances using a 4-point probe were measured across the wafer throughout processing for characterization of radial variations.

The base pressure of the vacuum chamber used for film deposition was 4×10^{-6} Pa with partial pressure of water, nitrogen, hydrogen being 133 nPa, 133 nPa, and 2660 nPa respectively. Prior to niobium deposition, the wafer surfaces were cleaned with a 6 min *in-situ* Ar RF plasma at 50 W with a chamber process pressure of 1.3 Pa and a −300 V substrate bias to remove surface contaminants. A 400 nm thick Nb layer was grown from a 76.2 mm diameter target by DC magnetron sputtering at 1 kW with a chamber process pressure of 0.64 Pa. Film stress was measured with a multibeam optical sensor, and controlled by tuning the chamber pressure to produce slightly compressive films, 200 MPa or less, in order to achieve the highest T_c film [26]. The substrate temperature during deposition was characterized to be approximately 60 °C via temperature indicator labels. Films had a nominal sheet resistance of 0.49 $\Omega/\square$ measured post deposition. The niobium film was patterned using standard photolithographic techniques and followed by an anisotropic inductively coupled plasma reactive ion etch (ICP/RIE) using an SF_6/Ar plasma.

Following the Nb patterning, an ICP/RIE PECVD tool was used to deposit 150 nm of SiO_x or Si_xN_y conformably, ensuring sidewall encapsulation. No dielectric was deposited on the unencapsulated device, but a native coating of Nb_2O_5 and sub oxides [4] upon exposure to atmosphere is expected. An *in-situ* Ar RF plasma clean was performed immediately prior to deposition of the dielectric films, minimizing interfacial contamination by removing the naturally occurring surface Nb_2O_5. An identical plasma cleaning process was used prior to deposition of either dielectric. SiO_x was formed using 2000 W/ 200 W ICP/RF plasma of N_2O and SiH_4 at 2 Pa. Optical properties of this composition yielded n = 1.47 at 633 nm determined by ellipsometry. Si_xN_y was deposited using 1000 W/ 0 W ICP/RF plasma of N_2 and SiH_4 at 1.3 Pa. Optical properties of this composition yielded n = 2.00 at 633 nm determined by ellipsometry.

Following the dielectric deposition, openings in the dielectric were defined for contact pads using photolithography and ICP/RIE etching with a trifluoromethane (CHF_3), Ar, and oxygen (O_2) plasma. The contact pad metalization process cleaned the substrate with an Ar RF clean, followed by a 10 s titanium (Ti) adhesion layer, and a 120 nm thick palladium gold alloy (PdAu) both deposited with DC magnetron sputtering. Wafers were then diced into 26 10 mm × 10 mm chips for annealing and testing.

B. Annealing

All chips were subjected to a baseline processing temperature of 150 °C during select photolithography steps. Thermal annealing experiments were conducted in a rapid anneal system with a silicon carbide chip carrier and a controlled atmosphere. Tests conducted in air, N_2, and forming gas environments established that argon best suppresses reactivity with impurities at the Nb surface. Argon atmosphere annealing yielded the most stable electrical behavior and reproducible results. Variations in purge duration were also explored, but did not produce measurable differences in electrical properties. Annealing steps were performed in an Ar atmosphere with a 3 min N_2 purge before each thermal cycle. Chips were annealed at 25 °C increments ranging from 175 °C to 450 °C, each for a duration of 10 min. A 10 percent overshoot of the target temperature was observed and consistent across samples, settling to the target temperature after 20 to 30 s.

III. Measurements

Electrical measurements of Nb film sheet resistance, residual resistivity ratio (RRR, defined as R_{300K}/R_{10K}), and the zero-resistance temperature (T_c), were used to asses the thermal stability of the etched Nb films. To measure both the longitudinal resistance and the sheet resistance, a structure with a 6 μm × 200 μm bar (33.33 squares) with electrodes on either end of the bar and a one square element measuring 6 μm × 6 μm was used. All resistances were measured using a bipolar technique of applying +/−1 mA to the structure and measuring voltage using a calibrated nanovoltmeter. Diced chips with these structures were affixed in a rapid test probe and immersed in liquid helium (LHe). A silicon diode thermometer was pressed in contact with the chip to monitor chip temperature. Room temperature resistance was measured at 293 K while low temperature resistance was

TABLE I
ROOM TEMPERATURE SHEET RESISTANCE IN Ω/□ OF HEAT TREATED SAMPLES

	150 °C	200 °C	300 °C	400 °C
Si_xN_y Cap	0.49	0.50	0.50	0.51
SiO_x Cap	0.49	0.50	0.52	0.60
No Cap	0.49	0.50	0.69	2.0

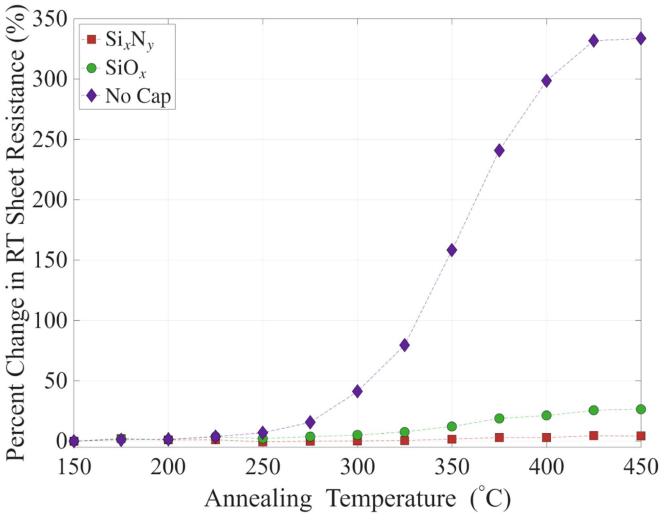

Fig. 1. Comparison of percent change in room temperature sheet resistance for Si_xN_y, SiO_x, and uncapped Nb wiring.

measured just above T_c near 10 K where resistivity is relatively constant. T_c of the structure was measured by sweeping temperature above a liquid helium bath and by lowering and raising the test probe to determine the zero of resistance.

IV. RESULTS

Parameters such as deposition process, deposition temperature, and film stress affect the morphology and grain size of the film, which can then be qualified using room temperature resistance, T_c, and RRR measurements [15], [21], [25]. Polycrystalline Nb thin films achieved using DC magnetron sputtering at room temperature and tuned for zero to slightly compressive film stress are known to be adequate for Josephson circuits, and typically have T_c>9 K and RRR ≈ 8 [26], as in this work.

Measured RT sheet resistance, RRR, and T_c, in all cases, show that the Nb thin film structures are degraded with sample annealing. Table I presents the raw RT sheet resistance data represented in Fig. 1 as a percent change as a function of annealing temperature, comparing RT sheet resistance measured before and after the heat treatment. Samples with dielectric capping layers exhibited minor degradation; an increase of approximately 4% for samples capped with Si_xN_y and 26% for samples capped with SiO_x up to 450 °C. Note the 333% increase in RT resistivity for sample structures with no dielectric cap (other than native Nb_2O_5). The RRR and T_c data in Figs. 2 and 3 show that the three wafers, both PECVD dielectric encapsulated and unencapsulated, retain superconducting properties up to 200 °C heat treatment. Available oxygen in these films does not diffuse significantly in this temperature range.

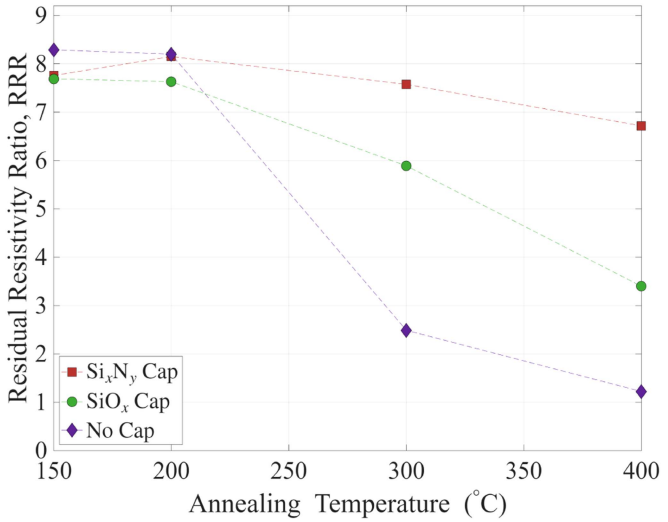

Fig. 2. RRR for Si_xN_y, SiO_x, and uncapped Nb, for heat treatment temperatures between 150 °C and 400 °C. Uncapped Nb RRR degrades rapidly between 200 °C and 300 °C. SiO_x capped films begin to see degradation at 250 °C while the Si_xN_y capped films retain high quality throughout this range.

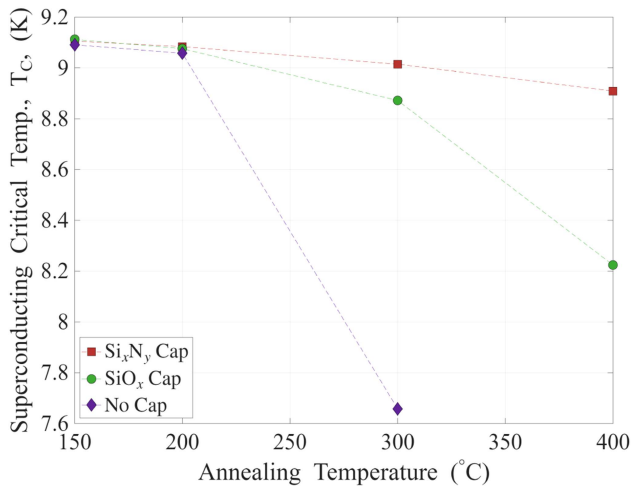

Fig. 3. Critical temperature for Si_xN_y, SiO_x, and uncapped Nb wiring, for heat treatment temperatures between 150 °C and 400 °C. Uncapped Nb degrades rapidly above 200 °C, and does not show a zero-resistance transition above LHe temperatures after 400 °C annealing.

In line with Fig. 1, application of post processing thermal treatment reduced the Nb T_c. Furthermore, the data remain consistent in that the films encapsulated using Si_xN_y exhibit T_c reduction of only 2% at 400 °C, while the films encapsulated using SiO_x reduced T_c by 10% at 400 °C. The unencapsulated film annealed at 400 °C did not have a superconducting transition above LHe temperatures.

V. DISCUSSION

It is well known that oxidation of Nb causes degradation of the superconducting properties specifically T_c and RRR, and increases normal state resistivity at 10 K [27], [28]. Oxidation may occur via multiple mechanisms including direct incorporation into the Nb lattice during sputtering [15] or post-deposition diffusion with temperature [29]. In this article, we

neglect the direct oxygen-incorporation during sputtering as the partial pressure of oxygen during sputtering was less than $\approx 7 \times 10^{-8}$ Pa, and films for all studied wafers were sputtered under similar conditions, thus wafers may be compared despite some incorporation during sputtering. Because the dielectric encapsulation layers were deposited *ex-situ*, all the Nb films in this trial were exposed to atmosphere postdeposition, where a surface layer of niobium oxide likely grew. For example, references [16], [17] found that Nb suboxides grow 1–2 nm thick followed by approximately 2–10 nm of Nb_2O_5 within hours of exposure to atmosphere. The grain structure and shape play an important role in natural surface oxidation. For DC sputtered thin Nb films on RF cleaned silicon oxide substrates, the grain size is on the order of 70 nm and has a columnar structure when deposited at nearly zero stress [30]. Oxidation on the surface, and within the fine columnar structure has been observed in Nb samples that have zero to slightly compressive stress [18]. It was found that a majority of the oxidation will occur on the surface, however, a minor, but nonnegligible amount will embed itself along the finely packed columnar grains [19].

After removal from the Nb deposition system, PECVD deposition was used to deposit the dielectric capping layers with an *in-situ* Ar RF plasma to remove surface contamination of the film prior to insulator deposition. Ar ions effectively clean the surface of the film, but only remove a few nanometers and cannot reach inside the grains. Though much of the surface niobium oxidation is removed, some oxygen will remain along the grain boundaries. Films with PECVD Si_xN_y were not exposed to oxygen during dielectric deposition whereas films encapsulated using SiO_x were exposed to N_2O plus SiH_4 as the precursor gasses used to form the silicon oxide (N_2O dissociates in the plasma to provide the oxygen source for SiO_2). The gas ratio used was $2.27 N_2O$: 1 SiH_4 yielding a 13.5% oxygen rich environment over stoichiometric silicon oxide for the standard SiO_2 recipe: for this reason we refer to this film as "SiO_x" rather than "SiO_2." Ellipsometer measurements indicate that the PECVD is forming stoichiometric SiO_2, meaning that the oxygen-rich environment within the PECVD encapsulation process and the high reactivity of the Ar plasma cleaned Nb surface may again oxidize the exposed Nb surface. The PECVD process is temperature controlled to 40 °C. Additionally, the slightly oxygen-rich PECVD may result in the incorporation of oxygen, which will dissociate and diffuse at temperatures of interest in this study [27].

A final significant source of oxygen is the atmosphere within the rapid thermal annealer. This tool does not have vacuum capability and therefore high purity is achieved by flowing a steady stream of 99.999% Ar gas through the process area. An initial purge plus a steady stream of Ar was flowed during annealing, but the background atmosphere was at least 1 ppm from the intrinsic gas impurities. At elevated temperatures, background oxygen can diffuse through a thin barrier of SiO_x[31]. Dielectric film thickness was fixed at 150 nm for this work, which may not provide a sufficient diffusion barrier.

If we assume that most of the oxygen is initially located at the film-dielectric interface, it will diffuse into the film during annealing according to the standard diffusion equation, dependent on initial oxygen concentration and diffusion coefficient. The diffusion coefficient should obey an Arrhenius-type relationship with temperature, determined by the activation energy and k_BT. Consequently, increasing the annealing temperature yields an exponential increase in oxygen diffusion [32].

With increasing temperature, the data shows that the unencapsulated Nb structure degrades significantly, with deviation from the capped samples with temperatures as low as 250 °C. The surface oxide, Nb_2O_5, is not stable at the study temperatures and readily decomposes into its sub-oxides releasing oxygen at the Nb surface [14], from experiments indicating that the surplus subsurface oxygen dissolves into the bulk [33].

Films with *ex-situ* PECVD SiO_x maintain their superconducting properties to somewhat higher temperatures. The available oxygen originates from the thin surface oxide remaining from the SiO_x deposition and from deep within the grains, additional background molecular oxygen can diffuse through thin SiO_2 at these temperatures [31]. As a source of oxygen from the SiO_x film itself, only interstitial oxygen could dissociate and migrate into the Nb. Stoichiometric SiO_2 is very stable and requires high temperature to decompose and is considered immobile.

Finally, the films with *ex-situ* PECVD Si_xN_y encapsulation show the least degradation in both the measured RRR and T_c values, with usable superconductive films surviving 400 °C annealing. The small, but significant improvement over the SiO_x encapsulated films is related to a reduced source of oxygen, either from less surface oxide formation during the encapsulation step or reduced diffusion through the cap during the annealing step. The data is insufficient to distinguish the source of oxygen. Note that even in the absence of surface oxide or diffusion through the encapsulation, the oxygen in the grain boundaries remains a source of impurities and would only be alleviated by *in situ* encapsulation.

VI. Conclusion

A series of multilayer Nb structures was studied to determine the thermal budget of superconducting films. It was found that pristine sputtered films degrade in both resistive and superconductive properties at temperatures greater than 200 °C. By encapsulating the Nb films with a dielectric layer (either SiO_x or Si_xN_y), the electrical properties remain minimally degraded for superconductive devices up to nearly 400 °C processing temperature. This degradation is attributed to oxygen incorporation in the films, which is diminished by dielectric encapsulation. This work demonstrates the importance of reducing oxygen incorporation during fabrication which yields greater improvement in film quality and thermal budget for more advanced superconductive circuits. *Ex situ* encapsulation of Nb supports foundry level fabrication capabilities and enables the advantages of thermally stable junction stack integration.

Acknowledgment

The authors acknowledge the support of NSA and useful discussions with Peter Hopkins, David Olaya, and John Biesecker. Fabrication support from the Boulder Microfabrication Facility staff is gratefully acknowledged. This work is a contribution of the U.S. government and is not subject to copyright in the United States.

REFERENCES

[1] J. Clarke, H. Weinstock, and R. W. Ralston, (Eds) "SQUIDS: Theory and Practice," in *The New Superconducting Electronics* (NATO ASI Series), vol. 251. Dordrecht, The Netherlands: Springer, 1993.

[2] K. D. Irwin, "An application of electrothermal feedback for high resolution cryogenic particle detection," *Appl. Phys. Lett.*, vol. 66, pp. 1998–2000, 1995.

[3] C. A. Hamilton, "Josephson voltage standards," *Rev. Sci. Instrum.*, vol. 71, no. 10, pp. 3611–3623, 2000.

[4] A. Murthy et al., "Developing a chemical and structural understanding of the surface oxide in a niobium superconducting qubit," *ACS Nano*, vol. 16, no. 10, pp. 17257–17262, 2022.

[5] M. Castellanos-Beltran, D. Olaya, A. Sirois, P. Dresselhaus, S. Benz, and P. Hopkins, "Stacked josephson junctions as inductors for single flux quantum circuits," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, May 2019, Art. no. 1300705.

[6] K. K. Likharev, O. A. Mukhanov, and V. K. Semenov, "Resistive single flux quantum logic for the Josephson-junction digital technology," *Squid*, vol. 85, pp. 1103–1108, 1985.

[7] H. Padamsee, "Superconducting radio-frequency cavities," *Annu. Rev. Nucl. Part. Sci.*, vol. 64, pp. 175–196, 2014.

[8] B. Baek, P. Dresselhaus, and S. Benz, "Thermal stability of Nb a- Nbx Si_{1-x} Nb Josephson junctions," *Phys. Rev. B*, vol. 75, no. 5, 2007, Art. no. 054514.

[9] A. Grassellino et al., "Nitrogen and argon doping of niobium for superconducting radio frequency cavities: A pathway to highly efficient accelerating structures," *Superconductor Sci. Technol.*, vol. 26, no. 10, 2013, Art. no. 102001.

[10] M. Henry et al., "Degradation of superconducting Nb/NbN films by atmospheric oxidation," *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, Apr. 2017, Art. no. 1100505.

[11] M. Yu et al., "The oxidation behaviors of high-purity niobium for superconducting radio-frequency cavity application in vacuum heat treatment," *Vacuum*, vol. 203, 2022, Art. no. 111258.

[12] J. Klaes, P. Rothweiler, B. Bornmann, R. Wagner, and D. Lützenkirchen-Hecht, "High-temperature treatments of niobium under high vacuum, dilute air- and nitrogen-atmospheres as investigated by in situ x-ray absorption spectroscopy," *J. Synchrotron Radiat.*, vol. 28, pp. 266-277, 2021.

[13] S. Tolpygo et al., "Inductance of circuit structures for MIT LL superconductor electronics fabrication process with 8 niobium layers," *IEEE Trans. Appl. Supercond.*, vol. 25, no. 3, Mar. 2015, Art. no. 1100905.

[14] Q. Ma and R. Rosenberg, "Surface study of niobium samples used in superconducting RF cavity production," in *Proc. Part. Accel. Conf.*, Chicago, IL, USA, 2001, pp. 1050–1052.

[15] M. Manzo-Perez et al., "Effects of residual oxygen on superconducting niobium films," *Appl. Phys. Lett.*, vol. 125, no. 11, 2024, Art. no. 112602.

[16] M. Grundner and J. Halbritter, "On the natural Nb_2O_5 growth on nb at room temperature," *Surf. Sci.*, vol. 136, pp. 144–154, 1984.

[17] J. Halbritter, "On the oxidation and on the superconductivity of niobium," *Appl. Phys. A*, vol. 43, pp. 1–28, 1987.

[18] M. D. Henry, S. Wolfley, T. Monson, B. G. Clark, E. Shaner, and R. Jarecki, "Stress dependent oxidation of sputtered niobium and effects on superconductivity," *J. Appl. Phys.*, vol. 115, no. 8, 2014, Art. no. 083903.

[19] Z.-H. Sung, P. J. Lee, and D. C. Larbalestier, "Observation of the microstructure of grain boundary oxides in superconducting RF-quality niobium with high-resolution TEM (transmission electron microscope)," *IEEE Trans. Appl. Supercond.*, vol. 24, no. 1, pp. 68–73, Jan. 2014.

[20] T. Shiota, T. Imamura, and S. Hasuo, "Plasma nitridation process for superconducting Nb wiring to improve their annealing stability," *J. Appl. Phys.*, vol. 70, no. 11, pp. 6959–6965, 1991.

[21] T. Imamura, T. Shiota, and S. Hasuo, "Fabrication of high quality Nb/AlO_x-Al/Nb Josephson junctions. I - sputtered Nb films for junction electrodes," *IEEE Trans. Appl. Supercond.*, vol. 2, no. 1, pp. 1–14, Jan. 1992.

[22] D. Olaya et al., "Nb/a-Si/Nb josephson junctions for high-density superconducting circuits," *Appl. Phys. Lett.*, vol. 122, no. 18, 2023, Art. no. 182601.

[23] M. Bal et al., "Systematic improvements in transmon qubit coherence enabled by niobium surface encapsulation," *Quantum Inf.*, vol. 10, no. 43, pp. 1–8, 2024.

[24] R. D. Chang et al., "Eliminating surface oxides of superconducting circuits with noble metal encapsulation," *Phys. Rev. Lett.*, vol. 134, no. 9, 2025, Art. no. 097001.

[25] S. Knappe, C. Elster, and H. Koch, "Optimization of niobium thin films by experimental design," *J. Vac. Sci. Technol. A*, vol. 15, no. 4, pp. 2158–2166, 1997.

[26] L. van Loyen, D. Elefant, V. Palmieri, W. Venrurini, and J. Halbritter, "Topography and electrical properties of sputtered niobium films," in *Proc. 1997 Workshop RF Supercond.*, Abano Terme (Padova), Italy, 1997, pp. 1119–1124.

[27] W. DeSorbo, "Effect of dissolved gases on some superconducting properties of niobium," *Phys. Rev.*, vol. 132, no. 1, pp. 107–123, 1963.

[28] C. C. Koch, J. O. Scarbrough, and D. M. Kroeger, "Effects of interstitial oxygen on the superconductivity of niobium," *Phys. Rev. B*, vol. 9, no. 3, pp. 888–897, 1974.

[29] C. Benvenuti, S. Calatroni, and V. Ruzinov, "Diffusion of oxygen in niobium during bake-out," in *Proc. 10th Workshop RF Supercond.*, Tsukuba, Japan, 2001, pp. 441–442.

[30] B. Okolo, P. Lamparter, U. Welzel, and E. Mittemeijer, "Stress, texture, and microstructure in niobium thin films sputter deposited onto amorphous substrates," *J. Appl. Phys.*, vol. 95, no. 2, pp. 466–476, 2004.

[31] T. Hoshino et al., "Diffusion of molecular and atomic oxygen in silicon oxide," *Jpn. J. Appl. Phys.*, vol. 42, pp. 3560–3565, 2003.

[32] R. J. Farraro and R. B. McLellan, "Diffusivity of oxygen and nitrogen in niobium," *Mater. Sci. Eng.*, vol. 33, pp. 113–116, 1978.

[33] M. Delheusy et al., "X-ray investigation of subsurface interstitial oxygen at Nb/oxide interfaces," *Appl. Phys. Lett.*, vol. 92, no. 11, 2008, Art. no. 101911.