# 130-nm CMOS-Integrated Superparamagnetic Tunnel Junction-Based p-bit

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***Abstract*— Probabilistic computers offer promising solutions for computationally hard problems in domains such as combinatorial optimization and machine learning. A key building block in these systems is the probabilistic bit (p-bit), which relies on superparamagnetic tunnel junctions (sMTJs) as its source of randomness. A challenging threshold to cross for scaling sMTJ-based p-bit systems is integration of sMTJs with CMOS technology. In this work, we present experimental results of a p-bit unit cell using sMTJs integrated with 130 nm CMOS technology and demonstrate that the sMTJ's resistance fluctuations can generate a corresponding fluctuating digital output voltage which is tunable via the input voltage. These findings establish the feasibility of CMOS-compatible, sMTJ-based probabilistic circuits and mark a key step toward scalable hardware for real-world probabilistic computing applications.**

***Index Terms*— CMOS integrated circuits, Spintronics.**

## I. Introduction

COMPUTATIONALLY hard tasks like combinatorial optimization and machine learning are deemed difficult for conventional deterministic computers. Probabilistic computing is an alternative computing method using probabilistic bits (p-bits) fluctuating in time between a digital high and low state [1]. When computationally hard problems are formulated into an Ising Hamiltonian [2], these fluctuations allow the computer to probabilistically sample a multitude of configurations. Recent probabilistic computers using field-programmable gate arrays (FPGAs) have demonstrated increasingly larger problem sizes [3] by utilizing concepts like parallel-tempering [4] and sparse encoding [5]. To scale to larger problems for real-world applications, p-computers using nanodevices as the source of randomness show potential for high-speed, low-power and low-area solutions [1], [6], [7], [8], [9].

A superparamagnetic tunnel junction (sMTJ) is a functional nanodevice containing a low barrier nanomagnet with potential for providing the randomness in p-bits. sMTJs are composed of two ferromagnetic layers separated by a tunnel barrier. The sMTJ can show a high or low resistance, depending on the angle of orientation between a reversible free and a fixed magnetization layer owing to the tunneling magnetoresistance (TMR) effect [10]. In contrast to magnetic tunnel junctions (MTJs) used in magnetoresistive random access memory [11], [12], sMTJs feature drastically reduced energy barriers so thermal fluctuations cause the device's state to probabilistically change on a nanosecond timescale [13], [14].

So far, sMTJ-based p-bits have been used to solve a multitude of problems [8], [15], [16], [17], [18], [19] and are typically represented with a unit cell circuit consisting of an sMTJ in series with an n-channel MOS (NMOS) transistor whose drain output is fed into an inverter [20]. The NMOS gate voltage is used to change the current flowing through the sMTJ, tuning the time it spends in one state and thus producing tunable binary voltage fluctuations between high and low [15], [16]. This tunable aspect of the p-bit is what allows the system to sample the energy landscape of the Ising Hamiltonian.

Current p-bit prototypes consist of sMTJs wire-bonded to a circuit board with an NMOS and an inverter; however, to show their potential as a highly-compact and high-speed solution, results showing large-scale ASIC operation are required. Therefore, a key phase of sMTJ-based p-bit development is the systematic study of back-end-of-the-line (BEOL) integration of s-MTJs with CMOS. This involves isolating each stage of the p-bit circuit to quantitatively evaluate properties suitable for both the CMOS and the sMTJ. In this work, we successfully integrate sMTJs with 130 nm CMOS technology, evaluate challenges of integration at each stage of the circuit, and demonstrate the operation of a complete p-bit unit cell.

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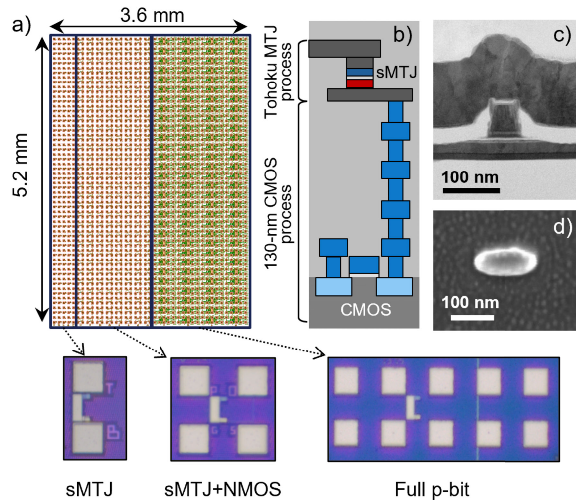


Fig. 1. (a) Layout schematic of test chip with 150 isolated sMTJs, 240 sMTJs in series with an NMOS transistor, and 150 full-stage p-bit circuits. b) Schematic of the cross-sectional structure of the integrated chip. c) cross-sectional scanning transmission electron micrograph of an sMTJ integrated above the CMOS. d) Plan-view scanning electron micrograph of an sMTJ.

## II. Chip Design and Fabrication

We systematically design a CMOS-integrated p-bit circuit to verify its functionality at each maturity stage. The 5.2 mm $\times$3.6 mm monolithic chip containing 150 isolated sMTJs, 240 sMTJs in series with an NMOS transistor, and 150 full-stage p-bit circuits, is fabricated using a 130-nm commercial CMOS process line and a dedicated MTJ process line at Tohoku University (Fig. 1 a,b). We design the sMTJ + NMOS circuit with electrodes for the gate, source, power-supply voltage $V_{\mathrm{DD}}$, and output connections. For the full-stage p-bit circuit, we design a cascode stage in series with the sMTJ to reduce the effect that the fluctuating resistance of the sMTJ has on the modulation of the source-drain current. The output feeds to the input of a variable threshold controller (VTC), containing two pull-up and two pull-down transistors, that collectively represent threshold voltages from 0.7 V to 1.1 V with a 100-mV step. The VTC stage output feeds into a final inverter which produces voltage fluctuations between 0 V and 1.8 V. The circuits for the sMTJ + NMOS and full stage are completed by patterning an sMTJ between the output (or input to VTC) pads containing vias to the CMOS and $V_{\mathrm{DD}}$. To enable a wide range of currents, the transistors are designed with channel widths of 1, 3, 9, 27 $\mu$m, producing currents from hundreds of $\mu$A to tens of mA.

To enable BEOL integration of sMTJs, the final encapsulating CMOS metal layer is left off, giving direct contact to the five metal and four via layers below. Doing so helps keep the roughness of the BEOL interface to a minimum, but carries the risk of the tungsten vias oxidizing. To prevent this, wafers were immediately coated in photoresist, where a mild removal process was used to clean the surface before material stack deposition. After photoresist removal, we first performed four-point probe measurements on the top and bottom electrodes to confirm ohmic contact. Furthermore, to reduce any impact of roughness from the vias, sMTJs are not patterned directly above the vias, but in an area of similar topography for each stage of the p-bit. Before BEOL integration, we performed vibrating sample magnetometry measurements of the magnetic properties of the materials stack in the case of deposition above a bare silicon wafer and the chip used in this work. We noticed no considerable difference in the magnetic properties.

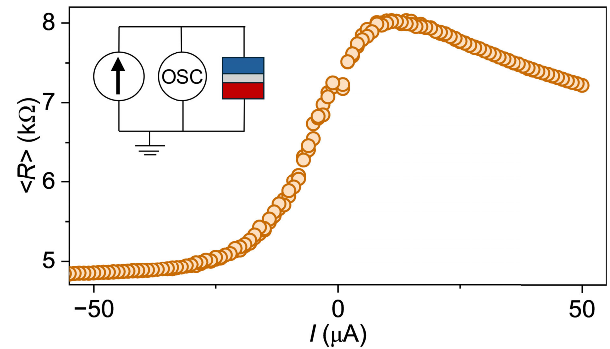


Fig. 2. Time-averaged resistance versus applied current for a single sMTJ with 25 nm $\times$100 nm dimensions. (inset) Experimental measurement setup.

We deposit the sMTJ stack above the CMOS circuits by DC and RF magnetron sputtering at room temperature of the following stack structure: Ta(5)/ PtMn(20)/ Co(2.4)/ Ru(0.9)/ CoFeB(2)/ MgO/ CoFeB(2.1)/ Ta(5)/ Ru(5)/ Ta(50) (thicknesses in nm). The sMTJs are patterned into circular pillars with diameters 50, 60, 70, 80 nm by Ar+ ion milling and reactive ion etching. Elliptical sMTJs are also patterned with aspect ratios of 1, 2, 3, 4 with major-axis and minor-axis diameters adjusted to keep the same magnetic volume as the circular sMTJs (Fig. 1 c,d).

## III. Experimental Results

To confirm electrically tunable stochastic behavior of the isolated sMTJs, the time-averaged resistance $< R >$ is evaluated as a function of applied current in a single sMTJ (Fig. 2). Measurements were performed by connecting DC probes to top and bottom electrodes, applying a DC current, and reading voltage fluctuations on an oscilloscope. The time-averaged voltage at each current is read through the same source-measure unit supplying the current and averaged for 100 samples taken at 10 ms intervals. At sufficiently large negative current, both ferromagnetic layers are parallel, and the device exhibits a low resistance. As the current increases to positive, the free ferromagnetic layer fluctuates in time and eventually settles into the antiparallel configuration, leading to the sigmoidal behavior shown. At even higher current, the tunnel magnetoresistance decreases with applied voltage, an effect commonly observed and thoroughly investigated in MTJs. Works have show that the slope of the sigmoidal region where the device resistance is fluctuating in time is dependent on the device diameter [21]. With varied diameters and aspect ratios, we measured a wide range of low resistance values ranging from 2.5 kΩ to 8 kΩ, and TMR ratios ranging from 50 % to 100 %. We also performed measurements on the random telegraph noise of the sMTJs, where devices showed fluctuations with ms dwell times (not shown).

Next, we present results of sMTJs integrated in series with an NMOS transistor to characterize a range of gate voltages required to tune the sMTJ (Fig. 3). In the full-stage p-bit, this gate voltage will act as the input to one p-bit cell. Figure 3(a) shows the time-averaged output voltage $< V_{\mathrm{out}} >$ of an sMTJ as the gate voltage $V_{\mathrm{gate}}$ is swept from 0.7 V to 1.0 V. Each

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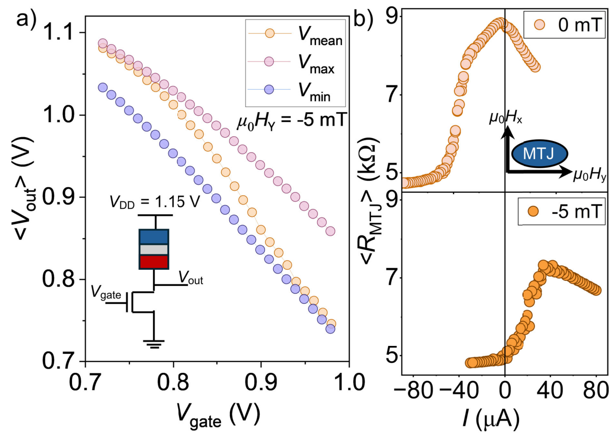


Fig. 3. (a) Time-averaged characteristics of an sMTJ (dimensions: 25 nm ×100 nm) integrated in series with an NMOS transistor (channel width 1 $\mu$m). $V_{max}$ and $V_{min}$ represent the maximum and minimum voltages of $V_{out}$ read as $V_{gate}$ is increased. $V_{mean}$ is the mean voltage measured, demonstrating sMTJ's state tunability. (inset) Circuit schematic of an sMTJ and NMOS transistor. (b) Time-averaged sMTJ resistance versus current plots showing the shift of the center of the sMTJ curve with applied magnetic field.

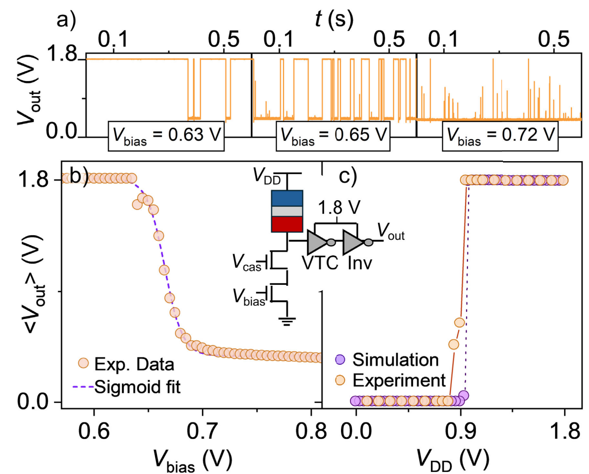


Fig. 4. (a) Time-series measurements of $V_{out}$ for three Vbias set points. The dimensions of the sMTJ for this device are 25 nm ×100 nm and the NMOS channel width is 1 $\mu$m. (b) time-averaged characteristics of the same device shown in a). (c) $V_{out}$ as a function of $V_{DD}$ when the p-bit input ($V_{cas}$, $V_{bias}$) is 0 V. (inset) Circuit schematic for the full-stage p-bit.

point is averaged over 20,000 points at a 10 kHz sampling rate. Measurements are performed by applying a DC voltage to both the gate of the NMOS and $V_{DD}$, which connects to the top electrode of the sMTJ. As the gate voltage increases/decreases, more/less current flows through the sMTJ. Accordingly, the time that the sMTJ spends in the high or low resistance state is tuned, following the result shown in Fig. 2. The output voltage $V_{out}$, read on an oscilloscope at the NMOS drain, is then a function of $V_{sMTJ}$ subtracted from $V_{DD}$.

For the sMTJ shown here, this results in a voltage swing at $V_{out}$ of 100 mV near $V_{gate}$ = 0.85 V. Due to a stray magnetic field [22] from the reference layer, the range at which the sMTJ shows resistance fluctuations is for negative currents at zero magnetic field. This range can be shifted to a positive current regime by applying a small field along the long axis opposite the stray field (Fig. 3 b). As the CMOS circuit can generate only positive currents, we apply this field in the full-stage p-bit experiment as well. Note that this stray field can be easily tuned by optimizing the stack of the reference material.

Finally, we verify a single cell of the full stage p-bit containing electrodes for $V_{DD}$, $V_{cas}$, $V_{bias}$, $V_{out}$, and ground (inset of Fig. 4 b). We set $V_{cas}$ to a voltage that pins the drain of the NMOS controlled by $V_{bias}$, which is the transistor used to change the sMTJ current, $V_{DD}$ to a voltage that when subtracted with the sMTJ voltage drop will result in a fluctuating input at the VTC, and $V_{OUT}$ to the input of an oscilloscope. The time-series response of the p-bit at three bias points (Fig. 4 a) demonstrates the tunability of the p-bit output with $V_{bias}$. As $V_{bias}$ is swept from 0.5 V to 0.8 V at a 5 mV step, $< V_{out} >$ where each poin is time-averaged over 200,000 points transitions from 1.8 V to 0.45 V, showing a sigmoid-like behavior (Fig. 4 b). These results indicate that the circuit with an sMTJ integrated here functions as a p-bit. Ideally, the inverter stage should drive outputs from 1.8 V to 0 V. This issue arises from non-idealities in the physical properties of the CMOS (Fig. 4 c) which we confirm by applying 0 V to both $V_{bias}$ and $V_{cas}$ so that $V_{DD}$ drops entirely at the input of the VTC. Doing so shows a stepped increase in the inverter output starting at $V_{DD}$ = 0.8 V, not shown in circuit simulations [23].

The ultimate goal for p-bit hardware is to scale the circuit to smaller CMOS technology nodes. Other works have shown simulations of this p-bit unit cell scaled down to 7 nm CMOS technology, and report large gains in area and energy [8]. Experimentally scaling, however, will require co-optimization of both the sMTJ properties and the CMOS. For example, CMOS inverter stages at different nodes exhibit varying voltage transfer characteristics, where small sMTJ voltage swings incapable of driving the transistor from 0 V to $V_{DD}$ cause high static leakage that dominates overall power consumption. For the sMTJ presented in Fig. 4, this results in 72 $\mu$W static leakage from the CMOS and 23 $\mu$W from the sMTJ. By increasing the swing, the static leakage is mitigated, bounding the total power by the intrinsic device power and dictating that p-bit efficiency requires maximizing sMTJ voltage swing while minimizing bias current. Fortunately, CMOS scaling assists this optimization; transitioning from a 130-nm node requiring a 300 mV swing [23] to a 22-nm node lowers the required swing to 150 mV [24], effectively accommodating a broader range of sMTJ properties and their distributions.

## IV. Conclusion

In this work, we have added a key step towards the realization of scaled p-computers by experimentally demonstrating a fully CMOS integrated sMTJ-based p-bit circuit. To understand the impact of sMTJ parameters on circuit performance, it will be crucial to combine both simulation and experiments, systematically studied at various CMOS nodes. Nevertheless, these results show the potential readiness of sMTJ-based p-bits to be used in large-scale circuits for solving computationally hard problems.

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