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ABSTRACT

Wide bandgap semiconductors, including gallium nitride (GaN), are crucial for next-generation power electronics due to their superior properties compared to silicon. However, challenges in their fabrication, particularly with epitaxial regrowth for vertical diode device structures, can introduce defects that impact performance. In this study, we report on vertical GaN pn diodes that exhibit an exceptionally large hysteresis loop with on/off ratios exceeding nine orders of magnitude, a behavior absent in devices grown *in situ* without changing growth reactors. We demonstrate that these devices exhibit robust endurance, maintaining a stable memory window for over 60 000 switching cycles at room temperature (20 °C), and remain partially viable up to at least 275 °C. Through analytical characterization, including secondary ion mass spectrometry and electroluminescence, we provide evidence that the hysteresis behavior is linked to a defect-rich interface region containing silicon and carbon impurities. To further investigate the underlying mechanism, we developed a technology computer aided design model that successfully replicates the observed hysteresis and identifies the likely mechanisms involved, key attributes of which include interfacial barriers, fixed negative charge, and positive charge trapping. These findings highlight a critical challenge for traditional GaN power devices while also demonstrating their potential for novel high-temperature memory applications.

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Semiconductor devices engineered to control and convert electrical power are crucial components in a wide range of modern applications, including artificial intelligence data centers and electric transportation.[1–4] While traditionally based on silicon technologies, current power electronics trends demand greater efficiency, higher voltage and current ratings, and superior thermal management.[1–4] Wide bandgap semiconductors are a key enabler for these requirements and have emerged as a commercially viable solution with rapid market share growth.[1–4]

Gallium Nitride (GaN), with a bandgap of about 3.4 eV, is one of the most promising wide bandgap material systems with several GaN-based products currently in production.[1–4] Compared to silicon, with a bandgap of 1.1 eV, GaN can withstand higher electric fields and temperatures, exhibits higher electron mobility and thermal conductivity, and displays lower on-resistance.[1–4] Notably, pn GaN vertical diodes offer significant improvements in efficiency, size, and performance over silicon-based counterparts and are poised to address the growing demand for energy-efficient power electronic solutions across a wide range of industries.[1–4]

However, GaN technologies are still maturing, requiring specialized and often more complex manufacturing processes.[5,6] Combined with the high cost of substrates, GaN devices are therefore more

expensive to produce than comparable silicon components.[5,6] Significant challenges also remain in materials integration and defect abatement, hindering more widespread commercialization.[5,6]

One such challenge is the difficulty of selective doping of GaN layers for vertically oriented devices.[5,6] Conventional silicon doping methods, such as ion implantation and diffusion, have been shown to be inadequate and are currently commercially unviable.[5,6] Consequently, most vertical GaN power devices require epitaxial growth for each device layer to achieve the desired level of doping.[5,6] This costly and time-consuming process is known to introduce various impurities and atomic-scale crystal defects at the growth interface, leading to significant performance, reliability, and yield challenges.[5,6] Specifically, epitaxial regrowth of the p-GaN layer for diode fabrication is known to introduce accumulation of silicon impurities at the interface.[7–11] Several possible explanations for the origin of the silicon contamination have been proposed and is currently an active area of research.[7–11] Nevertheless, it is generally reported to have a negative impact on the performance of devices designed for power electronic applications.[8,12,13] Devices known to contain impurities at the regrowth interface, including GaN and other nitride structures, have also been reported to display memristor-like resistance switching behavior.[14–17] While such hysteresis is typically undesirable for traditional power device applications, it has potential applications as a high-temperature or high-voltage memory device, possibly integrated on-chip with GaN high electron mobility transistors.

In this study, we report on pn vertical GaN diodes that exhibit an exceptionally large memory window hysteresis loop, exceeding previous reports by several orders of magnitude in on/off ratios. We demonstrate that these devices provide a repeatable and robust memory window with over 60 000 switching cycles and remain at least partially viable at temperatures up to 275 °C. To uncover the underlying physical mechanism responsible for this behavior, we perform comprehensive analysis, including secondary ion mass spectroscopy (SIMS) and electroluminescence (EL). Finally, we use technology computer aided design (TCAD) modeling to link our analytical and electrical findings and propose a plausible physical model for the processes involved. While the characterization of these candidate memory devices is far less elaborate than the exhaustive evaluations that are needed to test commercial memory viability, the remarkable memory window, and its stability, motivates this report for future GaN memory or selector research.

The pn vertical diodes used in this study were fabricated on identical GaN dot-core[18,19] substrates. Two sets of devices were prepared, with the key difference being that one set of devices consisted of a regrowth interface (i.e., experienced a break in vacuum before the p-GaN deposition), while the other did not (i.e., *in situ* grown). The regrowth procedure of pn GaN diodes followed similar reported procedures.[20,21] Both sets have identical contact metallization consisting of a patterned Pd/Pt/Au anode on the p-GaN and a Ti/Al/Ni/Au cathode on the GaN substrate.

Figure 1(a) schematically illustrates the device cross sections. Sample A devices were grown via an *in situ* epitaxial process within the same reactor. These devices consist of an 8 μm drift layer ($n \approx 1.7 \times 10^{16}\,cm^{-3}$) followed by a 400 nm p-layer ($[Mg] \approx 4 \times 10^{17}\,cm^{-3}$). As shown in Fig. 1(b), these devices do not exhibit any measurable hysteresis behavior. Sample B devices were fabricated by first epitaxial growth of a 5 μm drift layer ($n \approx 2 \times 10^{16}\,cm^{-3}$), followed by a break in vacuum before regrowth of a 400 nm p-layer ($[Mg] \approx 4 \times 10^{17}\,cm^{-3}$). As shown in Fig. 1(b), these devices display an exceptionally large current vs voltage (IV) hysteresis with on/off ratios exceeding nine orders of magnitude at 20 °C. As noted in later discussion, future work should include focused efforts to recreate, benchmark, and then optimize the processing steps that produced this behavior.

The electrical measurements shown in Fig. 1(b) reveal a stunning difference between the current vs voltage (I–V) characteristics of the two samples. Sample A displays a rather ordinary I–V curve, whereas sample B displays an exceptionally large hysteresis loop. These quasi-DC I–V curves were made at 20 °C utilizing a commercial semiconductor parameter analyzer with a current compliance limit of 100 mA. Applied voltage uncertainty varies with the selected applied voltage magnitude. This uncertainty is less than 0.018% of the applied voltage magnitude, plus an additional 6 mV. Measured current uncertainty is less than 10 pA. Each curve, with a measurement time of approximately one second, consists of a forward and reverse voltage sweep, in which the sweep starts at 0 V, increases to the maximum indicated voltage, and then immediately sweeps back to 0 V, as indicated by the arrows.

From a traditional power electronics engineering perspective, the predictable and well defined I–V response of sample A is clearly more desirable than the behavior of sample B. However, the hysteresis of sample B is so pronounced that one cannot help but draw comparisons to applications where this behavior is desirable, particularly memory devices and/or selector devices based on memristive switching of various oxide layers.[14–17] Given the large bandgap compared to silicon-based memory devices, a GaN-based memory device could potentially operate at higher temperatures and/or in more extreme environments.[1–4]

To explore this possibility, we performed a series of measurements to observe the hysteresis behavior as a function of temperature, the results of which are illustrated in Fig. 2. As shown in Fig. 2(a), quasi-DC IV measurements, similar to Fig. 1(b), were made at each temperature. Note, for visual clarity, these curves are plotted on a linear scale, and each curve is artificially offset 0.1 A. These curves are plotted on a logarithmic scale in the supplementary section. Next, the ratio of high resistance (I_{High}) state to low resistance state (I_{Low}) was calculated for each voltage. The maximum ratio value for each temperature is plotted in Fig. 2(b). We note that the voltage at which the maximum ratio occurred remained relatively constant at about 6 V. We find that even small increases in temperature above ambient (20 °C) rapidly reduce the switching window ratio on the lower voltage (low resistance state) side by many orders of magnitude, as shown in Fig. 2. The temperature dependence saturates at about 75 °C, and the on/off ratio then remains nearly constant at about a factor of two up to 275 °C, the maximum temperature in our commercially available wafer probing station is capable of (uncertainty in applied temperature is ±2.5 °C).

In order to emulate memory element programming and erasing cycles, pulse-based endurance cycling measurements utilizing an arbitrary waveform pulse-measure unit of a commercial semiconductor parameter analyzer (Fig. 3) were utilized. As illustrated in Fig. 3(a), the waveform used emulates that of a repetitive program/erase operation, which cyclically switches the device from its low resistance state to the high resistance state (SET operation) and then from the high

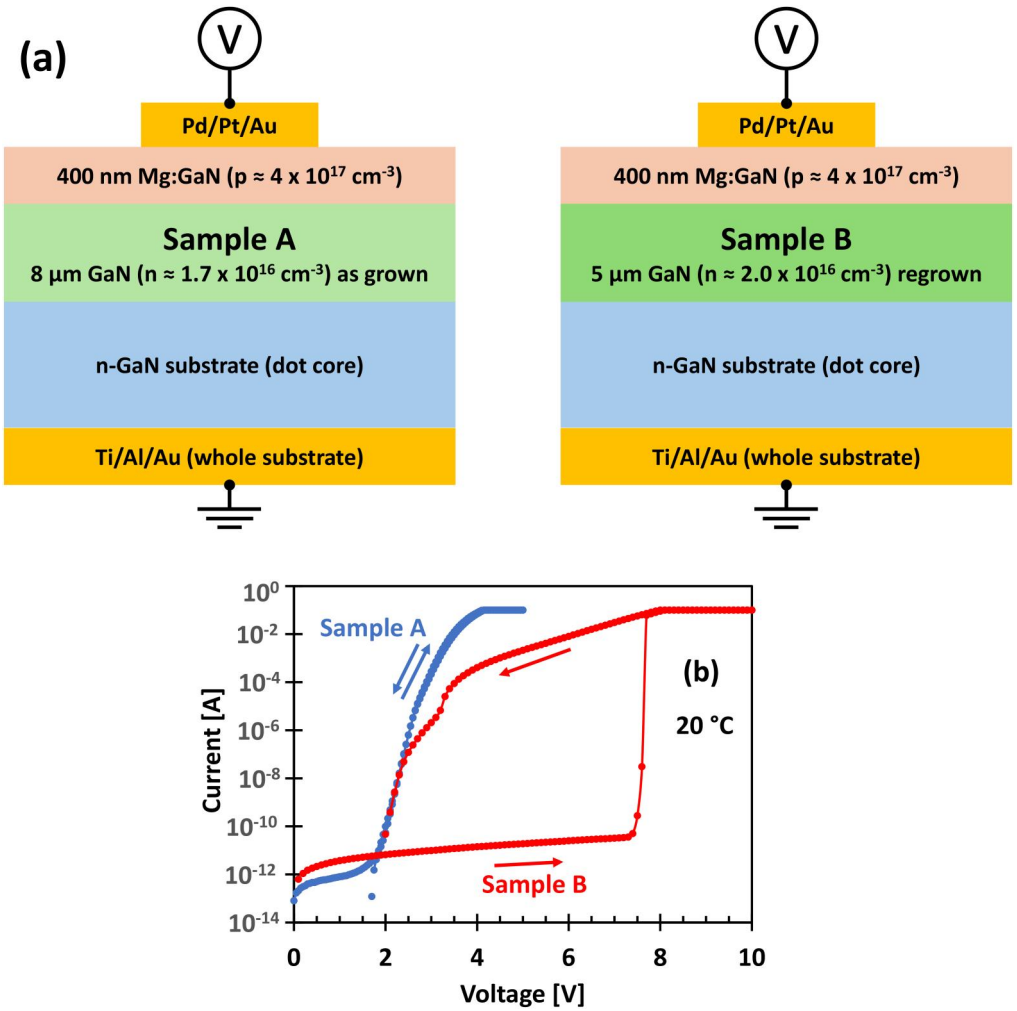

FIG. 1. (a) Schematic cross sections of the device structure. Samples A and B, described in the text, are nominally identical except for the drift layer thickness/doping, and the fact that sample B experienced a break in vacuum before regrowth. (b) Representative quasi-DC vs voltage measurements performed on both sets of samples at 20 °C. Sample A displays no measurable hysteresis, while sample B displays an exceptionally large hysteresis with on/off ratios exceedingly nine orders of magnitude. Arrows indicate voltage sweep direction. Current compliance was set at 100 mA.

resistance state back to the low resistance state (RESET operation). The waveform also includes an intermediate low voltage step (READ operation) after each switching event, which is used to measure the device current while in high (I_{High}) and low (I_{Low}) resistance states (thus providing the respective resistance values). The voltages used for SET, RESET, and READ operations were $V_{SET} = 10$ V, $V_{RESET} = -10$ V, and $V_{READ} = 4$ V, respectively. The time spent at V_{SET}, V_{RESET}, and V_{READ} was $t_{SET} = 100$ ms, $t_{RESET} = 4$ s, and $t_{READ} = 100$ ms, respectively. The uncertainty in applied voltage, measured I_{High}, measured I_{Low}, and timing characteristics are less than 10 mV, 1 μA, 10 nA, and 1 ns, respectively. The reset dynamics exhibits a strong dependence on the applied bias. Attempts to use shorter t_{RESET} times at −10 V did not successfully place the device back into the low current state; hence, the RESET operation required a much longer time compared to SET. While a larger V_{RESET} would likely shorten the required RESET time, equipment limitations precluded our attempts. While this timescale is incompatible with high or medium frequency memory applications, it could be relevant for low frequency memory circuits integrated directly into GaN high-voltage power electronics platforms and/or serve as embedded configuration or selector devices. In these types of platforms, much higher voltages than those utilized in this study would be available on chip and could be used to significantly reduce the reset time.

It should be noted that while no rigorous effort was made to measure the retention time, including any type of optimization of read voltage to eliminate the possibility of read-disturb events, we qualitatively note that no loss or state was observed throughout the course of our measurement and study. This places a lower bound on the possible retention time of order days and weeks, with the actual value likely being much longer.

Figure 3(b) illustrates the results of the cycling measurements, plotted on a linear scale, by comparing I_{High} and I_{Low} as a function of

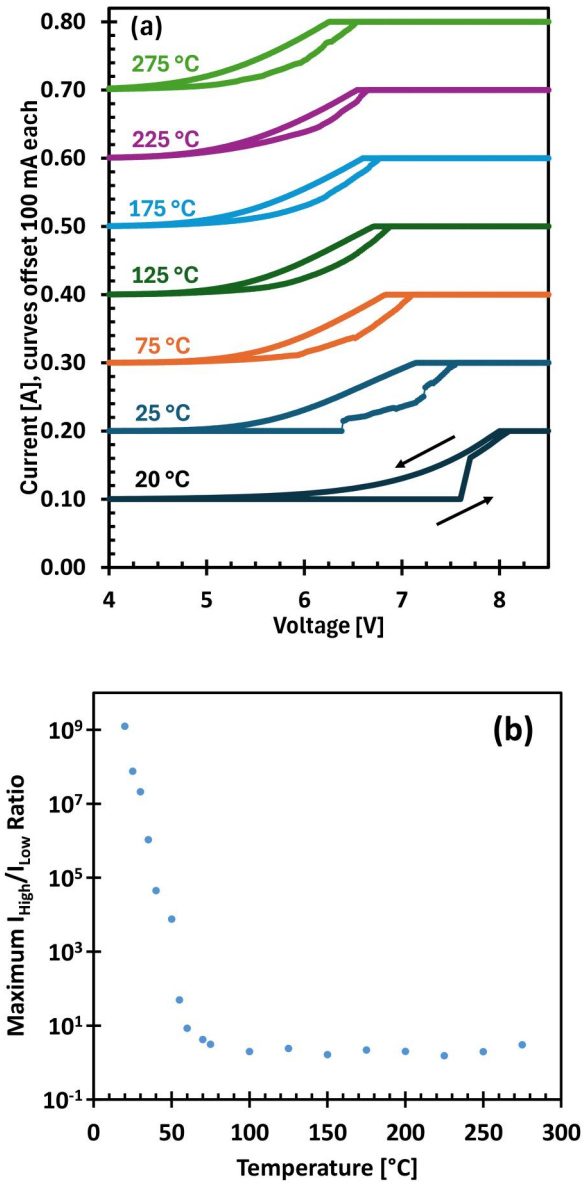

FIG. 2. (a) Quasi DC I–V curves for a subset of the range of temperatures studied. Since the memory window shrinks to about a factor of two at higher temperatures, the data are plotted on a linear scale such that the window is visible. (b) Maximum on/off ratios obtained as a function of temperature. The ratio was calculated between the up and down voltage sweeps, corresponding to high (I_{High}) and low (I_{Low}) resistance states. The voltage at maximum remained relatively constant at about 6 V. Note the extremely large memory window observed at ambient quickly degrades by many orders of magnitude and eventually saturates at about a factor of two by 75 °C. However, this factor of two memory window remains stable up to at least 275 °C.

switching cycles. See the supplementary section for the identical data plotted on a logarithmic scale. Note that in the first few cycles, after prolonged exposure to 0 V bias, the switching window (ratio of I_{High} and I_{Low}) is approximately 10^9, as shown in Fig. 2.

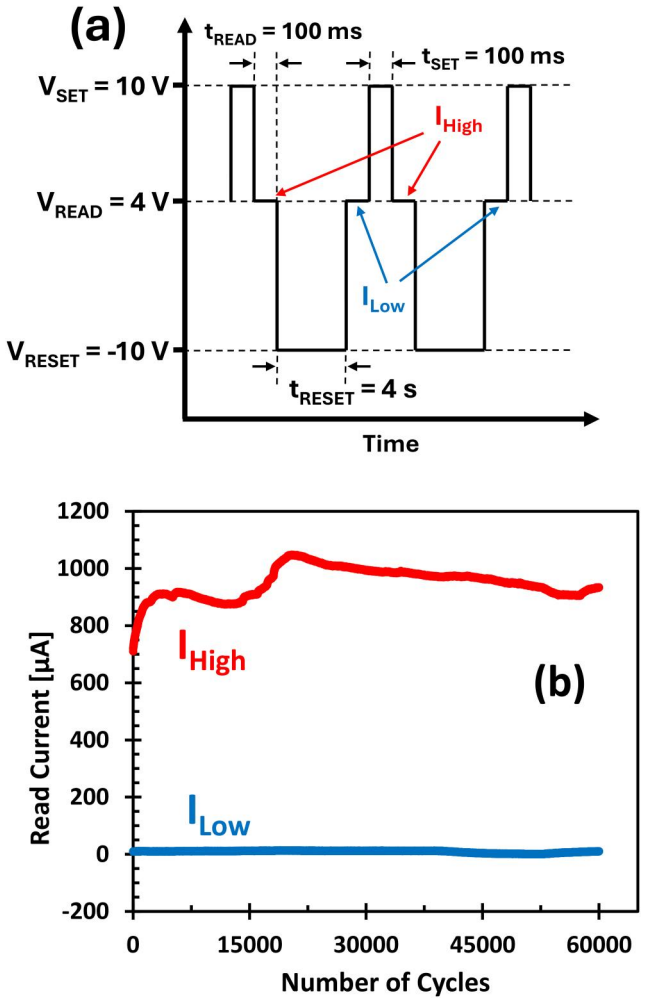

FIG. 3. (a) Schematic illustration of the waveform utilized to emulate operation of the device as a memory element. Here, the device is cycled between high and low resistance states, including an intermediary step to measure the actual resistance state. (b) Measured device response current response when subjected to the waveform of (a) through 60 000 cycles. While some stochastic variations exist, the memory window remains quite robust through at least 60 000 cycles.

In subsequent cycles, the window undergoes a rapid conditioning phase for the first few cycles, then saturates at roughly 10^2, and remains relatively stable throughout. While some stochastic variation exists over time, the memory endurance and retention characteristics are quite robust with no appreciable degradation, even after 60 000 cycles. We suspect this initial condition phase, in which the voltage window contracts from the initial 2–8 V, then stabilizes at 2–5.5 V for the remainder, and involves a rapid equilibrium process involving the complex interplay of the electrostatics governing the amount of fixed charge and the initial trapping/detrapping dynamics.

I–V curve hysteresis effects are often attributed to the trapping and detrapping of charge carriers at defect centers within the active region of the device. While the exact physical mechanisms and defect entities involved are often complex and difficult to identify, the basic

process involves trapped charge induced changes to the devices internal electrostatics, resulting in different electrical responses based on its history (resulting in a different I–V path during forward and reverse voltage sweeps). As discussed previously, the regrowth pn GaN epitaxial layers are known to incorporate silicon impurities[7–11] and likely explain the contrasting electrical behavior as seen by other groups.[14–17] The *in situ* growth of sample A pn layers, performed without breaking vacuum, is expected to result in a superior, cleaner interface. Indeed, SIMS analysis of the two samples (supplementary material) confirms this suspicion. The interface of sample B shows a clear spike in both silicon and carbon concentration, which is absent in sample A. Although SIMS cannot resolve the local atomic configuration at the interface, these results strongly suggest a defect-rich interfacial region, likely several nanometers thick. Given the lack of detectable oxygen, this region is unlikely to correspond to an oxide, such as SiO_x. Furthermore, EL analysis (supplementary material) reveals several additional spectral peaks in sample B compared to sample A, strongly indicating the presence of additional defect states.

To better understand the physical mechanisms behind the observed hysteresis, we developed a TCAD model that incorporates these defect-rich interfaces. We assume the effect is primarily due to nonidealities at the junction interface, such as the existence of a barrier layer and the movement of space charge. TCAD simulations were performed on ideal diodes as well as diodes with defective regions, with further details and step by step analysis provided in the supplementary material. Furthermore, the proposed mechanism was not assumed as *a priori* but was arrived at through a rigorous process using boundary conditions from our other measurements (physical/chemical information from SIMS and energy information from EL) and exclusions of alternative scenarios. Figure 4(a) illustrates the main results and the successful replication of the clean I–V curve of sample A and the large hysteresis effect observed in sample B. While these modeling efforts cannot be used to definitively identify the exact physical mechanisms and/or defects involved, they do provide a means to infer several key ingredients required, without which the hysteresis effect cannot be generated. As schematically illustrated in Fig. 4(b), they include: (1) an interfacial barrier between n and p layers. The thickness and bandgap of this layer are interrelated; a thinner barrier requires a larger bandgap and vice versa. (2) Fixed negative charge within the interfacial barrier. The amount and distribution of this fixed charge depend on the thickness and bandgap of the barrier. (3) Trapping and detrapping of positive charge within the p-GaN layer near the barrier. Again, the amount of charge depends on the spatial distribution. Our initial attempts to model the behavior using opposite polarity charge (i.e., fixed positive charge with trapping/detrapping of negative charge) were not able to successfully replicate the exceptionally large hysteresis in our samples. In these attempts, only much smaller shifts were possible. Furthermore, many alternative scenarios were attempted to reasonably replicate the observed data, including individual, paired, or other combinations of the above three elements, along with several other possibilities deemed either unlikely or nonphysical. Thus, our model should not be considered all encompassing, but rather reasonably possible and open to further improvements. Additionally, the model must only be viewed as qualitative since the exact details are quite complex involving many parameters, which are beyond our ability to measure at this time.

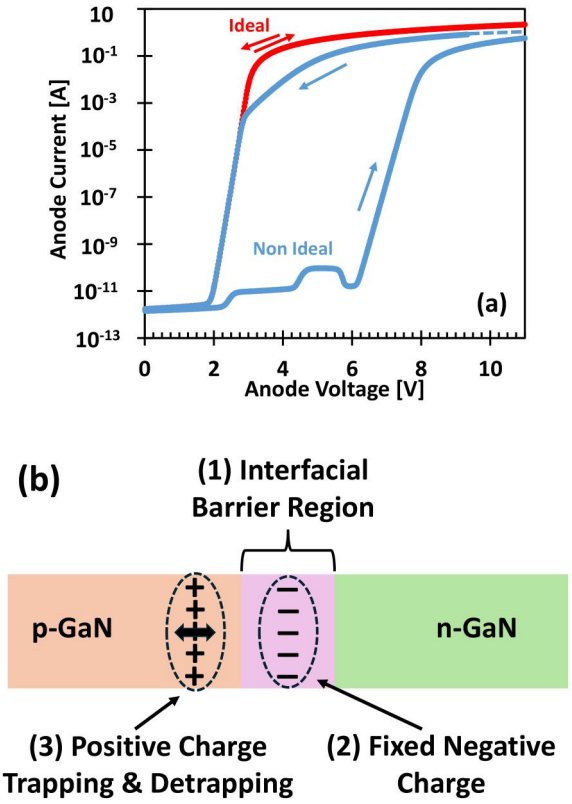

FIG. 4. (a) TCAD simulations that successfully recreate the ideal I–V response of sample A and the large hysteresis effect observed in sample B. The exact details involve an interplay between specific thicknesses, energy barriers, and charge concentrations and distributions; thus, these results only qualitatively recreate the experimental data. However, the three key ingredients necessary are an interfacial barrier, interfacial barrier fixed negative charge, and positive charge trapping/detrapping in the p-GaN layer, as illustrated in (b). See the supplementary section for further details.

While beyond the scope of this work, an exhaustive application-level characterization of this memory behavior would be very valuable and likely required prior to considering this effect as a truly viable memory device. This would include systematic mapping and optimization across a wide range of temperatures, including retention time analysis and algorithmic optimization of program, erase, and read/sense voltages (including their temporal functions) to maximize operating margins and minimize read-disturb effects. Additionally, since the devices used in this study were the result of GaN regrowth, further studies should include intentionally fabricated devices in which the processing conditions that lead to this behavior can be tightly controlled, and the material properties governing the trapping dynamics can be systematically tuned. Despite the absences of an in-depth evaluation of this GaN memory, the remarkably large and anecdotally stable memory window remains as the main motivation for this report. The observed memory window characteristics are so striking that we feel compelled to report these results with the hopes that they motivate future GaN memory or selector research.

In conclusion, we show that pn GaN vertical diodes fabricated with epitaxial regrowth exhibit a very large, robust, and repeatable

hysteresis window, a behavior absent in the *in situ* grown devices. We demonstrated that these devices provide a stable memory window with robust endurance characteristics, showing no degradation over 60 000 switching cycles. While the memory window quickly shrinks several orders of magnitude with elevated temperatures, the smaller window remains stable up to at least 275 °C. We attribute the effect to a defect-rich interface region created during the regrowth process, as evidenced by SIMS analysis showing increased silicon and carbon concentrations and by EL analysis revealing additional spectra peaks. Finally, our TCAD modeling successfully replicated the observed hysteresis, identifying a key combination of an interfacial barrier, fixed negative charge, and positive charge trapping as the key ingredients necessary for this memory-like behavior.

See the supplementary material for the SIMS and EL results for both samples, along with additional details of the TCAD simulations.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

S. J. Moxim: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **J. Comanescu:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **C. A. Voigt:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **O. Maimon:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **B. H. Hamadani:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **A. Winchester:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **E. Bittle:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **Q. Li:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **T. J. Anderson:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **J. K. Hite:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **A. Davydov:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **J. P. Campbell:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – review & editing (equal). **S. Pookpanratana:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Writing – original draft (equal); Writing – review & editing (equal). **J. T. Ryan:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Methodology (equal); Project administration (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

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