

# Development of Silicon Micromachined Waveguide Filter-Banks for On-Chip Spectrometers

Matthew A. Koc , Jason Austermann , James Beall , Johannes Hubmayr , Joel N. Ullom , Michael Vissers , and Jordan Wheeler 

**Abstract**—Development of high-speed, spatial-mapping spectrometers in the millimeter and far-infrared frequencies would enable entirely new research avenues in astronomy and cosmology. An “on-chip” spectrometer is one such technology that could enable Line Intensity Mapping. Recent work has shown the promise of high-speed imaging; however, a limiting factor is that many of these devices suffer from low optical efficiency. Here we present the fabrication of a metalized, Si waveguide filter-bank fabricated using deep reactive ion etching for use in millimeter spectroscopy. Our design simultaneously provides high-density pixel packing, high optical efficiency, high spectral resolution, and is readily compatible with simple and multiplexable MKID arrays. Gold plated test waveguide and filter show excellent match to simulations with a measured resolving power of 263 and a loss quality factor of 1116 at room temperature. The results show promise for extending the measurements to larger, multiwavelength designs.

**Index Terms**—Deep reactive ion etching, fabrication, filter-bank, waveguide.

## I. INTRODUCTION

THE (sub)millimeter radiation bands are rich with cosmological and astronomical information. One emerging technique that could probe over 80% of the volume of the observable universe is line intensity mapping (LIM) [1]. This technique images astrophysical emission lines as a function of redshift, which can provide deeper insight into areas of study such as dark matter and energy, inflation, and constraining  $\Lambda$  cold dark matter ( $\Lambda$ CDM) cosmology [2], [3], [4]. Each redshift bin provides a 2-D map of matter distribution. One major benefit of LIM is that it can simultaneously measure a large number of bands across a wide band of frequencies of interest, in contrast to current design for most cosmic microwave background (CMB) receivers having comparatively fewer bands within the same bandwidth [5], [6], [7].

Multiple (sub)millimeter on-chip spectrometers have been proposed for LIM, including grating spectrometers [8], [9],

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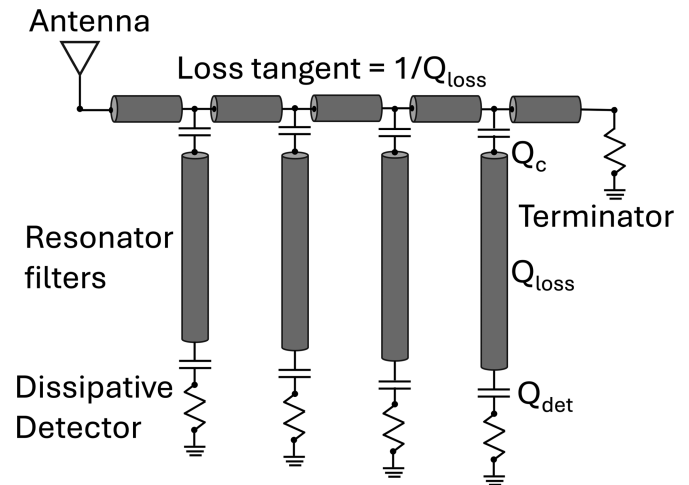


Fig. 1. Filter-bank operation principle. Signal is coupled into a transmission line via an antenna. The power is coupled to resonant filters and then each filter couples to a detector. The terminator absorbs any power not absorbed or reflected by the filters, preventing any standing waves on the main transmission line.

[10], Fourier transform spectrometers [11], [12], and Fabry–Perot interferometers [13], [14]. One promising technology for spectrally resolving (sub)millimeter light that has gained traction recently is the use of on-chip spectrometers using a filter-bank [15], [16], [17], [18], [19], [20], [21]. Filter-banks in the (sub)millimeter wavelength operate on the principles shown in Fig. 1. Light is coupled into the transmission line via an antenna. Light from the transmission line is then coupled to the spectral filters and then towards a detector with coupling strengths of  $Q_c$  and  $Q_{det}$ , respectively. The maximum power that can be delivered to the detector occurs when  $Q_c = Q_{det}$ . Multiple resonant filters can be added in series to separate the light based on the frequency, creating a filter-bank spectrometer. A single filter-bank spectrometer can fit within several  $\text{cm}^2$  of silicon, which approaches nearly an order of magnitude reduction in size compared to grating, Fourier transform, or Fabry–Perot spectrometers.

The maximum spectral efficiency of a filter-bank spectrometer,  $\eta = 50\%$ , is given by

$$\eta = \frac{1}{2} \left( 1 - \frac{R}{Q_{loss}} \right) \quad (1)$$

where  $Q_{loss}$  is the resonant quality factor describing any sources of loss in the filter-bank, and resolving power  $R$ , or quality factor

of the filter-bank, is defined as

$$\frac{1}{R} = \frac{1}{Q_c} + \frac{1}{Q_{\text{det}}} + \frac{1}{Q_{\text{loss}}}. \quad (2)$$

Here  $Q_c$  is the coupling quality factor between the feed-line and the filter and  $Q_{\text{det}}$  is the coupling quality factor between the filter and the detector [22]. These equations demonstrate the crucial need for low-loss (high  $Q_{\text{loss}}$ ) transmission lines as that parameter limits both the resolving power and the spectral channel efficiency. Although (sub)millimeter on-chip spectrometers have been under development for over a decade [23], [24], one major limitation has been the efficient transmission of photons from coupling optics to spectroscopic detection. The highest achieved optical efficiency reported is approximately a factor of 3 lower than theoretical maximum, indicating there is room for improvement in design and development [16], [17].

We propose a metalized, micromachined Si filter-bank waveguide designed in a split-block architecture. There is extensive work in micromachining waveguide components from silicon for low loss (sub)millimeter wavelength components [25], [26], [27]. Because the transmission media of the waveguide is vacuum, these waveguides represent the lowest potential loss of all materials; however, there is still the potential of loss through the side walls due to finite conductivity and surface roughness. Beuerle et al. demonstrated a decrease in loss along by reducing the waveguide by utilizing silicon-on-insulator (SOI) wafers and a polished silicon cap wafer to limit the roughness to just two of the four sides in an H-plane split; however, they required bonding the cap wafer to the waveguide to prevent extra radiative loss through the seams [27]. Likewise, an H-plane split-block waveguide has been used to demonstrate a micromachined filter at 1 THz [20]. In contrast to H-plane, split block E-plane waveguides minimize the loss due to reflections and radiative losses through gaps because the currents in the TE<sub>10</sub> mode do not cross the split plane, but these are prone to misalignment issues. The inclusion of a vernier scale on for alignment of E-plane waveguides was shown to allow alignment within 1  $\mu\text{m}$  [26].

Prior work in the development of WSPEC used direct machining of metal blocks to produce a filter-bank spectrometer with a split-block architecture [19], [28]. Direct machining tolerances of metals are often limited to  $\gg 1 \mu\text{m}$ , with greater tolerances often costing more to machine, whereas optical lithography readily achieves sub- $\mu\text{m}$  tolerance [28]. For the frequencies and resolution tested here we require  $\sim 4 \mu\text{m}$  tolerance, which is easily achieved with optical lithography. Optical lithography has greater accuracy and precision of absolute location of features, which also more readily allows for the E-plane split and matching of two parts than two disparate direct machined parts. A further benefit to silicon micromachining is that it is suitable for batch fabrication, leading to greater scalability compared to the serial nature of direct machining [26].

## II. METHODS

### A. Design

Here we present a single-channel waveguide filter-bank as a proof of concept demonstration. The waveguide architecture

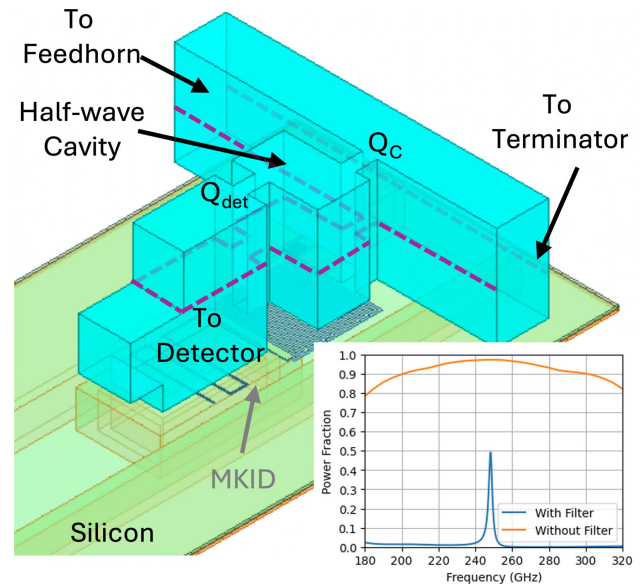


Fig. 2. 3-D realization of a single channel filter-bank as a high-frequency structure simulator (HFSS, Ansys, see Notes) model. The waveguide transmission line couples to a half-wave resonant filter, which in turn couples to a waveguide with an H-plane bend terminating into an MKID on a separate wafer. The location of the split plane is indicated by the dashed line. The inset shows the detector response with and without the filter. With the filter nearly perfect, 50% coupling can be achieved. This detector is on a 10  $\mu\text{m}$  SOI membrane with a separate deep-etched metalized wafer serving as a quarter-wave backshort.

shown in Fig. 2 can achieve a theoretical maximum  $\eta = 50\%$  for a single filter when  $Q_c = Q_{\text{det}}$ , based on standard transmission line circuit analysis. While in this architecture, a single channel is limited to 50% efficiency the total efficiency of a spectrometer can be increased to 90% or more by oversampling (placing channels with significant overlap in their spectral profiles) [23]. The half-wavelength waveguide cavity acts as the resonant filter, while the coupling strengths  $Q_c$  and  $Q_{\text{det}}$  are controlled by slots. An H-plane 90° bend brings the waveguide channel outputs to a detector. To realize this geometry, we create an E-plane split block waveguide by micromachining mirrored parts, as shown in Fig. 3(a). Images of a functioning, realized single-channel filter-bank are shown in Fig. 3(c) and (d). In the range of 200 to 300 GHz at  $R = 100$ , we need a tolerance of  $\sim 4 \mu\text{m}$ , which is readily achievable with optical lithography.

### B. Fabrication

Micromachined parts were fabricated using a 150-mm SOI wafer with a 430- $\mu\text{m}$  handle thickness, 0.5- $\mu\text{m}$  oxide thickness, and 220  $\mu\text{m}$  device side thickness. SOI wafers were used to ensure a consistent etch depth across the entire wafer. The test device was etched in three steps: primary alignment marks, back side deep etch, and front side deep etch. The resulting micromachined parts were aggressively cleaned to remove any residual etch byproduct on the side walls and were then metallized. All lithography was performed using direct-write photolithography.

1) *Primary Alignment Marks*: Alignment marks were lithographically placed in regions that would not affect the waveguide properties. Alignment marks were patterned into SPR 660 photoresist (Dow, see Notes) on the device-side layer. Marks were

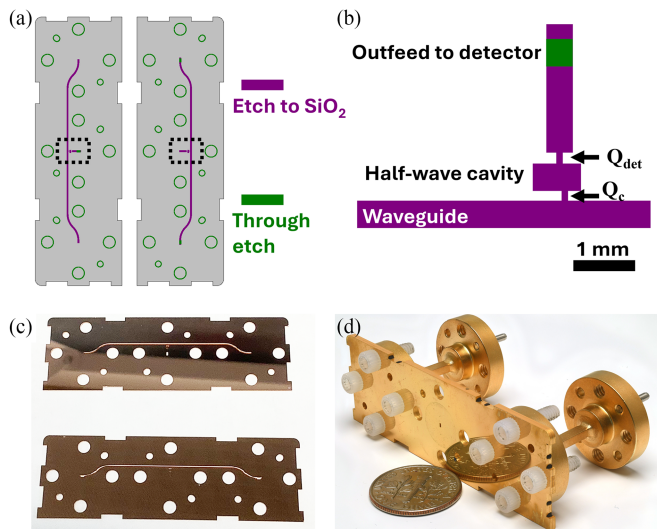


Fig. 3. Designed and fabricated test parts of a single filter waveguide test part. (a) Shows the full split-block design where the purple traces show an etch that stops on the  $\text{SiO}_2$  layer and the green is etched completely through the wafer. Each part of the split-block is almost a perfect mirror, but the feedhorn, terminator, and detector ports are not symmetric between the two halves. The black, dashed square box shows the filter bank that is seen in (b) and the 3-D render shown in Fig 2. The etched portion of the device outside of the box is the waveguide. (b) Shows the general shape of the filter. The wavelength is determined by the length of the half-wave cavity and quality factors are set by the position and width of the coupling slots. (c) Shows the fabricated device after an initial Ti/Cu seed layer. (d) Shows the assembled, Au-plated waveguide with attached commercial VNA coupling parts.

etched with a  $\text{SF}_6$  plasma etch process in a Deep Reactive Ion Etcher (DRIE) resulting in  $\sim 1 \mu\text{m}$  etch depth.

2) *Back Side Deep Etch*: The back side deep etch was patterned onto the handle side of the wafer with SPR 220-7 photoresist (Dow, see Notes) spun at approximately  $7 \mu\text{m}$  thickness. The primary alignment marks on the opposite side of this pattern were used to align the pattern in the maskless aligner. The back side deep etch pattern includes all features intended to be etched completely through the wafer, such as the perimeter, screw holes, and entrance/exit ports for coupling light into/out of the waveguide spectrometer.

The features were etched down  $430 \mu\text{m}$  to the oxide layer with a DRIE using a modified Bosch etching process in an SPTS Rapier (see Notes). Briefly, the etch process involved three steps which were looped sequentially until the etch depth was reached. First a  $\text{C}_4\text{F}_8$  plasma was used to deposit an isotropic, passivating  $\text{CF}_x$  film to protect the side walls and cover the exposed Si, followed by a directional  $\text{O}_2$  etch to clear the bottom passivation film, finally followed by an isotropic  $\text{SF}_6$  etch to rapidly remove exposed Si. The platen temperature was set to  $0^\circ\text{C}$  for this process. The endpoint of the etch was monitored by an optical endpoint detector which followed the intensity of the Si-F optical emission line at  $440 \text{ nm}$  [29]. The  $\text{SiO}_2$  layer is only weakly reactive using this process, so it acts as an etch stop, allowing for a uniform etch depth across the wafer. Once the  $\text{SiO}_2$  layer is exposed, the concentration of  $\text{SiF}_4$  in the plasma decreases which can easily be measured in the optical emission spectrum. After visual confirmation of completely etching to the oxide

layer across the entire device, the oxide is removed using a low power  $\text{CF}_4/\text{O}_2$  reactive ion etch.

3) *Front Side Deep Etch*: The etched back side of the wafer was laminated with roll-on negative photoresist with a BoPET backing to protect the electrostatic chuck in the DRIE once the wafer was etched through. The front side was patterned with  $\sim 7 \mu\text{m}$  photoresist as described in the back side deep etch. The features were etched using the same Bosch process on the DRIE and the etch was monitored with the optical emission end point detector as described above. This step etches the waveguide and filter-bank features at a depth of  $220 \mu\text{m}$ , due to the device-side thickness. It also simultaneously etches through the remaining silicon on the through-etch portions, such as the device perimeter and screw holes. Accurately stopping the etch once the endpoint is reached is critical, because etching longer can result in more severe undercut, altering the frequency set by the dimensions of the half-wavelength cavity. The  $0.5 \mu\text{m}$  oxide layer in the waveguide and filter-bank features was cleared using the  $\text{CF}_4/\text{O}_2$  reactive ion etch described above.

### C. Preparation for Metallization

The etch byproduct on the sidewalls from deep etching is notorious for preventing conformal metallization [30], [31]. To address this, each part was cleaned through an aggressive cleaning process. Photoresist was removed by soaking in a bath of acetone for 3 min, sonicating in a clean bath of acetone for 3 min, then rinsing in a bath of IPA for 3 min. The parts were allowed to dry overnight. Samples were then cleaned in  $75^\circ\text{C}$  Nano-strip (FUJIFILM Electronic Materials, see Notes) for 15 min, then were rinsed in a quick dump rinse (QDR) tank with DI water for 20 cycles. The parts were then cleaned in a bath of  $55^\circ\text{C}$  Novex7200 (3M, see Notes) for 15 min and a bath of  $70^\circ\text{C}$  PlasmaSolv EKC265 (DuPont, see Notes) for 15 min. Residual EKC 265 was removed from the parts with 2 baths of IPA for 3 min, 20 cycles of QDR, then a final bath of IPA for 3 min. Parts were allowed to air dry undisturbed overnight. Although an HF dip to remove native oxide from the silicon surface can improve metal adhesion, prior work in this group on silicon micromachined devices has demonstrated that this step was not needed for good metal adhesion [30], [31].

### D. Metallization and Assembly

Multiple, different metallization methods were attempted; however, only electroplating with Cu and Au yielded a functional device. The Au plating was performed in a two step process at external vendors. A seed layer was performed at LGA Thin Films, Inc. (Santa Clara, CA, USA, see Notes), where parts underwent an in situ sputter clean followed by  $200 \text{ nm}$  Ti topped with  $1 \mu\text{m}$  of Cu at high pressure. Parts were then electroplated at Custom Microwave Inc. (Longmont, CO, USA, see Notes) resulting in  $3 \mu\text{m}$  of electroplated Cu followed by  $3 \mu\text{m}$  of Au.

Test devices were also coated with sputtered Al in-house. Cleaned Si parts were mounted to a carrier wafer. Al was deposited via sputtering in an Ar plasma with the carrier wafer cooled to  $25^\circ\text{C}$  and rotated at  $40 \text{ r/min}$  to ensure a uniform

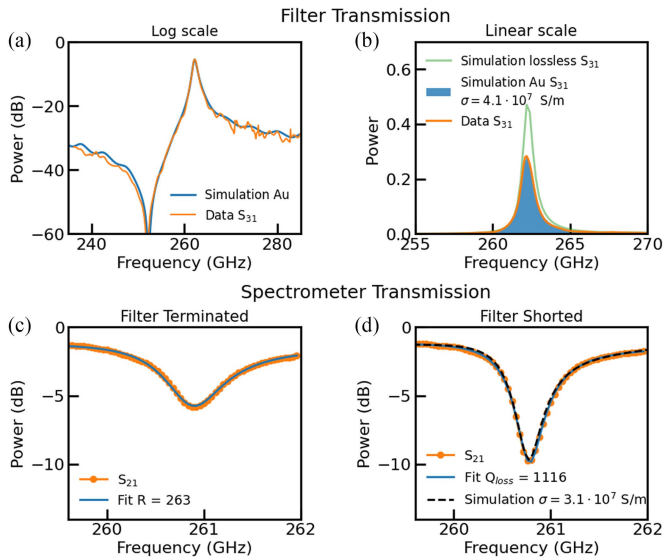


Fig. 4. Experimental and simulated results for the Au-plated waveguide filter in the log (a) and linear (b) scales. The Au-plated simulation of the design (blue,  $\sigma = 4.1 \times 10^7$  S/m) matches the measured data (orange). It should be noted that since  $Q_{\text{det}} < Q_{\text{loss}}$ ,  $Q_{\text{loss}}$  is not well constrained by a measurement of  $S_{31}$ . The lossless waveguide was simulated (green) to show a maximum possible efficiency for a single isolated channel with this design. (c) Measured power loss of the filter when it is terminated resulting in a fit of  $R = 263$ . (d) Measured power loss when the filter is shorted (effectively setting  $Q_{\text{det}} \gg Q_{\text{loss}}$ ), resulting in a fit of  $Q_{\text{loss}} = 1116$ . This  $Q_{\text{loss}}$  is consistent with a reduced conductivity from nominal gold at  $\sigma = 4.1 \times 10^7$  S/m to  $\sigma = 3.1 \times 10^7$  S/m. The reduced conductivity may be due to surface roughness.

coating. Multiple deposition times were tested from 20 to 40 min per side.

The two mirrored parts were assembled on granite blocks, aligned with vernier marks [26] to within  $2 \mu\text{m}$  on all four edges. Multiple screws with Teflon washers were used to temporarily clamp the parts together while STYCAST 2850FT (Henkel Loctite, see Notes) was applied along the edges to permanently hold the parts together.

### III. RESULTS AND DISCUSSION

A single-channel (260 GHz) Au-plated waveguide filter-bank was fabricated and tested at room temperature using a mm-wave vector network analyzer (VNA). The VNA experimental setup has been previously presented [30]. Commercial VNA adapter components were used to test the design measuring the transmitted frequency through the filter and the spectrometer as seen in Fig. 4. The data show a good match to HFSS (Ansys, see Notes) simulation of Au-plated waveguide with a slight shift (0.5%) in frequency. We measure a filter efficiency of nearly 30%, which matches the Au simulation. We find that  $S_{11}$  is less than  $-10$  dB, indicating that the H-plane  $90^\circ$  bend does not have a significant reflection. The resolving power is fit to be  $R = 263$  (designed  $\sim 300$ ), as shown in Fig. 4(c).

By terminating and shorting the filter output with commercial components (effectively setting  $Q_{\text{det}} \gg Q_{\text{loss}}$ ) and measuring the transmitted power through the output of the spectrometer, we determine  $Q_{\text{loss}} = 1116$ , as shown in Fig. 4(d). We can calculate our maximum spectral efficiency based on (1) to be  $\eta = 0.384$  at

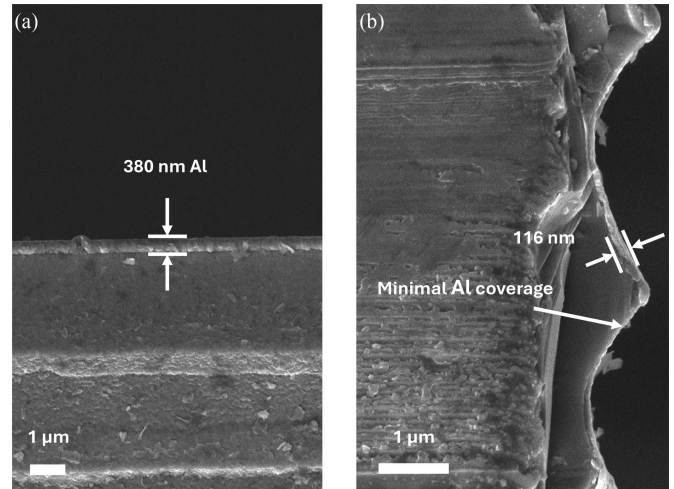


Fig. 5. SEM images of DRIE etched waveguide parts, sputtered with Al. (a) For a process that results in 380 nm of Al deposited on the top surface (b) only a fraction can coat the side walls within the etch cavity. The curved “scallops” on the sidewalls are caused by the Bosch etching process used to deep etch the silicon. The upward facing surface of the scallop has  $\sim 100$  nm of Al while the downward, shadowed surface has minimal Al coverage. Resultant devices metallized in this manner showed excessive loss.

room temperature. Because the  $Q_{\text{loss}}$  can improve as the square root of the residual-resistance ratio (RRR), it is reasonable that a significant improvement in loss can be achieved upon cooling. However, the anomalous skin effect will limit the high-frequency loss reduction when compared to the dc loss dictated by RRR alone [32], [33]. With a modest RRR of 5, we might expect a  $2\times$  improvement in  $Q_{\text{loss}}$ , reaching 2200. For  $\text{RRR} > 5$ , the anomalous skin effect will dominate the high-frequency loss, and further improvements to  $Q_{\text{loss}}$  will be minimal and likely not exceed  $3\times$  improvement. A factor of a few improvement is roughly consistent with the measured cryogenic loss of a gold-plated orthomode transducer at 450 GHz [34].

Waveguides metallized using only sputtered metal resulted in extremely lossy waveguides. Because the Bosch etching process results in a sidewall that is scalloped, even with a high-pressure sputter, the underside of the scallop is shadowed and little-to no metal is adhered, as seen in Fig. 5, resulting in a waveguide with lossy sidewalls. Thus, the need for mass transport within the cavities during the metallization step is indicated and has been addressed by electroplating. Lossy waveguides were observed with multiple conditions of in-house Al sputtering as well as parts with the Ti/Cu sputtered seed layer performed by the external vendor.

Given the achieved  $Q_{\text{loss}}$  in excess of 1000 it is reasonable to build spectrometers with resolving powers of 100 or less without further development to improve loss. As such, the simulated performance of a full spectrometer is shown in Fig. 6. The spectrometer is composed of 80 channels with  $R = 100$  and a bandwidth of 1.5. The overall dimension of the filter-bank is  $5 \times 50 \text{ mm}^2$ , so an array of 20 of these filter-banks could easily be fabricated using a single 150 mm SOI wafer and coupled to a single monolithic 1600 detector MKID array. This spectrometer card could then be oriented in the z-direction of

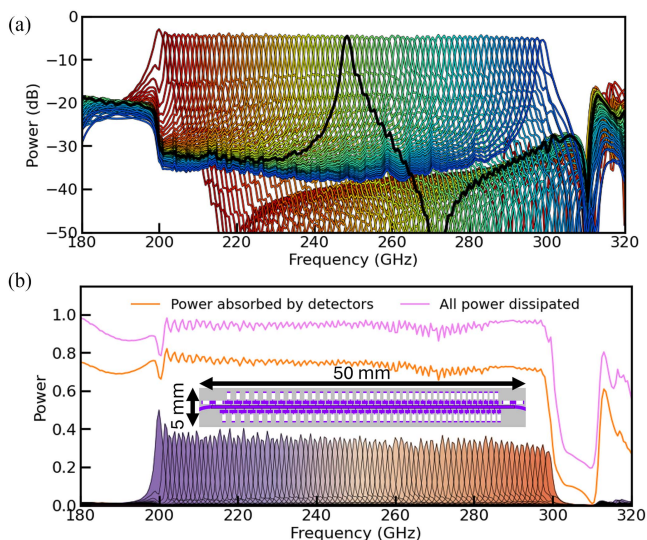


Fig. 6. Simulation of a full filter-bank spectrometer. The simulation is made via cascading all of the S matrices of individual filters together and each filter to a detector simulation S matrix. A filter-bank was designed with 80,  $R = 100$  channels with 1.5 bandwidth. (a) Shows the spectrometer performance for each individual filter using a log scale. One specific filter is highlighted (black) to show the general shape of each filter. Out of band coupling within the spectrometer operation range of 200 to 300 GHz is less than 30 dB. (b) Shows filter response in linear scale and also the cumulative power absorbed by the detectors (orange) and the total dissipated power (purple). The difference between the orange and purple curves is due to dissipation from  $Q_{\text{loss}}$ . The inset shows a schematic of the spectrometer size.

a sub-millimeter focal plane so that it only occupies  $5 \times 100$  mm<sup>2</sup> of focal plane real estate. A stack of 20 spectrometer cards would make a 400-pixel, 32 000 detector spectrometer with a focal plane footprint of only  $\sim 100 \times 100$  mm<sup>2</sup>. In this geometry, light would need to be coupled into the device with a specialized feedhorn, compared to the commercial adapters used for the prototype presented here. This spectrometer is designed to efficiently transmit light in the range of 200 to 300 GHz, which would be capable of measuring the CO and CII emission lines [2]. Presuming a similar filter-efficiency to the single-filter that we measured, we expect  $\sim 74\%$  device-efficiency across the band. For comparison, a nearly lossless filter-bank could result in up to 90% device-efficiency across the frequency range.

#### IV. CONCLUSION

The Au-plated, single filter results demonstrate one of the highest reported filter efficiencies to date. This technology is highly scalable and will enable accurate spectroscopic measurements with high-spatial mapping speeds. By utilizing an E-plane split-block construction we can minimize any losses due to gaps in assembly, resulting in a highly efficient spectrometer. A further increase in efficiency should be possible by metallizing with a superconducting metal, such as Nb or TiN. We were unsuccessful in complete sidewall coverage when exclusively using sputtering as the technique for metallization and require a method such as high-pressure seed layer sputtering or atomic layer deposition followed by electroplating to ensure complete coverage.

#### NOTES

Products or companies named here are cited only in the interest of complete technical description, and neither constitute nor imply endorsement by NIST or by the US government. Other products and companies may be found to serve just as well.

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