IEEE Open Journal of
Ultrasonics, Ferroelectrics, and Frequency Control

Received 22 August 2025; revised 30 December 2025; accepted 4 March 2026. Date of publication 9 March 2026; date of current version 17 March 2026.

Digital Object Identifier 10.1109/OJUFFC.2026.3672064

Flicker Suppressed Direct Digital Phase and Amplitude Noise Measurements

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This work was supported by the National Institute of Standards and Technology (NIST).

ABSTRACT In this article, we present a new and innovative technique that reduces the close-to-the-carrier noise floors in direct digital measurement systems. For a 100 MHz carrier, with respect to our previous state-of-the-art direct digital measurement system, we report a noise floor reduction of over 35 dB in the flicker region for both phase and amplitude noise, and greater than a factor of 20 improvement in Allan deviation. Moreover, this technique reduces the impact of analog-to-digital converter's voltage reference noise and aperture jitter on the system noise floor, allowing the construction of multichannel systems for timescale applications while maintaining the same performance levels. We call this new method flicker-suppressed direct digital. At 100 MHz for a single channel, we report single sideband residual phase noise floor of $\mathscr{L}(1\text{Hz}) = -147\text{dBc/Hz}$, with a flicker corner of about 0.03 Hz. The single channel residual Allan deviation noise floor for the same carrier is less than 1.3×10^{-16} at 1 second averaging time (τ) with a 0.5 Hz bandwidth. Further improvement can be achieved with the use of cross-correlation techniques. To our knowledge, this represents the lowest flicker noise and Allan deviation performance ever reported for a digital measurement system.

INDEX TERMS Allan deviation, amplitude noise, analog-to-digital converter (ADC), cross correlation, digital down conversion, direct digital measurement, field programmable gate array (FPGA), flicker noise, phase noise.

I. INTRODUCTION

MEASURING phase and amplitude noise of local oscillators and two-port devices is often critical for many applications such as telecommunication [1], [2] and radar [3]. Since their first commercial introduction, direct digital techniques [4], have been widely used in time and frequency metrology offering numerous advantages. These include the ability to utilize asynchronous reference (REF) and device under test (DUT) frequencies, eliminating the need for phase-locking, simplified near-to-the-carrier measurements, simultaneous phase and amplitude noise detection, and Allan deviation measurement, all without the need for sensitivity calibration [4], [5], [6], [7], [8].

State-of-the-art performance is achieved using 2-input high-performance analog-to-digital converters (ADC) [9] to suppress common noise sources such as aperture jitter and the voltage reference. In multi-input applications, such as timescales, the performance could be degraded due to the limited common mode noise suppression between ADCs distributed over independent devices. During Allan deviation measurements, low measurement bandwidths (BW) are generally used, meaning that the measurement system's noise floor is often limited by residual flicker-phase noise in the ADCs. To overcome these noise floor limitations, the most commonly used technique in commercial instruments is cross-correlation averaging [8], [9], [10]. However, when ultra-low noise devices or the best optical atomic clocks are measured, it could take days of cross-correlation averaging to achieve the necessary close-to-the-carrier noise floor. Moreover, when using cross-correlation, noise floor improves as the square root of averaging time, and because of limitations in channel isolation and practical measurement time, enhancements over an order of magnitude are hardly achieved in Allan deviation.

For a previously designed measurement system [9], we demonstrated a state-of-the-art single channel 10 MHz

single sideband noise floor performance of $\mathscr{L}(1\text{Hz}) = -143\text{dBc/Hz}$, and a residual single channel frequency stability of 3.2×10^{-15} @ $\tau = 1$ s. Since then, we constructed a new multichannel system based on a similar architecture, incorporating a newly developed and innovative technique that we call "flicker suppressed direct digital" (FSDD) [11]. This technique significantly reduces the residual flicker noise floor and delivers consistent results for differential measurements, whether they are taken between inputs on the same dual ADC or across distributed ADCs, a highly desirable feature for multichannel measurement systems. For 100 MHz carriers, the residual single-channel phase noise floor without FSDD is $\mathscr{L}(1\text{Hz}) = -124\text{dBc/Hz}$ when the 2 inputs on the same ADC are used, and $\mathscr{L}(1\text{Hz}) = -111\text{dBc/Hz}$ when inputs from different ADCs are utilized. In both cases, the single channel noise floor is flicker phase noise limited. On the other hand, when FSDD is implemented, we observe over 35 dB lower residual flicker with the measurement being mostly white noise limited for both phase and amplitude noise. For the same 100 MHz carriers, single channel Allan deviation residual noise demonstrates more than a factor of 20 improvement when FSDD is used. These already record-breaking results can be further improved with the use of cross-spectrum and cross-variance [10] techniques, bringing the instrument noise floor to the low 10^{-17} @ $\tau = 1$ or better. In a live timescale application, where cross-correlation cannot be used, FSDD theoretically supports some of the best optical atomic clocks after converting their outputs into the RF domain [12], [13].

II. FLICKER SUPPRESSED DIRECT DIGITAL

Figure 1 shows a block diagram of a single-channel FSDD noise measurement system. The most intuitive way to understand this new technique is by superposition: if the red blocks in Figure 1 are removed, the system performs a conventional direct digital measurement of DUT and REF as already discussed in our previous work [9], which will also include the system noise floor. On the other hand, if DUT and REF are removed, the correction signal (CORR) performs a residual system noise floor measurement. Because both measurements, conventional and residual using CORR, are performed simultaneously and share the same noise floor, by subtracting their measured phase fluctuations the noise floor is effectively reduced, particularly in the flicker noise region. This explanation is an over-simplification, and a rigorous analysis must be performed.

Figure 2 shows the ADC model used. The ADC core is assumed ideal, and quantization noise is not considered or assumed negligible. Three main noise sources for each ADC are indicated as follows:

- A buffer at the clock port.
- A voltage reference.
- A buffer at the input port.

Both white and flicker noise of the clock buffer will introduce aperture jitter φ_{A_xJ} for the specific ADCx, and it will be by definition a time modulation (x(t) type of noise). This aperture jitter will scale between the DUT carrier and CORR carrier as their frequency ratio. On the other hand, the voltage reference will introduce amplitude noise for a particular ADCx, and since its fluctuations will change the ADC core's gain, it can be defined as α_{A_xR}. Finally, the residual noise of the input buffer has been divided in two components: flicker and white for both phase and amplitude. The white noise components $\varphi_{A_xW_y}$ and $\alpha_{A_xW_y}$ will be independent for each ADCx and carrier y, while the flicker components φ_{A_xF} and α_{A_xF} will be independent for each ADCx, but the same for each carrier y. Flicker noise is a near-DC process, and because of non-linearities in a device, flicker is up-converted when a carrier goes through an active device [14]. Therefore, since the source of flicker noise is common, when two or more carriers go through the same device simultaneously, they will experience the same flicker modulation [15]. Up-converted flicker noise ideally does not scale with carrier frequency or power [14], suggesting that φ_{A_xF} is a phase modulation ($\varphi(t)$ type of noise). Similar reasoning can be applied for amplitude noise, and therefore α_{A_xF} will be the same for all carriers going through a particular device simultaneously.

DUT and CORR signals are sampled through ADC0. In the digital domain, two digital down converters (DDC) extract the phase and amplitude noise for the DUT carrier (ν_D) and for the CORR carrier (ν_S). The DDCs are described in detail in our previous work [9]. The DDC dedicated to the DUT will measure:

$$\text{DDC}_{\nu_D} = \begin{pmatrix} \varphi_D - \dfrac{\nu_D}{\nu_C}\varphi_C + \varphi_{A_0F} + \varphi_{A_0W_D} + \varphi_{A_0J} \\ A_D\left(1 + \alpha_D + \alpha_{A_0F} + \alpha_{A_0W_D} + \alpha_{A_0R}\right) \end{pmatrix} \tag{1}$$

while the second DDC for ν_S will generate instead:

$$\text{DDC0}_{\nu_S} = \begin{pmatrix} \varphi_S - \dfrac{\nu_D}{\nu_C}\varphi_C + \varphi_{A_0F} + \varphi_{A_0W_S} + \dfrac{\nu_S}{\nu_D}\varphi_{A_0J} \\ A_S\left(1 + \alpha_S + \alpha_{A_0F} + \alpha_{A_0W_S} + \alpha_{A_0R}\right) \end{pmatrix} \tag{2}$$

The top and bottom rows of the matrices contain the phase and amplitude noise terms, respectively. φ_D and φ_S are the DUT and CORR phase noise respectively, and φ_C is the ADC clock's phase noise instead. ν_C is the ADC clock frequency. For the amplitude noise case, A_D and A_S are the amplitudes of the DUT and CORR carriers respectively, while α_D and α_S their amplitude index fluctuations.

By scaling and subtracting equations (1) and (2), we see the first effects of FSDD

$$\begin{aligned} &\begin{pmatrix} 1 \\ \dfrac{1}{A_D} \end{pmatrix} \odot \text{DDC}_{\nu_D} - \begin{pmatrix} \dfrac{\nu_D}{\nu_S} \\ \dfrac{1}{A_S} \end{pmatrix} \odot \text{DDC0}_{\nu_S} \\ &= \begin{pmatrix} \varphi_D - \dfrac{\nu_D}{\nu_S}\varphi_S + \left(1 - \dfrac{\nu_D}{\nu_S}\right)\varphi_{A_0F} + \varphi_{A_0W_D} - \dfrac{\nu_D}{\nu_S}\varphi_{A_0W_S} \\ \alpha_D - \alpha_S + \alpha_{A_0W_D} - \alpha_{A_0W_S} \end{pmatrix} \end{aligned} \tag{3}$$

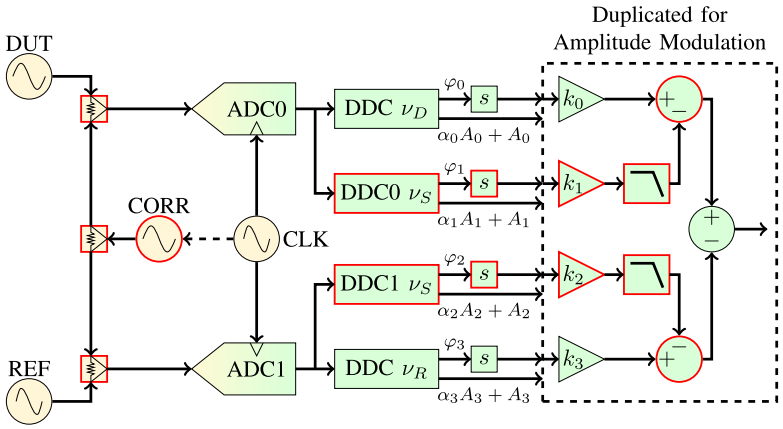

FIGURE 1. Simplified single-channel block diagram implementing the flicker suppressed direct digital (FSDD) technique. The correction signal (CORR) is injected into the DUT and REF paths. For ADC0 two DDCs extract DUT and CORR phase fluctuations, whereas for ADC1 two DDCs extract REF and CORR phase fluctuations. The phase noise information is then scaled and subtracted. The red border shows the additional components over the conventional direct-digital technique. The correction signal can be an independent source, or a scaled frequency of the ADC clock such as a frequency divider, a DDS, or a programmable PLL. The symbol *s* denotes differentiation, and the scaling constants k_x are described in equation 5.

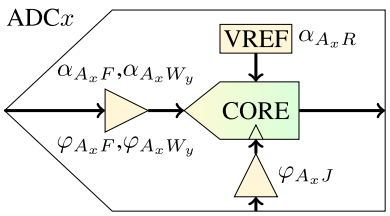

FIGURE 2. Model of the ADC noise. The ADC core is assumed to be ideal, while a clock buffer adds aperture jitter ($\varphi_{A_x J}$), the voltage reference adds amplitude noise ($\alpha_{A_x R}$), and the ADC input buffer adds flicker ($\varphi_{A_x F}$, $\alpha_{A_x F}$) and white ($\varphi_{A_x W_y}$, $\alpha_{A_x W_y}$) noise components for both phase and amplitude cases.

The symbol $\odot$ designates the element-wise product. From equation (3) one can see that the DUT is measured against CORR, the aperture jitter and ADC clock phase noise cancels, and the input buffer flicker reduces and has a suppression factor which depends on the DUT to CORR frequency ratio. On the other hand, for amplitude noise, input buffer flicker and voltage reference noise simplifies.

Similarly, for the REF path:

$$\begin{pmatrix} 1 \\ \frac{1}{A_R} \end{pmatrix} \odot \mathrm{DDC}_{\nu_R} - \begin{pmatrix} \frac{\nu_R}{\nu_S} \\ \frac{1}{A_S} \end{pmatrix} \odot \mathrm{DDC1}_{\nu_S} = \begin{pmatrix} \varphi_R - \frac{\nu_R}{\nu_S}\varphi_S + \left(1 - \frac{\nu_R}{\nu_S}\right)\varphi_{A_1 F} + \varphi_{A_1 W_R} - \frac{\nu_R}{\nu_S}\varphi_{A_1 W_S} \\ \alpha_R - \alpha_S + \alpha_{A_1 W_R} - \alpha_{A_1 W_S} \end{pmatrix} \tag{4}$$

where φ_R and α_R are the REF phase and amplitude noise respectively. A_R is the REF signal amplitude.

Finally, equation (4) can be scaled by the DUT to REF frequency ratio and subtracted from equation (3). The final result is then (5), as shown at the bottom of the page.

The DUT is now measured against the scaled REF as expected. In contrast to the traditional direct-digital technique, ADC aperture jitter now is removed and the flicker-phase noise from both ADCs are suppressed, however, additional new white noise components are present. The final measurement equations do not contain terms from the phase and amplitude noise introduced by the correction

$$\begin{pmatrix} 1 \\ \frac{1}{A_D} \end{pmatrix} \odot \mathrm{DDC}_{\nu_D} - \begin{pmatrix} \frac{\nu_D}{\nu_S} \\ \frac{1}{A_S} \end{pmatrix} \odot \mathrm{DDC0}_{\nu_S} - \begin{pmatrix} \frac{\nu_D}{\nu_R} \\ \frac{1}{A_R} \end{pmatrix} \odot \mathrm{DDC}_{\nu_R} + \begin{pmatrix} \frac{\nu_D}{\nu_S} \\ \frac{1}{A_S} \end{pmatrix} \odot \mathrm{DDC1}_{\nu_S} = \begin{pmatrix} \varphi_D - \frac{\nu_D}{\nu_R}\varphi_R + \left(1 - \frac{\nu_D}{\nu_S}\right)\varphi_{A_0 F} - \left(\frac{\nu_D}{\nu_R} - \frac{\nu_D}{\nu_S}\right)\varphi_{A_1 F} + \varphi_{A_0 W_D} - \frac{\nu_D}{\nu_S}\varphi_{A_0 W_S} - \frac{\nu_D}{\nu_R}\varphi_{A_1 W_R} + \frac{\nu_D}{\nu_S}\varphi_{A_1 W_S} \\ \alpha_D - \alpha_R + \alpha_{A_0 W_D} - \alpha_{A_0 W_S} - \alpha_{A_1 W_R} + \alpha_{A_1 W_S} \end{pmatrix} \tag{5}$$

signal, clock aperture jitter or clock phase noise. The amount of ADC flicker reduction and white noise degradation can be controlled with the frequency ratio between DUT, REF and the correction signal.

From a practical point of view, white noise is further deteriorated by the limited ADC dynamic range. In fact, if the available dynamic range is split in half to accommodate the correction signal, we expect 6 dB higher ADC residual white noise in both phase and amplitude noise. Power levels for DUT, REF, and CORR, and ν_S can be optimized to maximize flicker suppression, or to limit white noise degradation.

To recover some white noise performance at high-frequency offsets, Figure 1 shows two digital low-pass filters for the ν_S paths. These filters, however, will compromise aperture jitter and voltage reference noise suppression above their cut-off frequency.

The CORR frequency must be different enough from DUT and REF to not compromise the measurement with a specific bandwidth, and analog filters might be needed to prevent the CORR's phase and amplitude noise sidebands from overlapping with the DUT and REF noise sidebands, and vice versa. Aliasing caused by the sampling must also be considered when utilizing more than one Nyquist region.

Finally, to avoid the necessity of requiring an additional source for the correction signal, it could be conveniently derived from the ADC clock with the use of programmable phase lock loops (PLL), direct digital synthesizers (DDSs) or frequency dividers and multipliers. The residual noise of these components can be considered part of φ_S and α_S, and will suppress according to the equations shown above. Moreover, the model in Figure 2 allows us to demonstrate that noise introduced on the ADC clock paths can be considered as aperture jitter, and therefore will be suppressed; while flicker noise introduced by components on the ADC input path can be considered as input-buffer noise, and therefore will partially suppress according to equation (5). This result allows the use of buffers and amplifiers on the clock and input ADC ports with minimal performance degradation. Also, since time modulation (x(t) noise) is greatly suppressed, cable length variations are compensated for from the points of injection of the correction signal to the ADCs.

III. EXPERIMENTAL RESULTS

A. HARDWARE

This flicker reduction technique has been implemented and tested on our newly developed prototype, visible in Figure 3. The prototype is composed by three main parts:

- Input module.
- Backplane.
- ZCU102 evaluation board.

The input module is the most critical part, and features the AD9652 16-bit dual ADC from Analog Devices, and all the electronics and power regulation to support the ADC. The input conditioning is implemented with a simple unbalanced-balanced transformer able to accept frequencies from 1 MHz to 400 MHz, and the module presents an adjustable low-noise voltage reference, and a loosely locked PLL as described in our previous article [9]. The input module also features an Artix-7 field programmable gate array (FPGA) to implement the DDCs, and a high speed serial communication link that sends the phase and amplitude data stream to the ZCU102 evaluation board for processing. These modules also have a temperature controller capable of maintaining the temperature of ADC, voltage reference, and input conditioning circuits constant. The temperature controller, however, has not been used during the measurements presented.

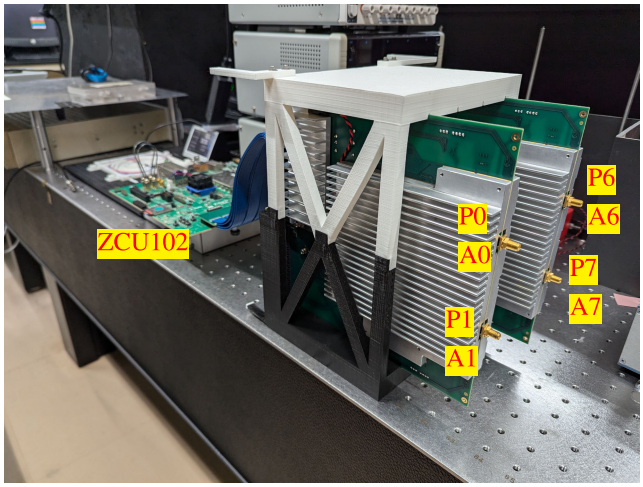

FIGURE 3. Picture of the prototype. The system features all custom modular hardware except for a ZCU102 evaluation board used as a temporary solution to perform the measurements presented. Here, *Px* and *Ax* represent the phase and amplitude of channel *x*(= 0, 1, 6 and 7) respectively.

The backplane, capable of hosting up to four input ADC modules, provides power conditioning, communication with the ZCU102 computation engine, and the system clock resources. The system clock includes a 1 GHz oscillator, a programmable PLL that generates the ADC clocking frequency, and a AD9912 DDS that produces the correction signal. The system clock can be steered, and it is frequency locked to one or an ensemble of the input signals to avoid moving spurs during the measurement.

The ZCU102 evaluation board controls and monitors the custom system, and implements decimation chains, Fourier and Allan deviation analysis pipeline similar to our previous prototype [9]. This evaluation board is a temporary solution, and these tasks will eventually be performed by a custom-made plug-in module in a future version.

B. MEASUREMENT SETUP

Two input modules (four ADC inputs) placed in the first and fourth slots of the backplane are used to test the effectiveness of FSDD. Three main residual measurements

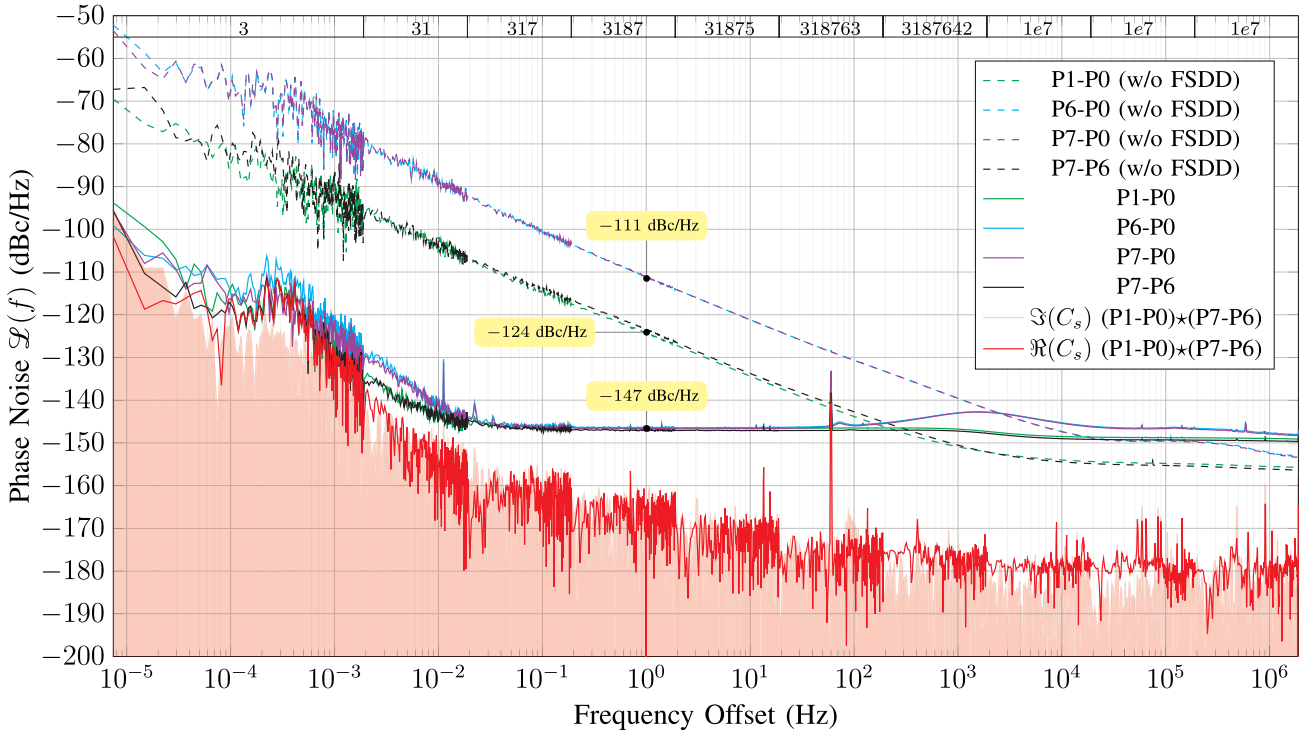

FIGURE 4. Residual phase noise at 100 MHz with a 104.2 MHz correction signal, compared to the residual noise using traditional direct-digital. Over 35 dB of close-to-the-carrier improvement is observed. The number of averages indicated on top are for the cross-spectrum measurement. *Px* represent the phase of channel *x*(=0, 1, 6 and 7).

are performed at 100 MHz using a NEL O-CDFE Series OCXO oscillator. The first evaluation is performed without the use of FSDD as a reference point, and the input signal power is maximized to cover the full dynamic range of the AD9652 (Figures 4, 5 and 6, repeated in Figures 7, 8 and 9). The second evaluation also incorporates a 104.2 MHz correction signal. To maximize the effectiveness of FSDD, and to minimize white noise degradation, the ADC dynamic range is divided equally to accommodate both the 100 MHz and correction carriers (Figures 4, 5 and 6). Due to the narrow frequency spacing between the test and correction signals, analog filters are not used, causing the noise sidebands of both signals to overlap. The third and final evaluation has been executed with the correction in the third Nyquist region at 307.25 MHz (Figures 7, 8 and 9). According to equation (5), in this last configuration the input buffer flicker suppression is less effective, and it's possible to identify improvements due to just aperture jitter and voltage reference noise removal. Moreover, in this case, band pass filters are used to avoid noise sidebands overlap and the power levels are adjusted to minimize white noise degradation for phase noise.

In all measurement setups, the ADCs are clocked at 288.312 MHz, the measurement bandwidths are kept constant, and residual phase and amplitude noise are evaluated between inputs of the same modules P1-P0 (A1-A0) and P7-P6 (A7-A6), and inputs from different modules P6-P0 (A6-A0) and P7-P0 (A7-A0). The P indicates phase analysis, while A is for amplitude. The number indicates the input channel number, and inputs from 2 to 5 are missing since the center two slots of the backplane are unpopulated. Finally, the measurements using inputs of the same modules are also cross-correlated. These types of measurements allow evaluating the residual performance of our prototype when used as a noise analyzer (cross-correlation and cross-spectrum averaging), or for timescale applications (different input combinations without cross-correlation). To avoid moving spurs during measurements, the system clock is frequency locked to an ensemble of DUT and REF such that the vectors in the 100 MHz dedicated DDCs rotate at 60 Hz. The constant rotation generates a spur, and this frequency has been chosen since a 60 Hz power network spur is expected anyway. The signal is distributed to the 4 inputs using four 2-way Wilkinson power splitter/combiners. The first device is used to combine the 100 MHz carrier with the correction signal (correction port terminated in the first measurement), and the other 3 are used to split the combined signal in a symmetrical tree fashion. Isolation of the power splitters and impedance matching are critical for cross-correlation and cross-spectrum averaging improvements.

C. 100 MHZ RESIDUAL NOISE

Figures 4, 5 and 6 show the great advantage of FSDD. Residual phase noise without FSDD measured at 1 Hz offsets $\mathscr{L}(1\text{Hz}) = -123.7\text{dBc/Hz}$ when inputs from the same ADC are used, and $\mathscr{L}(1\text{Hz}) = -111\text{dBc/Hz}$

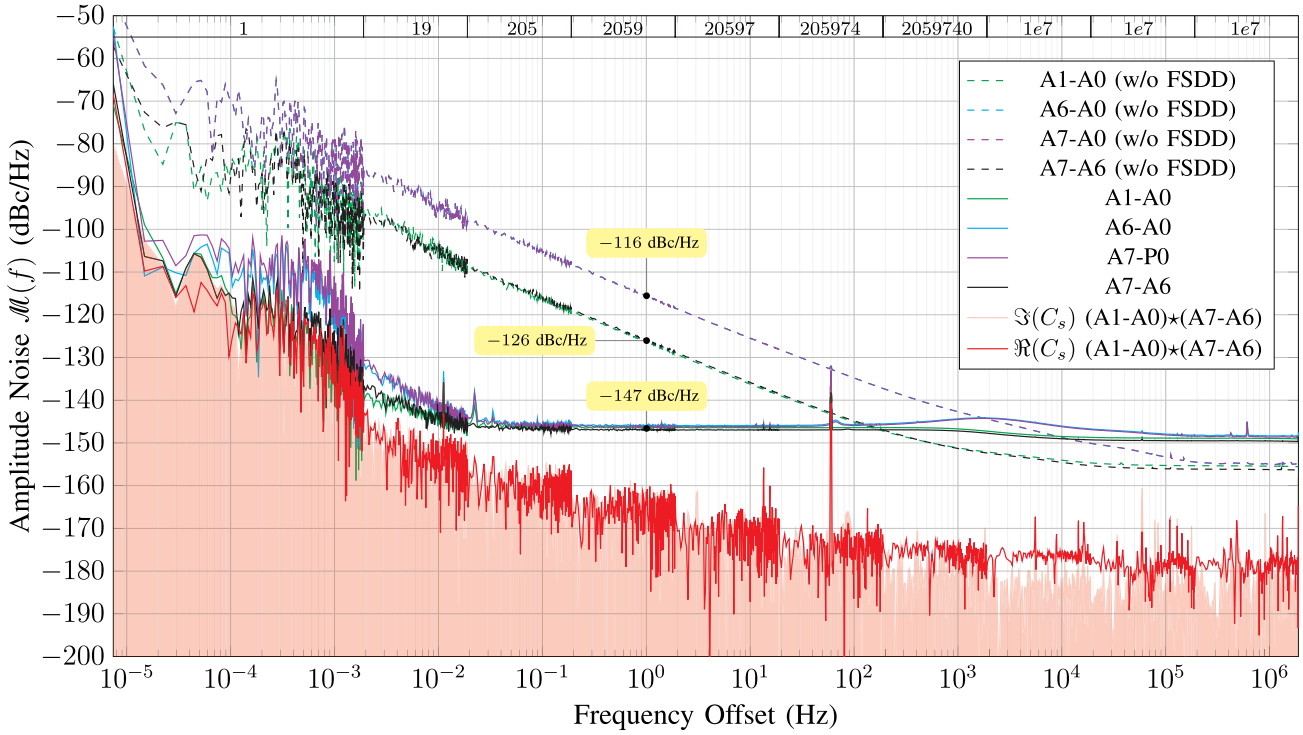

FIGURE 5. **Residual amplitude noise at 100 MHz with a 104.2 MHz correction signal, compared to the residual noise using traditional direct-digital. Over 35 dB of close-to-the-carrier improvement is observed. The number of averages indicated on top are for the cross-spectrum measurement. *Ax* represent the amplitude of channel *x*(=0, 1, 6 and 7).**

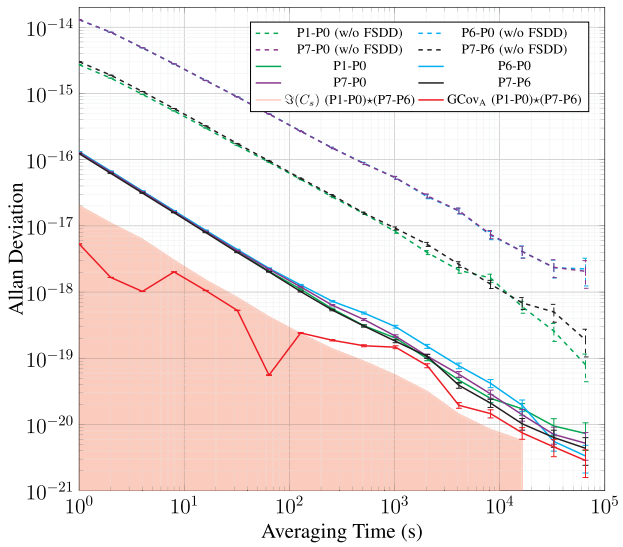

FIGURE 6. **Residual Allan deviation at 100 MHz with a 104.2 MHz correction signal, compared to the residual noise using traditional direct-digital. Over a factor of 20 improvement is observed. 0.5 Hz bandwidth.**

otherwise. Similarly, for residual single sideband amplitude noise, we register $\mathscr{M}(1\text{Hz}) = -126.0\text{dBc/Hz}$ and $\mathscr{M}(1\text{Hz}) = -115.5\text{dBc/Hz}$. For both phase and amplitude noise, FSDD suppressed flicker by over 35 dB when the correction frequency was very close to the measured signal of 100 MHz. Moreover, all input combinations show similar residual performance within the cut-off frequency (∼1 kHz) of the digital low-pass filters on the correction paths. Using FSDD, the system reached phase noise floors of $\mathscr{L}(1\text{Hz}) = -147\text{dBc/Hz}$ with a flicker corner of about 0.03 Hz for all input combinations, and these results can be further improved with the use of cross-spectrum averaging. Single channel white noise degradation with respect to the non-FSDD case is clearly visible due to the shared ADC dynamic range (above the digital filter cut-off frequency), and also due to correction (below the digital filter cut-off frequency). Cross-spectrum averaging also unveils numerous far-from-the-carrier spurs. Due to the presence of two carriers and their harmonics, inter-modulation products, and aliasing, it is difficult to find an ADC clock frequency that yields spur-free spectra when FSDD is used. Furthermore, the lack of analog filtering causes the sidebands of the two carriers to overlap. Combined with limited single-channel isolation, this restricts the ultimate noise floor achievable through cross-spectrum averaging. The small discrepancy in performance between single channels in the 10^{-3} to 10^{-2} frequency offsets area is suspected to be caused by different temperature coupling between input ports on the same or different modules. By taking advantage of the fact that a dual-input ADC presents highly correlated aperture jitter and voltage reference noise, the technique presented could be modified, such that the correction signal could be fed to one of the inputs while DUT or REF is measured on the other. In this way, white

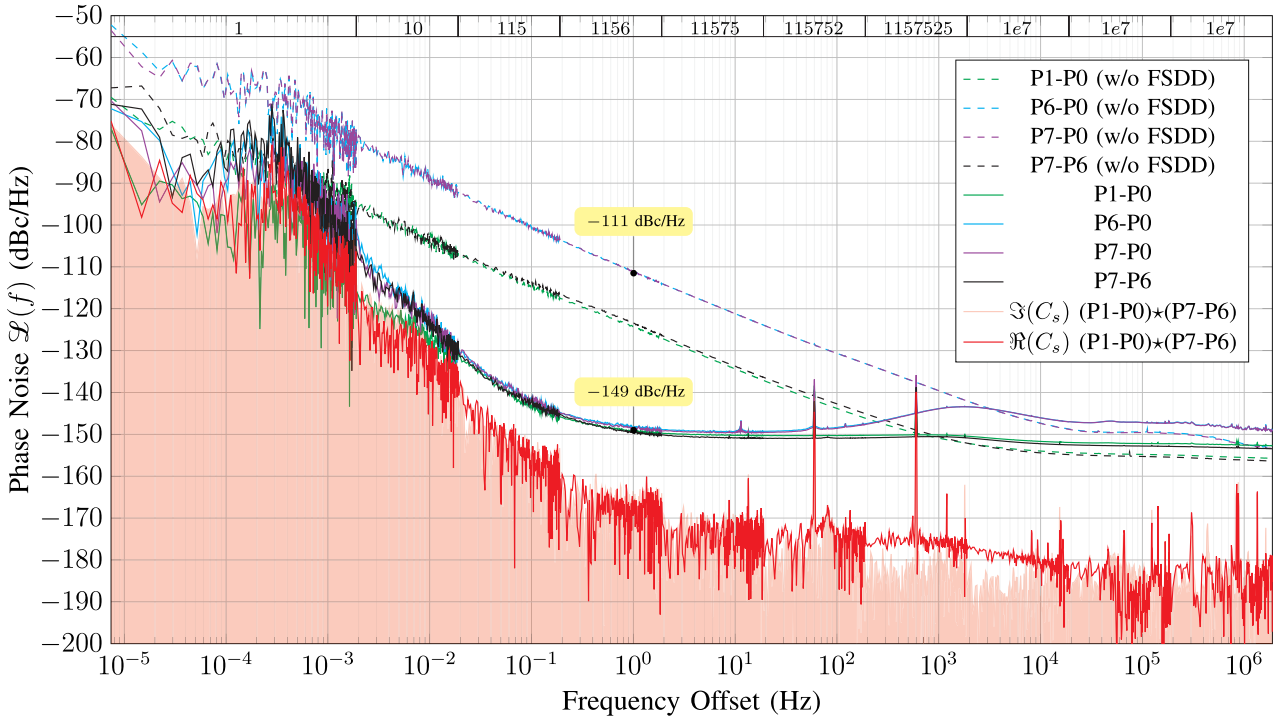

FIGURE 7. Residual phase noise at 100 MHz with a 307.25 MHz correction signal, compared to the residual noise using traditional direct-digital. Similar improvements are observed, but higher temperature sensitivity is present for phase noise. The number of averages indicated on top are for the cross-spectrum measurement.

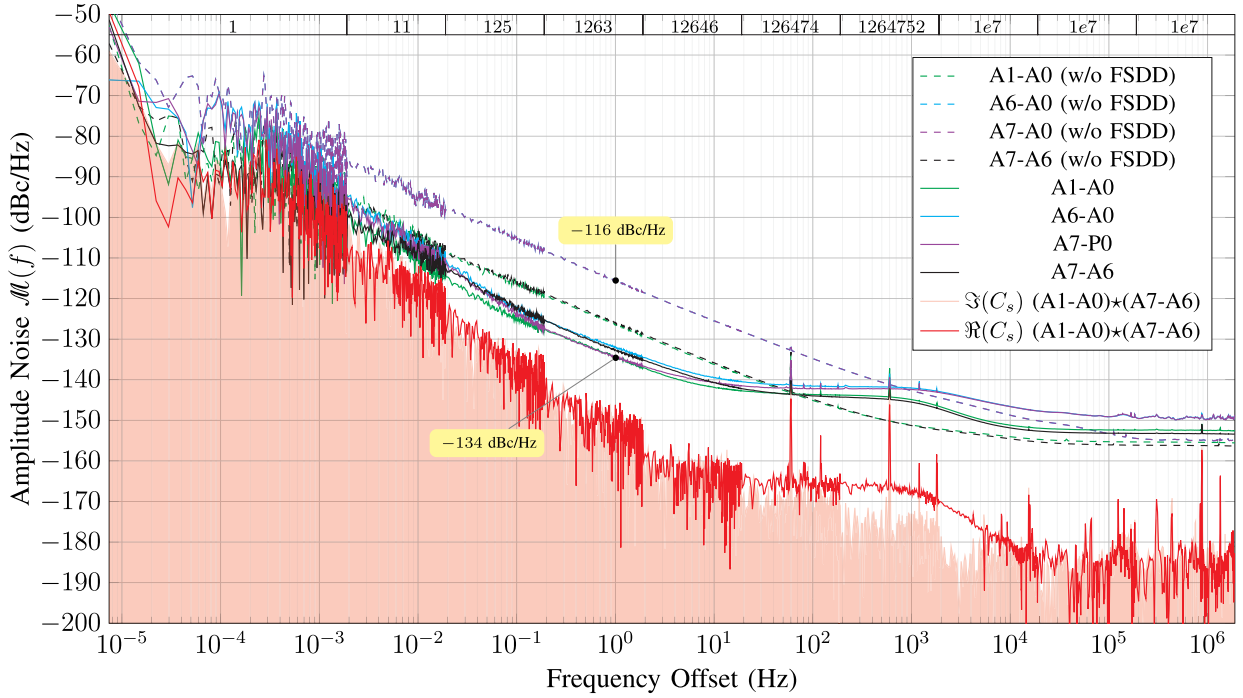

FIGURE 8. Residual amplitude noise at 100 MHz with a 307.25 MHz correction signal, compared to the residual noise using traditional direct-digital. FSDD is not very effective for amplitude noise. The number of averages indicated on top are for the cross-spectrum measurement.

noise and spectral purity performance can be preserved, and different ADC chips will present similar flicker performance to a single chip.

The residual Allan deviation also shows great improvements. At 1 s averaging times, the residual frequency stability improved from 3.0×10^{-15} and 1.3×10^{-14} for

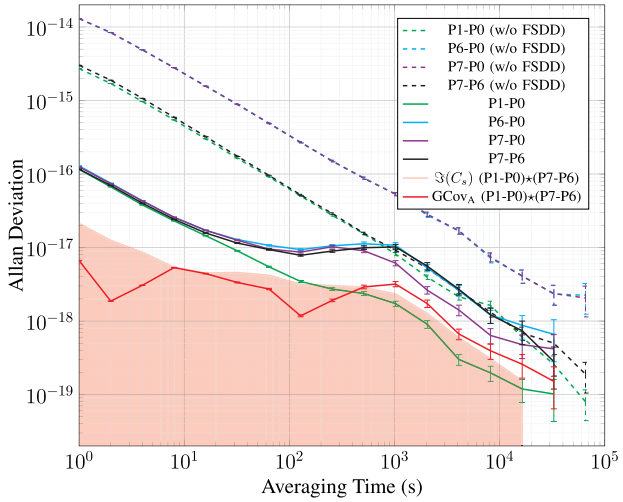

FIGURE 9. Residual Allan deviation at 100 MHz with a 307.25 MHz correction signal, compared to the residual noise using traditional direct-digital. Over a factor of 20 improvement is observed at 1 s, and temperature sensitivity limits the performance at higher averaging times. 0.5 Hz bandwidth.

inputs on the same module or different modules respectively, to 1.3×10^{-16} in both cases with a better $(1/\tau)$ behavior. More than a factor of 20 improvement in the single channel noise floor is achieved when FSDD is enabled, and these results can still be further improved with the Groslambert covariance (GCov), as shown in Figure 6.

On the other hand, in the last measurement setup, the correction frequency has been moved to 307.25 MHz and its power level has been decreased to about (1/4) of the ADC's dynamic range, leaving more room for the 100 MHz test signal. Figure 7 shows that FSDD is less effective for residual phase noise, even though it yields to slightly better white noise performance. Far from the carrier and above the digital low-pass filters' cut-off frequency the system can average below −180 dBc/Hz, while inside the ∼1 kHz cut-off frequency the single channels approach −150 dBc/Hz and the cross-spectrum is instead limited by the poor isolation at the correction signal's frequency. Close to the carrier, a steeper than flicker behavior is observed and has been attributed to temperature fluctuations causing $\varphi(t)$-type disturbances. The residual Allan deviation measurement (Figure 9) confirms that the system performs identically at 1-second intervals. However, for some input combinations, it exhibits a plateau between 100 and 1000 seconds, which is a typical range for thermal time constants. Above approximately 400 seconds, the 2-sample covariance also reveals correlation between (P1–P0) and (P7–P6).

The correction signal's low power causes highly degraded white noise performance below the digital filters' cut-off frequency for residual amplitude noise (Figure 8), and limited improvements in the flicker region. All input combinations show similar residual noise around 1 Hz offset and the residual noise between different modules shows almost 20 dB lower flicker, suggesting that the voltage reference noise has been successfully corrected for.

IV. CONCLUSION

A new and innovative flicker noise suppression technique that allows for greatly improved close-to-the-carrier performance in direct digital measurement systems for both phase and amplitude noise has been presented. Time domain measurements also significantly benefit from this method.

By testing the flicker suppression technique with correction signal both close and far from the DUT and REF carrier frequencies, the behavior predicted as predicted in equation (5) has been confirmed for phase noise. According to the theory, and confirmed by the presented results, FSDD is more effective when the correction frequency is placed closer to the test carrier (Figure 4 vs. 7). However, the amplitude noise model presented in Section II appears incomplete, as it predicts that improvements in amplitude flicker due to correction should be independent of frequency and power levels, whereas the experimental results demonstrate a clear dependence (Figure 5 vs. 8). A possible cause of this response is the strong dependency of residual amplitude flicker to carrier frequency and power.

Nevertheless, the prototype built to test the FSDD technique shows, for 100 MHz carriers, a residual single channel Allan deviation of 1.3×10^{-16} at 1 second averaging times regardless of which inputs are used, opening the door to multichannel measurement systems with state-of-the-art performance and capable of measuring and potentially ensembling the current best optical atomic clocks [16], [17]. The high effectiveness of FSDD showed in Fig. 4 suggests that residual fractional frequency performance metrics are expected to further improve at higher DUT carrier and ADC clock frequencies. We expect single channel residual Allan deviation in the low 10^{-17} at 1 s intervals for 1 GHz carriers. Unfortunately, the current prototype available does not support these frequencies.

The high inherent close-to-the-carrier noise of the ADCs limits the use of conventional digital measurement systems to far-from-the-carrier measurements of two-port devices, crystal and RF oscillators. The FSDD method, with its improved flicker response, enables close-to-the-carrier noise measurements of two-port components much more effectively, saving time that would otherwise have been needed for cross-spectrum averaging or the setup of advanced techniques such as carrier suppression [18], [19], [20]. The absolute phase noise of optical cavities or optical atomic clocks can be measured directly after converting the signals to the RF domain.

ACKNOWLEDGMENT

The authors would like to thank Jeffrey Sherman and Ben Pera for their useful comments on this manuscript. Certain equipment, instruments, software, or materials are identified in this article to specify the experimental procedure adequately. Such identification is not intended to imply

recommendation or endorsement of any product or service by NIST, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

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