Impact of Deep-Level Traps on Carrier Mobility in β-Ga_2O_3 MOSFETs

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***Abstract*— Gallium oxide (β-Ga_2O_3) is a promising semiconductor for high-power and high-frequency electronics due to its ultra-wide bandgap and high breakdown field. However, the carrier mobility in β-Ga_2O_3-based metal-oxide-semiconductor field-effect transistors (MOSFETs) remains significantly lower than its theoretical limit, often attributed to the presence of deep-level traps. In this work, an electro-optical measurement technique is used to study ionized impurity scattering by deep-level traps in lateral depletion-mode β-Ga_2O_3 FETs. Using the conductance method and photo-assisted capacitance-voltage (PCV) measurements with sub-bandgap illumination from 730 nm (1.7 eV) to 280 nm (4.4 eV), the density of interface trap states (D_{it}) in β-Ga_2O_3 FETs was determined between 0.4 eV – 4.4 eV below the conduction band (E_C) of β-Ga_2O_3. D_{it} peaks near the band edges, similar to conventional material systems. Based on the results, traps located between E_C – 4.0 eV and E_C – 3.4 eV are primarily responsible for carrier scattering, reducing the mobility by 50 % – 75 % in these devices with increasing distance from the interface. The increased mobility degradation further from the interface is attributed to traps located in the bulk.**

***Index Terms*— Ga2O3, interface defect, trapping, lateral transistor**

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I. Introduction

BETA-PHASE gallium oxide (β-Ga_2O_3) is quickly emerging as a promising ultra-wide bandgap (UWBG) semiconductor for high power and RF applications. Additionally, β-Ga_2O_3 is the only wide bandgap (WBG) semiconductor that can be grown from the melt, giving rise to large, high quality, and low-cost substrates that are projected to be nearly 80 % cheaper than SiC [1], [2], [3]. The performance of β-Ga_2O_3 high power devices have progressed rapidly in recent years as Schottky barrier diodes [4], [5], [6], [7] and field-effect transistors (FETs) [8], [9], [10], [11]. Even with this progress, there is still significant amount of defects and traps which hinder the device performance. Interface and oxide traps pose problems for β-Ga_2O_3 transistors through premature gate oxide breakdown due to trap-assisted tunneling [12], threshold voltage instabilities [13], [14], [15], and current dispersion in DC or RF operation[16], [17].

Traditional trap characterization methods, developed for narrow bandgap devices, are sensitive to shallow traps (i.e., near the band edges) and these methods include deep level transient spectroscopy (DLTS) [18], [19], [20], [21] positive and negative bias stress instability[13], [14], [15], [22], high- and low-temperature I-V and C-V [23], [24], and pulsed I-V [16], [17]. However, the long emission time of deep traps in WBG semiconductors requires the use of optical excitation and novel techniques such as deep-level optical spectroscopy [20], [25], [26], persistent photo-capacitance[27], photo-assisted C-V (PCV) [28], [29], [30], and photo-assisted I-V (PIV) [31]. These methods provide a means to extract useful information about traps such as its concentration, spatial and energy locations, degradation mechanisms, and time constants. Additionally, it is well known that high densities of traps can significantly reduce mobility by scattering free carriers. In WBG devices, this has primarily been studied for shallow interface traps in SiC inversion FETs [32], [33], [34], [35], but few studies have focused on the scattering effects of deeper traps in β-Ga_2O_3 FETs. For β-Ga_2O_3 at a carrier concentration

of 10^{19} cm^{-3} at room temperature, experiment has reported a spread in the Hall mobilities ranged 25 cm^2 V^{-1} s^{-1} – 100 cm^2 V^{-1} s^{-1} [36]. The spread in the experiment values suggest scattering mechanisms must be considered. The reported discrepancy between μ_{Hall} and field-effect mobility (μ_{FE}) can also be attributed to the large density of interface or defect states, as has been widely reported in SiC MOSFETs [37], [38]. Thus, it reinforces the need to critically probe and assess the impact of charge traps that limit the performance of β-Ga_2O_3 devices.

In this work, a room temperature electro-optical measurement technique is used to study the ionized impurity scattering of deep level traps in a lateral depletion-mode β-Ga_2O_3 FET. Using PCV and PIV with sub-bandgap photon energies, E_{hv}, the effective mobility, μ_{eff}, is measured under different trapping conditions. The PCV and subsequent PIV methods rely on modulating the charge state of deep-level traps to quantify their density and impact on carrier transport. A spatial-dependent scattering model is used to fit mobility impacted by ionized impurities (μ_{ii}) and provides insight into the traps responsible for mobility degradation.

II. Experimental Methods

The device fabrication details are described elsewhere [39] and only briefly mentioned here. A 50 nm β-Ga_2O_3 Si-doped epitaxial layer was grown on a semi-insulating substrate by molecular beam epitaxy with a target doping density (N_D) of 2.4 × 10^{18} cm^{-3}, verified by electrochemical C-V. Ohmic contacts were formed using a Ti/Al/Ni/Au metal stack and rapid thermal annealing at 470 °C for 1 minute in N_2. A 20 nm Al_2O_3 gate oxide was then deposited by plasma-enhanced atomic layer deposition. Finally, a Ni/Au stack was deposited as the gate metal. The MOSFET dimensions were determined by atomic force microscopy, measuring a width of 100 µm, source-gate and gate-drain spacings of 0.3 µm, and gate length of 1.25 µm. A cross-section schematic of the MOSFET is shown in Fig. 1(a).

DC characterization measurements were performed using an Agilent 4156B semiconductor parameter analyzer, C-V and PCV measurements were performed using a Keysight E4980A LCR meter, and the PIV measurements were made using a Keysight 81150A arbitrary waveform generator and a Tektronix MS064B mixed signal oscilloscope [40]. (P)CV measurements were performed at 200 kHz with ac modulation of 0.05 V and parallel plate model, while frequency-dependent CV measurements were performed between 100 Hz and 2 MHz. Illumination for PCV and PIV measurements were done with sub-bandgap light, to avoid creating electron-hole pairs [41]. LEDs with wavelengths ranging from 730 nm (1.7 eV) to 280 nm (4.4 eV) were used for PCV, while only 455 nm (2.7 eV), 395 nm (3.1 eV), 365 nm (3.4 eV), and 310 nm (4 eV) LEDs were used for PIV because of the minor changes in mobility at the longer wavelengths. The photon flux of the LEDs was kept constant at 3 x 10^{14} cm^{-2} s^{-1} for all measurements.

III. Results and Discussion

The MOSFET DC transfer and output curves are measured in the dark, and the characteristics of typical of working devices on the investigated chip are shown in the supplemental information (SI) Fig. S1. Briefly, the transistor exhibits a threshold voltage of -4 V, an on/off ratio of 10^{10}, a low gate leakage of 7 x 10^{-9} mA mm^{-1}, and good saturation behavior [39] and these results provide a basis for comparison to the PCV and

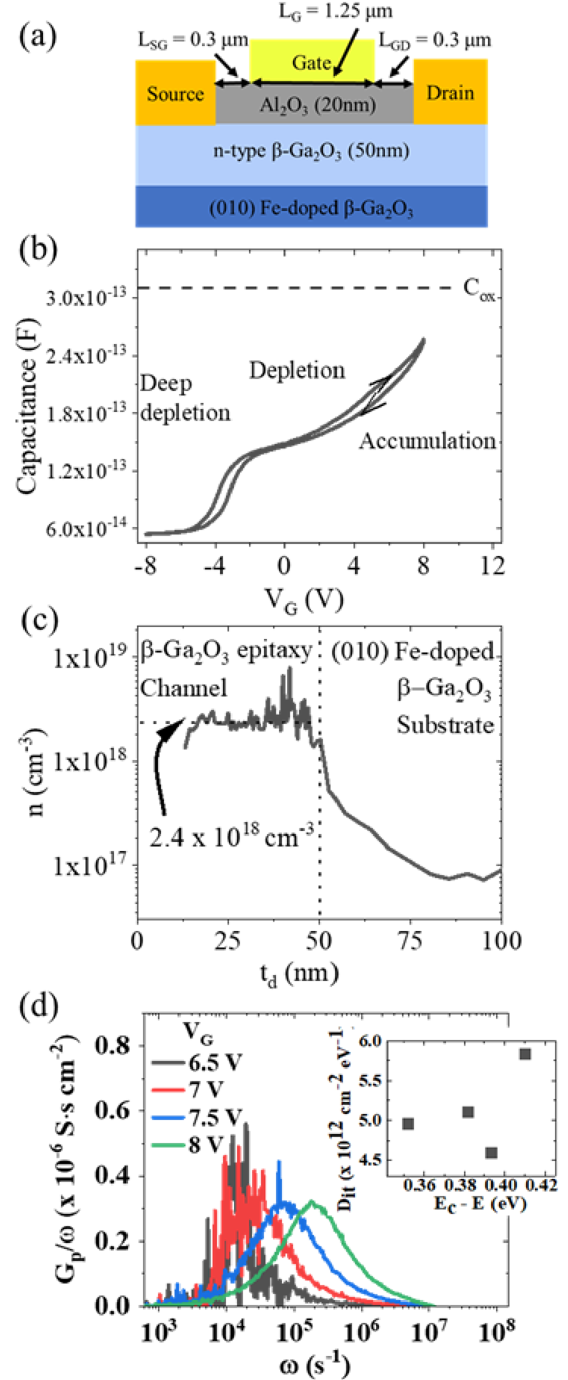

Fig. 1. The lateral MOSFET device (a) schematic cross-section, (b) gate capacitance C-V hysteresis of the FET at 200 kHz with a C_p-G_p model, (c) free carrier concentration (n) versus depth (t_d) calculated from the C-V curve in (b), and (d) frequency-dependent parallel conduction G_P ω^{-1} versus ω from frequency sweeps with the inset showing the calculated D_{it} from the conductance method. In (b), the high density of interface traps stretches out the C-V curve and prevents reaching flatband and accumulation before gate-oxide breakdown occurs. In (c), the dotted horizontal line and dashed vertical line indicate the target N_D and epitaxy thickness.

PIV results. The FET gate capacitance was measured from a gate voltage (V_G) of -8 V to 8 V and displays a slight hysteresis, shown in Fig. 1(b). The oxide capacitance (C_{ox}), denoted by the dashed flat line at 310 fF, was determined using metal-insulator-metal (MIM) capacitors on the same chip. The flatband voltage (V_{FB}) was estimated by linear extrapolation of the $(C_{ox}/C)^2 - 1$ line to the V_G axis. The V_G is not swept beyond 8 V in order to avoid gate-oxide breakdown (> 10 V) which is attributed to the high density of interface traps; therefore, the device does not reach true accumulation since V_G does not go to the flatband voltage. This effect is referred to as C-V stretch-out [42]. We systematically determined the V_{FB} using the following criteria: 1) the slope $(C_{ox}/C)^2 - 1$ versus V_{gate} from post-depletion (with light) had to be nearly the same as pre-depletion (i.e., dark), and 2) the range is extrapolated within range -5 V to 5 V to limit the LCR meter artefact. More details are in Supplemental Section F. We also determined that waiting 30 min between post-depletion and pre-depletion measurement sequence is sufficient to reset the device and ensures that it returns to the same initial state (i. e., traps filled) for all subsequent measurements. In Fig. 1(c), the depletion depth (t_d) and carrier density (n) were found using (1) and (2), respectively [43]:

$$\varepsilon_s \varepsilon_0 A \left(\frac{1}{C} - \frac{1}{C_{ox}}\right) \quad (1)$$

$$\frac{2}{q \varepsilon_s \varepsilon_0 A^2 d(1/C^2)/dV_G} . \quad (2)$$

The constants ε_s, ε_0, and A are the semiconductor dielectric constant, permittivity of free space, and gate area, respectively. The n versus t_d profile in Fig. 1(c) confirms that the carrier density and channel thickness are close to their target values of N_D (2.4×10^{18} cm^{-3}) and 50 nm, respectively. Also inferred from Fig. 1(c), the band bending between the channel and substrate interface results in a depletion of carriers about 5 nm into the channel and a carrier density tail from 50 nm to approximately 70 nm into the substrate side. The equivalent parallel conductance ($G_P\ \omega^{-1}$) versus ω at various V_G, is shown in Fig. 1(d). The peak parallel conductance shows a maximum and the frequency where the maximum $G_P\ \omega^{-1}$ occurs varies with V_G, and together this suggests the presence of interface traps [44]. The interface trap state density (D_{it}) as a function of energy below the conduction band (E_C – E, or trap energy) is calculated using the conductance method and frequency-capacitance measurements from 100 Hz to 2 MHz. The energy below the conduction band is determined using (3):

$$E_C - E = kT ln(\frac{\sigma\, v_{th}\, N_C}{\pi f}) \quad (3)$$

where σ is capture cross-section of the trap and assumed as 1 x 10^{-15} cm^{-2} [45], v_{th} is the thermal velocity of carriers and estimated as 2.2×10^7 cm s^{-1}, and N_c is the effective conduction band density of state and estimated as 3.7×10^{18} cm^{-3}. The inset shows the calculated D_{it} and trap energy from the peaks in G_P ω^{-1} versus ω. Using this method, only shallow traps down to E_C – 0.4 eV can be probed due to the high emission time constants of deeper traps at room temperature [46].

In order to investigate the distribution of traps deeper below E_C, photo-assisted C-V (PCV) measurements are used. Sub-gap illumination with photon energies of 1.7 eV to 4.4 eV is used, where the PCV timing diagram is shown in Fig. 2(a) and summarized here. First, the capacitance is measured while the gate voltage (V_G) is swept where the device goes from near accumulation (A) to deep depletion (D) in the dark immediately before illumination (referred to as "pre-depletion"). This is immediately followed by holding the device in depletion either in dark or while shining light for times between 1 min – 60 min ($t_{hold,n}$). During illumination, electrons trapped between E_C and (E_C - E_{hv}) are excited into the conduction band and then swept away due to the depletion electric field. After $t_{hold,1}$ has passed, the illumination is turned off and the capacitance is measured by sweeping V_G from D to A (referred to as "post-depletion"). The dark measurements (referred to as pre-dark and post-dark) provide a reference for those with illumination. To reset the device (i.e., traps are re-occupied), a 30 min wait is added between sweeps. The measurement is then repeated with a longer holding time, $t_{hold,2}$.

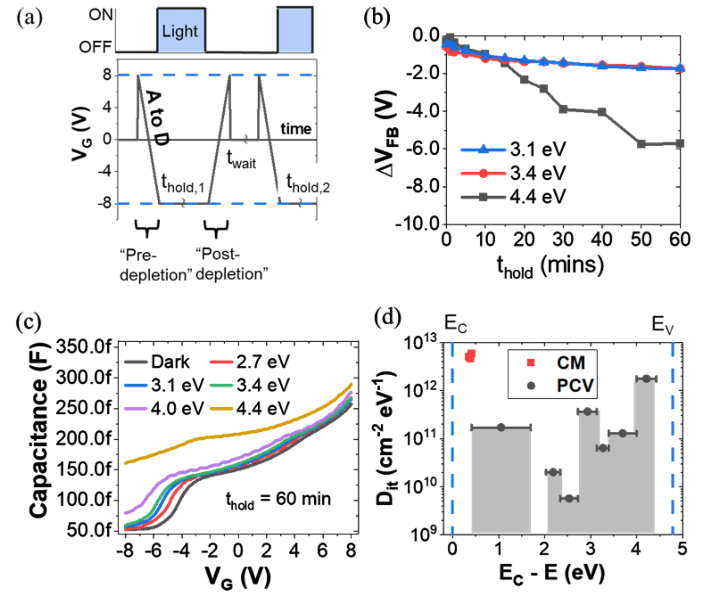

Fig. 2. The PCV measurement at 200k Hz and derived results: (a) timing diagram of the PCV measurement, (b) ΔV_{FB} versus holding time at different photon energies, (c) post-depletion C-V curves showing changes in capacitance with increasing photon energy, (d) D_{it} from the conductance method (CM, red dots), and PCV data (shaded grey). In (b), measurements are compared at 60 minutes because the PCV curve with 4.4 eV illumination nearly flattens then. The bar width in (d) represent the average value of D_{it} for the range (hv_1 – hv_2) due to the limited, discrete nature of LED wavelengths used.

The resulting flatband voltage shift (ΔV_{FB}) between the pre-depletion and post-depletion capacitance has been proposed as an approximate measure of the average D_{it} between E_C and E_C - E_{hv}. This electro-optical method is sensitive to all deep levels within the measurement window, including true interface states, oxide border traps close to the interface, and near-interface bulk traps in the semiconductor as the absorption of sub-E_{gap} light is significant [47], therefore D_{it} is used broadly for these traps. However, the specific timing sequence employed between pre- and post-illumination C-V sweeps inherently mitigates the influence of certain non-modulating charges, such as fixed oxide charge or border traps with very long emission time constants. For a given photon wavelength, the holding time required to remove all charge from interface traps is determined when ΔV_{FB} saturates. As seen in Fig. 2(b), the 4.4 eV illumination is the limiting factor where ΔV_{FB} nearly becomes constant near 60 mins. The $|\Delta V_{FB}|$ continues to slightly grow with holding times longer than 60 mins, indicating that the

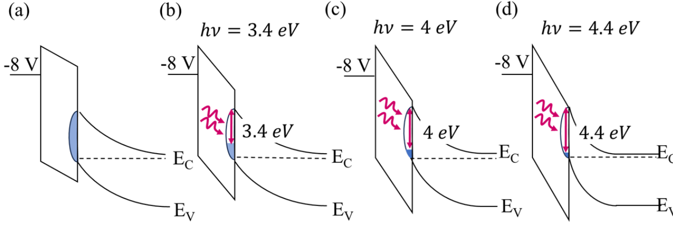

Fig. 3. Band diagrams of the FET in the PCV hold-state in (a) dark, and (b) 3.4 eV, (c) 4.0 eV, and (d) 4.4 eV illumination. The occupied D_{it} is shown by the blue shaded area. In dark, deep traps above the Fermi level, denoted by the dashed line, remain filled due to their high emission time constants. Illumination, however, excites trapped electrons into the conduction band, emptying traps from E_C to E_C - E_{hv} and shrinking the depletion region as the net charge at the interface becomes less negative.

calculated D_{it} is only a lower bound. The post-depletion C-V curves at 60 mins for dark and illumination at 2.7 eV, 3.1 eV, 3.4 eV, 4 eV, and 4.4 eV are shown in Fig. 2(c). The leftward shift of the C-V with increasing photon energy is a direct result of the increasing number of empty traps. The D_{it} is then calculated using (4):

$$D_{it}\ (E_C - \ (E_{hv1} - E_{hv2})) = \frac{C_{ox}}{A}\frac{(\Delta V_{FB,hv1} - \Delta V_{FB,hv2})}{q(hv_1 - hv_2)} \quad (4)$$

where hv_1 and hv_2 refers to the larger and smaller energy light, respectively. The resulting D_{it} determined from the conductance method (see Fig. 1(d)) and PCV are shown in Fig. 2(d), where it rises near the conduction and valence bands, resembling the D_{it} of many common semiconductor/oxide interfaces [32], [48], [49]. The post-depletion C-V at 4.4 eV illumination is significantly different than lower energy illumination where we observed an increase in carrier concentration. This coincides with defect E8 in β-Ga_2O_3 [20], [26], [50] which is about 4.4 eV below E_C. It is possible that 4.4 eV light is releasing trapped negative charge, however the origin of E8 is still under investigation. Based on PCV, the free carrier concentration versus depletion depth does not significantly change with illumination at 2.7 eV, 3.1 eV, 3.4 eV, and 4.0 eV.

The band diagrams in Fig. 3 illustrate the changes in trap occupation, depletion depth, capacitance, and oxide electric field derived from the PCV results. The band diagram was sketched using commonly accepted β-Ga_2O_3 values of band gap (4.8 eV), $E_c - E_F$ (36 meV), electron affinity (4 eV), electron affinity of Al_2O_3 (2 eV), and work function of Ti (3.9 eV). Enough bias is applied so that the depletion extends to the substrate (i.e., beyond 50 nm), Fig. 3(a). As mentioned earlier, traps above the Fermi level remain occupied because of their long emission time constants. Illuminating the sample with photons of energy E_{hv} empties traps from E_C to E_C - E_{hv}, Fig. 3(b-d). From Fig. 3(a) to Fig. 3(d), as the traps become unoccupied with exposure to larger photon energies, the depletion region decreases and the electric field across the oxide increases due to charge balance. The net interface charge becomes less negative as electrons are removed. The charge balance between the interface and depletion charge reduces the depletion region, resulting in an increased capacitance, as observed in the PCV result in Fig. 2(c), and a larger oxide electric field as less voltage is dropped across the depletion region.

To probe the effect of traps on carrier mobility, PIV is utilized to extract conductance (g_{d0}), effective mobility (μ_{eff}), and mobile charge density (Q_n). The effective mobility, μ_{eff}, is calculated in (5) from the drain conductance, g_{d0}, and mobile charge density, Q_n, using

$$\mu_{eff} = \frac{Lg_{d0}}{WQ_n}\bigg|_{V_{GS}} \quad (5)$$

The PCV measurements are used to calculate Q_n by integrating the n with respect to t_d in Fig. 1(c). A PIV measurement is used to determine g_{d0} from the slope of the I_D – V_D curve, and the source and drain (including contact) resistance were de-embedded to account for the light access regions in the measurements [43]. More details on calculating Q_n and g_{d0} are in the supplementary information. The PIV timing diagram, Fig. 4(a), is similar to that of the PCV. To maintain the device in the linear region, the drain-source voltage (V_{DS}) is swept from 0.1 V to 0 V (i.e., reverse sweep)

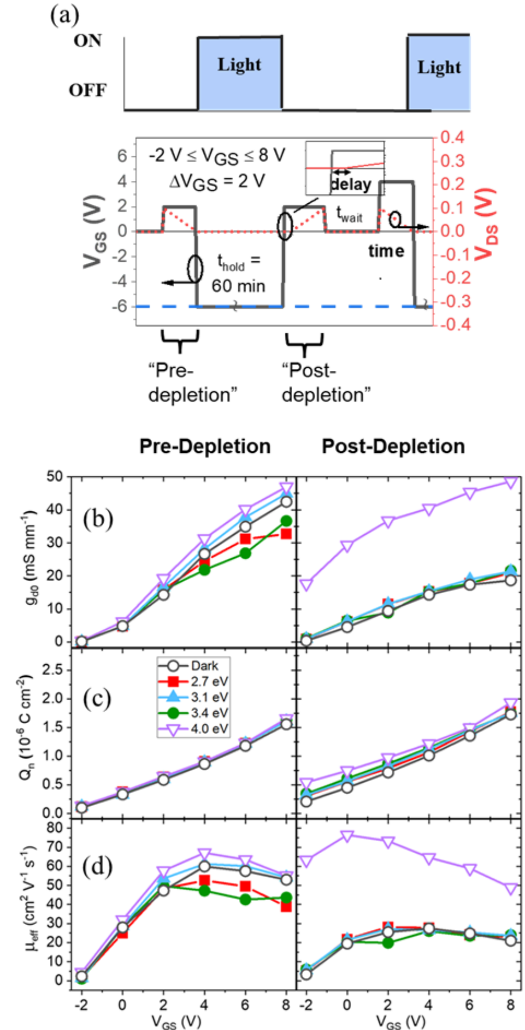

Fig. 4. The PIV (a) timing and measurement diagram and derived pre-depletion and post-depletion results of (b) conductance g_{d0}, (c) mobile charge density Q_n, and (d) effective mobility μ_{eff}. Only 4.0 eV illumination significantly impact derived μ_{eff}.

at a constant V_{GS} and this constitutes as the reference, pre-depletion g_{d0} regime. The device is then biased in depletion, with V_{DS} at 0 V for 1 hour, in either dark or illumination conditions. Afterwards, V_{GS} returns to the pre-depletion value, the forward sweep of the V_{DS} is performed (after a short period to stabilize the device) to determine the post-depletion g_{d0}. After a 30 min wait to reset the device, the measurement is repeated at the next V_{GS} value, where it is varying from -2 V to 8 V in 2 V increments.

Fig. 4(b) – (d) shows g_{d0}, Q_n, and μ_{eff}, respectively, under dark and 2.7 eV to 4.0 eV illumination conditions. The device stress caused by holding in depletion for 1 hour results in a lower g_{d0} and μ_{eff} when comparing the dark pre-depletion and post-depletion results. When comparing the post-depletion curves, 4 eV illumination measurements resulted in significant variation of g_{d0}, thus impacting μ_{eff}. Along with higher mobilities, there is also a leftward shift, similar to the C-V curves in Fig. 2(c), due to the emptied traps at 4 eV illumination. Series resistance varied by less than 5 % under 2.7 eV to 4.0 eV illumination compared to dark via TLM measurements (see supplemental section C) and is therefore assumed to be constant for de-embedding purposes.

The improved effective mobility determined by PIV at 4.0 eV suggest that there could be scattering sites within this energy window which may have considerable impact on device performance. Common charge scattering mechanisms that can impact mobility are acoustic-phonon, neutral impurities, surface roughness, and Coulomb scattering (see the supplementary information for more details). Phonon and acoustic deformation potential scattering are assumed constant since all measurements are taken at room temperature. Neutral impurities scatter carriers that are directly in its path [51] and only impact the mobility if they are located in the channel region. The density of neutral impurities in the channel is assumed constant since we do not anticipate light interacting with neutral impurities. Thus, the ionized impurity (Coulomb) and surface roughness scattering mechanisms remain for consideration. To determine the dependencies of both mechanisms, the post-depletion mobilities are plotted against the depletion depth, t_d, and the effective surface electric field, E_{eff}, in Fig. 5(a). The increasing mobility with t_d follows ionized impurity scattering because the larger separation between the channel and charged traps reduces the Coulombic force on the mobile charge. This is important in depletion-mode FETs where the channel can be far from the interface. The surface roughness mobility is inversely proportional to E_{eff}, however, and Fig. 5(a) indicates that this mechanism is not present here. This is primarily because the FET is operating in depletion, where the channel is far from the surface [52], and becomes dominant in accumulation [53], where a high density of carriers are located close to the surface.

Considering only ionized impurity scattering, the effective mobility can be express as:

$$\mu_{eff}(N_{ii}, t_d) = \frac{\mu_0}{1 + \alpha N_{ii} \exp\left(\frac{-t_d}{l_{crit}}\right)} \quad (6)$$

where μ_0 is the low-field mobility, N_{ii} is the charged trap state density, α is a fitting factor of the charged traps [32], and l_{crit} is a fitting parameter which estimates the influence of traps far from the interface and is adapted from Matthiessen's Rule to include interface charge scattering model [54]. Here, the μ_0 of 90 $cm^2\ V^{-1}\ s^{-1}$ was selected to improve the fitting and is in agreement with recent experimental Hall mobility results [36]. The exponential term accounts for the spatial dependence of the ionized impurity scattering using the depletion depth, t_d, from Fig. 1(c). Equation (6) is used to fit the measured post-depletion mobilities using a least-squares method, shown as solid lines in Fig. 5(a). The value of N_{ii} values are found from (7) by:

$$N_{ii} = \left| \int_{E_V}^{E_C - E_{h\nu}} D_{it}\, dE \right|, \quad (7)$$

assuming deep traps are charged when filled with electrons and neutral when empty, which is consistent with deep level traps found in β-Ga_2O_3 [20], [26], [27]. The N_{ii} near E_V was assumed

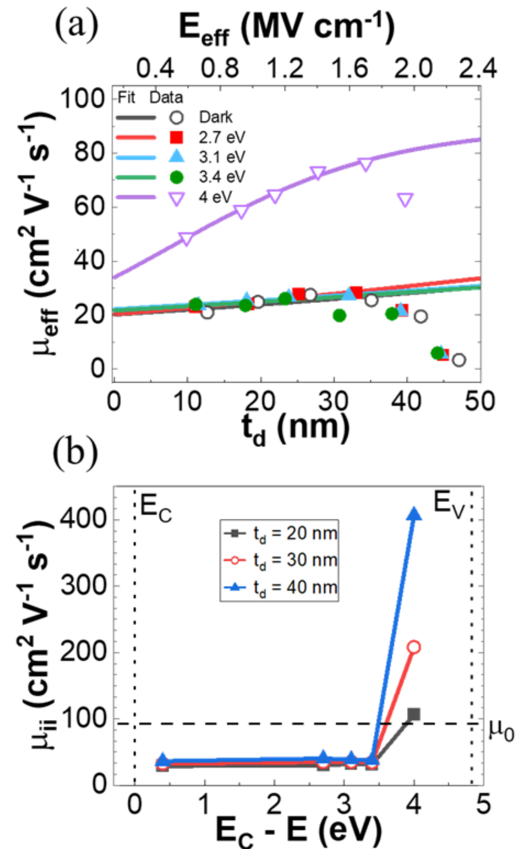

Fig. 5. Calculated post-depletion (a) μ_{eff} versus t_d and E_{eff} (symbols) and (b) μ_{ii} as a function of the occupied trap level relative to the conduction band at different depletion depths. Fits of μ_{eff} versus t_d using equation (6) are also shown (lines). In (b), the left and right dashed lines denote the valence and conduction band, respectively, and the horizontal dashed line is μ_0 (90 $cm^2\ V^{-1}\ s^{-1}$) as explained in the main text. The traps primarily responsible for reducing the mobility, observed by the large drop in μ are located between E_C - 4.0 eV and E_C - 3.4 eV.

to be 5 × 10^{12} cm^{-2}, similar to the shallow D_{it} from the conductance method. However, since α is a fitting parameter in Equation (6), the value of N_{ii} does not demand precision. The corresponding fit parameters are summarized in the supplementary information, section E. In Fig. 5(a), the distinct rise in mobility between 3.4 eV and 4.0 eV illumination is in an

indication that the traps between E_C – 3.4 eV and E_C – 4.0 eV reduce carrier scattering when empty and increase scattering when occupied. Therefore, traps residing between E_C – 3.4 eV and E_C – 4.0 eV are an overall detriment to device operation by increasing the scattering effects which reduces mobility.

Likewise, the traps impact carrier mobility due to the ionized impurity traps mobility contribution, μ_{ii}. The effective mobility can be described using Matthiessen's rule, $\mu_{eff}^{-1} = \mu_0^{-1} + \mu_{ii}^{-1}$. In Fig. 5(b), μ_{ii} is shown where the occupied trap level is relative to the conduction band, with all traps are unoccupied at E_V and occupied at E_C. Each data point corresponds to the different measurements taken in dark or under illumination. The left-most point is from the dark, conductance method measurement (see Fig. 1(d) located at (E_C - 0.4 eV). Similarly, the right-most point is from the 4.0 eV illumination measurement, located at (E_C - 0.8 eV). The mobility due to ionized impurities varies as traps in each energy range switch from empty to occupied; the large drop in μ_{ii} highlights the strong scattering effects of the occupied deep traps between (E_C – 3.4 eV) and (E_C – 4.0 eV). All other trap ranges show similar scattering.

While traps can originate from a multitude of reasons beyond material composition, bulk traps remain as a possible explanation for the observed scattering based on the dominance of ionized impurity scattering in a depletion-mode device, coupled with the spatial dependence of scattering. Bulk traps that have been suspected as strong scatterers between (E_C – 3.4 eV) and (E_C – 4.0 eV) could correspond to H3 hole traps with physical origins such as self-trapped holes (STH), gallium vacancies (V_{Ga}), or V_{Ga} complexes with hydrogen [20], [27]. Different densities of these electron and hole traps can correspond to the observed increase in μ_{ii} when occupied. The larger difference in μ_{ii} (and therefore μ_{eff}) with increasing depletion depth (Figure 5a) is consistent with the exponential distance dependence of Coulomb scattering originating from these deeper, bulk-like centers. Further studies on the origin and mitigation of these deep-level bulk and interface traps are crucial for realizing devices with high mobilities, with isolation structures to interrogate defects and substrate conduction. FET mobilities are approaching Hall mobilities [8] which attests to the drive to reduce interface, border, and bulk trap state densities. It is therefore essential to identify mobility-limiting traps for continual improvement in device performance.

IV. Conclusion

In this work, we present a room-temperature electro-optical measurement technique that probes the impact of deep-level interface and bulk traps on carrier mobility in lateral β-Ga_2O_3 MOSFETs. By integrating photo-assisted C-V and I-V measurements under sub-bandgap illumination, we extract the energy-dependent effective mobility and isolate the contribution of specific trap states to ionized impurity scattering. Our analysis reveals that deep-level traps located within the energy range of E_C – 4.0 eV and E_C – 3.4 eV are primarily responsible for mobility degradation, reducing effective mobility by up to 75% relative to the trap-free case. Bulk traps in this energy range, such as H3 hole traps originating from self-trapped holes and gallium vacancies, are located closer to the channel and explain the larger difference in μ_{eff} with depletion depth. Surface roughness scattering was determined to have minimal influence under depletion-mode biasing, consistent with the observed trends in mobility versus electric field. This methodology provides a powerful framework for identifying and characterizing mobility-limiting defects in ultra-wide bandgap devices. The ability to localize and quantify the energetic and spatial distribution of active trap states offers critical guidance for targeted defect passivation and interface engineering, ultimately advancing the development of high-performance β-Ga_2O_3 power electronics.

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