

Picosecond Josephson Samplers: Modeling and Measurements

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Measurement of signals generated by superconducting Josephson junction (JJ) circuits require ultra-fast components located in close proximity to the generating circuitry. We report a detailed study of optimal design criteria for a JJ-based sampler which balances the highest sampler bandwidth (shortest 10%–90% rise time) with minimal sampled waveform distortion. We explore the impacts on performance of a sampler, realized using a single underdamped JJ as the logical sampling element (*the comparator*), due to the type of signal-comparator coupling scheme that is utilized (galvanic, inductive, or capacitive). In these simulations we emulate the entire waveform reconstruction sampling process, via comparator threshold detection, while sweeping the time location at which the waveform is being sampled. We extract the sampled waveform rise time (or FWHM) as a function of the comparator's Stewart-McCumber parameter and as a function of the coupling strength between the device under test and comparator. Based on our simulation results we design, fabricate, and characterize a cryocooled (3.6 K operating temperature) JJ sampler utilizing the NIST state-of-the-art Nb/amorphous-Si/Nb junctions. We separately sample a step signal and impulse generator co-located on-chip with the comparator and sampling strobe generator by implementing the same binary search comparator threshold detection technique during sampler operation as is used in simulation. With this technique the system is fully-digital and automated and operation of the fabricated device directly mirrors simulation. Our sampler technology shows a 10%–90% rise time of 3.3 ps and the capability to measure transient pulse widths of 2.5 ps FWHM. A linear systems analysis of sampled waveforms indicate a 3 dB bandwidth of 225 GHz, but we demonstrate effective measurement of signals well above this – as high as 600 GHz.

I. INTRODUCTION

Circuits based on superconducting Josephson junctions (JJs) have wide applications ranging from signal metrology^{1,2}, low-noise amplification^{3–5}, to novel computation (superconducting super-^{6,7} and quantum- computers^{8–12}) arising from their low power consumption, the nonlinear Josephson inductance, and area quantization of the single flux quantum (SFQ) pulses they can generate. Metrology of signal waveforms generated by JJ-based circuits is challenging due to the short duration of an SFQ pulse (a few picoseconds), and the fact the circuits are embedded in cryogenic systems – precluding direct access using short cabling lengths. Despite these challenges, JJ-based samplers have successfully been used to diagnose operation of complex superconducting circuits via integration at key circuit nodes¹³.

To minimize dispersion, and thus faithfully detect JJ-generated signals, an appropriate measurement technology must be located in close proximity to the superconducting circuits. An obvious choice is to incorporate a single JJ^{14–16} or superconducting quantum interference device (SQUID)¹⁷ as a logical comparator on the same chip with the target circuitry. This strategy is beneficial in terms of ease-of-integration – the sampler can be co-fabricated on the same chip as the device under test (DUT) – and simplicity of the experimental setup. Furthermore, this strategy provides a wide parameter space for the DUT-comparator coupling in terms of strength and type – galvanic, inductive, or capacitive – which can be easily defined and fixed during the design and fabrication phases.

Electro-optic (EO) sampling strategies^{18–20} present another viable path to sampling waveforms generated by superconducting circuits and, due to the femtosecond timescale rou-

tinely available in pulsed laser systems today, can potentially offer rise times beyond that available to Nb-based superconducting samplers^{21,22}. However, a major limitation of EO sampler implementations arises from the need to incorporate an EO transduction element such as lithium- or niobium-tantalate. These transduction elements typically have large dielectric constants, e.g. $\epsilon_r = 43$ for LiTaO₃¹⁸, and are frequently coupled to the electric field in an on-chip microwave transmission line, resulting in significant distortion of the target waveform (signal). Multiple reflections of the laser pulse from the substrate's top and bottom surfaces also confound the goal of low-distortion sampling^{18,19}. A final concern is the interplay between the EO sensitivity (or signal-to-noise ratio) and laser power, which has the potential for significant quasi-particle generation and degradation of the performance of the superconducting DUT circuitry. Nonetheless, EO sampling is a demonstrated technique for measurement of JJ-generated signals – e.g. SFQ pulses²⁰.

Initial JJ sampler efforts focused on Nb-based underdamped (latching) junctions, i.e. with Stewart-McCumber parameter $\beta_C = 2\pi I_c C R^2 / \Phi_0 > 1$ ^{15,23–29}, which still hold the highest bandwidth and shortest rise time of all clearly-demonstrated sampling techniques¹⁵. In the late 1980s, a commercial sampling oscilloscope and time domain reflectometer with advertised 70 GHz bandwidth and 5 ps rise-time was developed based on this technology^{25,30,31} – however these bandwidths and rise times are insufficient for our applications targeting precision voltage metrology of circuits with rise times and pulse FWHM of $\lesssim 5$ ps. More recent efforts have been made using high temperature superconductors (HTSs)^{32,33} in attempts to leverage the increased gap frequency³⁴ to yield a faster sampler response³⁵. Because these realizations of HTS JJs were intrinsically shunted, and

either critically- ($\beta_C = 1$) or over-damped ($\beta_C < 1$), a latching comparator could not be implemented. Instead, it was necessary to incorporate additional complexity in the form of SFQ-to-dc readout SQUIDs to determine comparator switching. As we will show in Sec. III A, shunting JJs into the critically-damped regime also increases their switching time and limits the bandwidth of such a sampler. Indeed, damping in HTS JJ samplers has served to significantly reduce the achieved bandwidth compared to expectations based simply on the increased gap frequency.

The ultimate goal of our sampler development lies in voltage and waveform metrology of JJ-based circuits generating signals with characteristic timescales of a few picoseconds, so the target sampling technology must have similar rise times and dynamic bandwidths of hundreds of gigahertz – ideally faster and wider bandwidth than the target circuitry. To this end we pursue a latching JJ sampler co-located with the target-signal-generating circuits as this technology possesses the most straightforward, and flexible path to high-bandwidth, low-distortion sampling. Using NIST’s state-of-the-art JJ process using Nb electrodes and amorphous-silicon (a-Si) barriers^{36,37} we design a sampler prototype similar to [15] and demonstrate this strategy has sufficient speed for measuring circuits based on SFQ pulses.

In this paper we present both simulations and test results of sampling the picosecond-duration output waveforms of two different DUTs with all JJs realized using underdamped (latching) Nb/a-Si/Nb JJs with a critical current density, J_c , of $0.22 \text{ mA}/\mu\text{m}^2$. We demonstrate a novel technique for comparator threshold detection using a binary search that we apply in both simulation of the full sampling operation and measurement of fabricated devices. This allows us to fully simulate the entire sampling process in the same manner it is performed in the laboratory – for the first time ever in Josephson sampler technology – and enables strong agreement between our modeling and measurement results. In Sec. II we first review the operation of a latching Josephson sampler. In Sec. III we simulate a JJ sampler comprised of a single comparator with a critical current $I_c = 2 \text{ mA}$, a pulse-generating *strobe* circuit, and the circuit generating the target signal (the DUT). The first DUT that we consider outputs a step signal and the second outputs a finite-duration impulse. We implement these circuits in simulation with physically realizable components: a latching SQUID for the step signal DUT, and a Faris pulser²⁴ for the impulse generator DUT¹⁵. We will show there exists an interplay between the intrinsic sampler rise time / bandwidth and the dynamics of the DUT used to characterize it. In Sec. IV we describe our experimental setup and present cryogenic measurements of sampler devices operated at 3.6 K for both the step function and impulse DUTs. Sec. V details a first-order linear systems analysis to extract an approximate sampler bandwidth. Additional simulation and measurement details are included in the Appendices.

II. LATCHING JOSEPHSON SAMPLER OPERATION

The principle of operation of a latching Josephson sampler is shown in Fig. 1. A JJ with a large critical current, I_c^{comp} (the *comparator*) is dc-biased with current I_b^{comp} . The comparator is attached to an on-chip sampling pulse generator, the

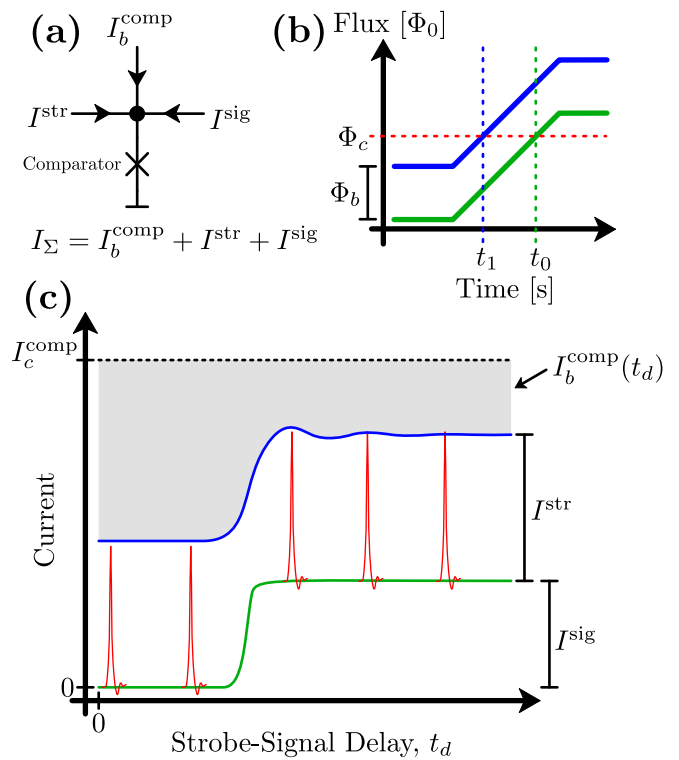


FIG. 1. Simplified description of the latching JJ sampler operation. (a) Schematic showing how a large-critical-current JJ acts as a comparator. The comparator JJ is supplied with a dc bias current I_b^{comp} from room temperature but also has current coming from an on-chip fast impulse generator I^{str} (the *sampling strobe*), and the signal current coming from the on-chip DUT, I^{sig} . Once the sum current, $I_\Sigma = I_b^{\text{comp}} + I^{\text{str}} + I^{\text{sig}}$ exceeds the comparator junction critical current, I_c^{comp} , it latches and generates an easily measurable dc voltage equal to the superconducting gap voltage. (b) Example of how a dc offset to a step-function magnetic flux-actuated strobe or DUT can be used to tune the relative delay between strobe emission and target waveform generation. For zero dc flux bias the strobe/DUT is triggered at time t_0 but when the dc flux bias is increased to Φ_b they are triggered at t_1 . (c) Cartoon diagram showing the various currents during operation. The relative timing, a delay between the strobe (red pulses) and signal (green trace) is swept using the technique shown in (b), and the sum of the strobe and signal currents varies. Here we show the strobe moving relative to the signal but in practice we hold the strobe timing fixed and *advance* the signal to traverse the strobe. At each delay I_b^{comp} is tuned so I_Σ always just exceeds I_c^{comp} and is recorded. The I_b^{comp} as a function of delay trace is thus the inverse (and offset) sampled signal (blue trace). Note that the sampled step signal (blue trace) is depicted with a shallower slope and with post-step oscillations to highlight possible artifacts resulting from the sampling measurement.

strobe, and a number of DUT circuits. The comparator and the strobe generator make up the *sampler*; where the strobe is used to selectively drive the total comparator current above I_c^{comp} at a specified time. In general, only a single DUT circuit is operated and sampled at a time. When the sum (I_Σ) of the dc bias (I_b^{comp}), the strobe current pulse (I^{str}), and the DUT signal (I^{sig}) exceeds the comparator I_c^{comp} (the *threshold*), the comparator voltage rapidly latches to the superconducting gap voltage. In this way, the entire DUT signal waveform can be sampled by changing the delay of the strobe relative to the DUT signal, as illustrated in Fig 1. The comparator remains

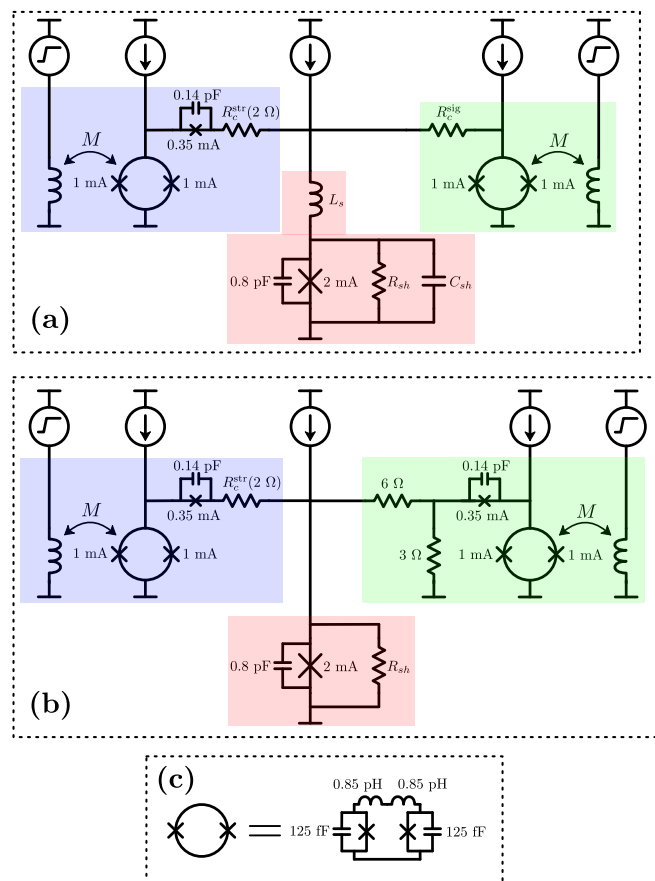


FIG. 2. Schematics of the circuits used to perform simulations, where (a) implements a latching SQUID step signal DUT and (b) uses a Faris pulser impulse DUT. The comparator and additional reactive coupling elements (Sec. III C and Appendix D) are highlighted in red, the Faris pulser strobe generator in blue, and the DUT in green. Each Faris pulser is comprised of a symmetric SQUID with 1 mA I_c SQUID JJs and a 0.35 mA I_c output JJ. The sampler is comprised of the blue (strobe) and red regions with the strobe coupled to the comparator via R_c^{sig} whose nominal value is 2Ω . We apply static current biases – corresponding to 90% of the subcircuit I_c – to the strobe, comparator and DUT, and magnetically actuate the strobe and DUT using step current pulses. M represents the mutual inductance between the flux trigger line and the SQUID loops. The strobe pulse time is held fixed and we sweep the DUT signal across the strobe pulse by varying the relative delay of the DUT trigger. All static component values are listed numerically, while all swept parameters are indicated symbolically. R_{sh} is used to explicitly tune the comparator β_C , while R_c^{sig} tunes the coupling strength of the SQUID DUT. In Appendix D we discuss the sampler response under reactive coupling by sweeping C_{sh} and L_s . (c) Circuit values for the symmetric SQUIDs.

latched at the Nb gap voltage of 2.8 mV until I_2 is dropped below the comparator return current – making it an experimentally straightforward task to both determine whether the comparator has latched and to reset it for the next sampling event. We define the interval between setting and resetting all biases, during which the strobe and DUT are triggered and the comparator is allowed to latch (depending on I_2), as a *sampling period*. Due to this required reset, the dc biases are actually square pulses.

Latching JJ samplers have historically operated with sampling periods on the order of a few microseconds inside a

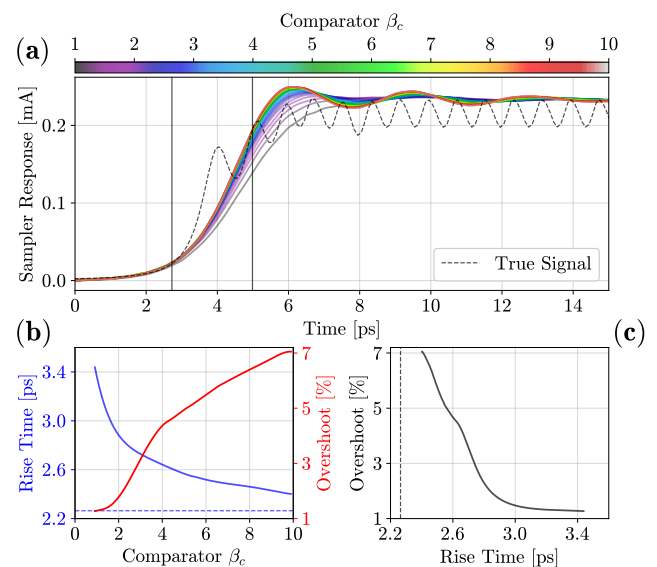


FIG. 3. Simulation of the sampler response with a step signal while varying the comparator β_C . Here β_C is tuned by sweeping the comparator's explicit shunt resistance R_{sh} . (a) Solid colored lines show the sampler output of the latching SQUID for various β_C . The black dashed line shows the simulated SQUID signal at its output node which the sampler is attempting to reconstruct. Vertical black lines show the 10% and 90% times for the SQUID signal. (b) The blue (red) line shows the sampler rise time t_r (overshoot) as a function of β_C . The blue dashed line shows the SQUID rise time, i.e. the minimum measurable t_r . (c) Illustration of the tradeoff between minimal sampled signal distortion (i.e. overshoot) and rise time. The SQUID rise time is denoted here by the black dashed line.

slower feedback loop (with integration times 0.1 s– 1 s) configured to maintain the total current into the comparator exactly at I_c^{comp} on slow timescales^{15,23,25,26,38}. A secondary bias current is typically applied at the slower timescale which sweeps the relative delay between triggering the strobe and DUT by causing one to generate its waveform slightly earlier on the rising edge of the flux pulse. Thus the sweep bias causes the strobe and signal to traverse one another at the slower integrator feedback timescale, resulting in full sampling of the target waveform at the sweep generator frequency.

Note that the purpose of the integrator feedback is to determine the change in bias required to latch the comparator at a given relative timing delay, shown as the gray $I_b^{comp}(t_d)$ region in Fig. 1, due to the value of the target signal when the strobe arrives. In this work, we omitted the sweep bias and feedback loop in favor of a digitizer and two programmable current sources. One current source is used to first set a fixed delay by setting a small added current bias to the DUT flux trigger. Then the digitizer timestream mean voltage – windowed over a portion of a single sampling period after the strobe is known to have triggered – can be used as a simple metric to determine if the comparator has latched. The second current source, supplying $I_b^{comp}(t_d)$, is dithered to determine the (e.g. 50%) latching threshold for each programmed delay. In practice we implement a binary search algorithm to determine $I_b^{comp}(t_d)$. This experimental procedure is deliberately chosen to mirror the simulation strategy described in the following section to permit us to much more accurately simulate experimentally-realized samplers³⁹.

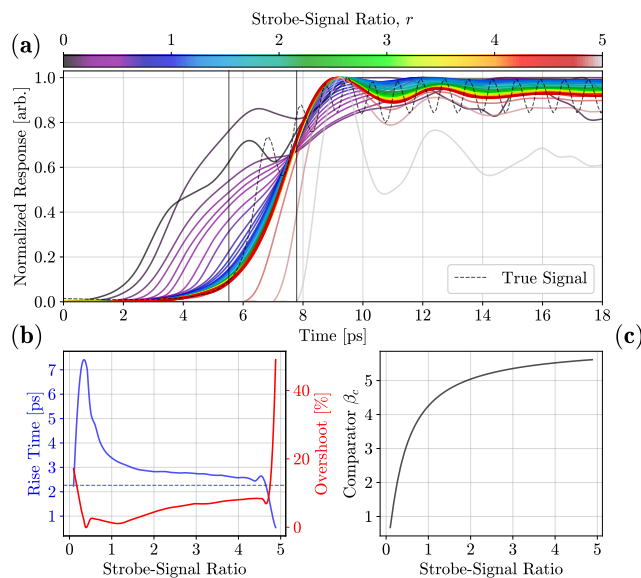


FIG. 4. Simulation of the sampler step signal response while varying the strobe-to-signal ratio (r) by tuning the signal coupling resistance, R_c^{sig} , linearly from 0.5Ω to 25Ω keeping the strobe coupling fixed at $R_c^{\text{str}} = 2 \Omega$. (a) Solid colored lines show the normalized sampled SQUID signal for various r . The black dashed line and vertical black lines show the simulated SQUID signal at its output node, and the 10% and 90% rise times, respectively, as in Fig. 3 (b) The blue (red) line shows the sampler rise time t_r (overshoot) as a function of r . The blue dashed line shows the SQUID rise time, i.e. the minimum measurable t_r . Large excursions in t_r and overshoot, resulting from significant sampled waveform distortion, are observed for extreme values of r . For $r \lesssim 1$ the strobe does not strongly determine which part of the signal to sample, and for $r \gtrsim 4.5$ the sampler response becomes a strong convolution of not just the comparator dynamics and the target waveform, but also of the strobe and its post-pulse behavior. (c) The comparator β_C as a function of r . β_C is dominated by the $R_c^{\text{str}} = 2 \Omega$ resistor, but for $R_c^{\text{sig}} \lesssim 4 \Omega$ the comparator β_C is appreciably affected by lowering the signal coupling resistance. As expected, when $\beta_C \sim 1$ the sampled response is heavily distorted due to unstable comparator latching.

III. SAMPLER PERFORMANCE SIMULATIONS

Simulations of the ideal and ultimate JJ sampler performance using a delta function strobe and zero-rise-time step signal have recently been performed^{39,40} so here we focus on physically realizable circuits and signals. To extract rise time we simulate the circuit shown in Fig. 2(a) – where the DUT is a latching SQUID. To simulate sampling of a finite-duration pulse we use the circuit shown in Fig. 2(b). For a step signal the important metrics are the 10%–90% rise time – defined as the *rise time*, t_r – and the distortion of the sampled signal – which is quantified as the *overshoot* during the initial rise in sampler signal relative to the asymptotic, or steady-state, sampler response after the SQUID has latched⁴¹. When considering the response for imaging an impulse we consider the full width at half maximum (FWHM) and the *undershoot* following the main peak to benchmark performance. In both cases there is an effective *speed limit* imposed by the intrinsic dynamics of the target signal generators beyond which the sampler cannot be characterized. For the step signal DUT this is the 10–90% rise time of the SQUID itself, and for the im-

pulse generator DUT this is the FWHM of the Faris pulser pulse directly at its output. These effects are due to the fact that the sampler output is the convolution of the comparator response and the DUT signal.

We use the WRspice circuit simulation package^{42,43} to perform our simulations and use the built-in resistive- and capacitively-shunted junction (RCSJ) model. We choose the WRspice quasiparticle model giving a quasiparticle contribution with an exponential dependence on the bias current^{6,43,44}. We use JJ parameters characteristic to our Nb/a-Si/Nb fabrication process⁴⁵ (Appendix C): a specific capacitance of $80 \text{ fF}/\mu\text{m}^2$, characteristic voltage of $I_c R_n = 1.5 \text{ mV}$, and a sub-gap resistance of 60Ω . We remove the implicit JJ shunts in WRspice and provide explicit shunts in the circuit definition when needed. To determine the threshold comparator bias at each strobe-signal delay we implement a binary search technique in which only single sampling periods at a time are simulated and comparator latching is determined by a simple voltage threshold in the absence of noise (see Appendix A).

A. Step Signal Response

First we consider the sampler dynamics when sampling the step signal created by the latching SQUID, shown in Fig. 2(a), while various circuit parameters are swept. As previously mentioned, the goal of this study is to determine optimal design considerations for a JJ sampler – specifically in terms of an ideal target for the comparator Stewart-McCumber parameter in the presence of an external coupling network $\beta_C = 2\pi I_c C_{sh,eq} R_{sh,eq}^2 / \Phi_0$, and the most favorable signal coupling method: galvanic, capacitive, or inductive. Here $C_{sh,eq}$ and $R_{sh,eq}$ are the equivalent capacitance and resistance shunting the comparator due to the addition of the connected circuits in Fig. 2. First we perform a β_C sweep, by tuning the value of the explicit comparator shunt resistor R_{sh} , and extract t_r and the overshoot from the sampled output waveform. The comparator β_C is $R_{sh,eq} = [R_{sh}^{-1} + (R_c^{\text{str}})^{-1} + (R_c^{\text{sig}})^{-1}]^{-1}$, and is thus effectively bounded above by $R_c^{\text{str}} = 2 \Omega$ for our case. Results of this simulation sweep are shown in Fig. 3 and reveal a clear tradeoff between minimal distortion sampling of the SQUID signal and the rise time. Indeed, low-distortion sampling – corresponding to an overshoot of $< 1\%$ – requires a nearly critically-damped comparator. Given the weaker relation between β_C and t_r it is more favorable to enforce $\beta_C \lesssim 3$, as this is effectively the “knee” in Fig. 3(b,c) above which small gains in rise time result in significant distortion of the signal when sampled.

The next obvious question in Josephson sampler design is how large the relative amplitudes of the strobe and signal should be. Previous Josephson sampler implementations^{23,24,35} have operated with strobe-to-signal ratios, $r = I^{\text{str}}/I^{\text{sig}}$, from unity to over 10 – with the most successful sampler¹⁵ possessing two DUTs with strobe-to-signal ratios of ~ 1.8 and ~ 3 . To determine the sampler response as a function of the strobe-to-signal ratio we choose the coupling resistor R_c^{sig} as our free parameter and conduct a rise time simulation, as detailed above, and with $R_{sh} = 2 \Omega$ (maximum $\beta_C = 5.6$). For these simulations, because we sweep R_c^{sig} over an order of magnitude, the amount of SQUID bias current which branches upon latching of the SQUID and is

then injected into the comparator is significant. This reduces the amplitude of the signal current relative to the full range of comparator bias needed to ensure I_{min} never latches the comparator while I_{max} always latches. To compensate for these effects we peak-normalize the sampler output for each R_c^{sig} trace.

Fig. 4 shows the simulated sampler output while varying r . Significant signal distortion and degradation in the rise time is evident in Fig. 4(a) for $r \lesssim 1$. Additionally, for $r \gtrsim 4.75$ we see that the sampler is unable to reconstruct the target signal with appreciable fidelity. This is due to the finite, non-zero tail produced by Faris pulsers, i.e. the strobe, implemented with large sub-gap resistance JJs⁴⁶. When the relative height of the strobe's post-pulse tail is approximately equal to the SQUID DUT signal amplitude the sampler instead attempts to measure both the target waveform and the strobe pulse tail simultaneously. Our cutoff of $r \sim 4.75$ indicates the post-pulse tail amplitude is approximately 1/5th the peak pulse height, which is in good agreement with the strobe Faris pulser output seen in simulation. Clearly, for our implementation, the strobe-signal ratio has an optimum value of 2–3 as this optimizes the rise time while allowing variation in r without compromising performance.

1. High Current Density JJs: Faster DUTs and Sampler

The extracted sampler rise times in the simulations in Sec. III A are a result of the convolution of the sampler response and the finite-width of the SQUID DUT step-function output³⁵. The sampler response is limited by the comparator dynamics and the finite-width of the strobe pulse; both can be improved by increasing the ratio of the critical current to junction capacitance, as shown elsewhere^{16,39,40,47,48}. The rise time of the SQUID DUT output is limited by the SQUID β_c ^{29,40} and both the L_{SQ}/R and RC rise times. The relevant resistances for R are both the SQUID normal resistance and the DUT-comparator coupler R_c^{sig} .

Here we explore the feasibility of creating a real circuit (DUT) which could be used to measure the true ultimate rise time of the comparator. Namely we explore avenues to increase the SQUID latching speed, while making no changes to the comparator+strobe (sampler) circuit, and test whether we can observe improved sampled rise times compared to those presented in Sec. III A. Decreasing the SQUID self-inductance, L_{SQ} , and JJ capacitance yields a significantly faster SQUID response. In our simulations we can reduce the SQUID switching time by over a factor of 4.5, resulting in a 10%–90% rise time of 0.47 ps, by lowering L_{SQ} to 0.19 pH and the SQUID JJ capacitance to 50 fF. These values are a reduction by a factor of 10 and 2.5 relative to L_{SQ} and C_{JJ} used in Sec. III A, respectively. Both reductions are physically possible by (a) moving to a geometry where the SQUID loop axis is in the plane of the substrate rather than orthogonal¹⁵, and (b) varying the JJ process critical current density³⁶ at fixed specific capacitance (80 fF/ μm^2).

We simulated the sampled rise time of this faster SQUID DUT, fixing L_{SQ} at 0.19 pH and sweeping the SQUID J_c while the sampler circuit remained unchanged (J_c held fixed at 0.2 mA/ μm^2). In WRspice⁴² this is accomplished by fixing I_c and sweeping the JJ self-capacitance – i.e. a JJ fabricated

in a higher J_c process will have a smaller area for a fixed I_c and thus a smaller capacitance. Fig. 5 shows the results of this “multi- J_c ” device with a comparator β_c of 10 (fastest sampler response of Fig. 3). We observe from these results that, even with the SQUID J_c a factor of two below our original design point of 0.2 mA/ μm^2 , the reduction in L_{SQ} still allows us to *measure and demonstrate* a sampler t_r which is faster than that obtained in the simulations of Sec. III A; note however, that without changing the sampler circuit parameters, the minimum measured rise time is ~ 1.9 ps even with a SQUID rise time of ~ 0.5 ps. Thus we may interpret these results as revealing the intrinsic sampler rise time is approximately 1.9 ps

The dependence of the minimum quantifiable sampler rise time on the SQUID J_c is nontrivial and is actually deleterious once the SQUID J_c exceeds ~ 0.3 mA/ μm^2 . I.e., the most fruitful path to produce a DUT whose rise time is less than the intrinsic comparator capability, and guarantees we may fully explore this contribution to the sampler's t_r , is to reduce the SQUID self-inductance. Of course, care must be taken to produce DUTs whose response is fast enough that the ultimate limiting behavior of the sampler (and not the DUT-sampler system convolution) may be faithfully characterized. Co-fabricating a DUT with a higher J_c than that of the comparator is purely a technique for extracting the intrinsic sampler rise time and bandwidth, at a cost of more processing steps, and is not of large practical import.

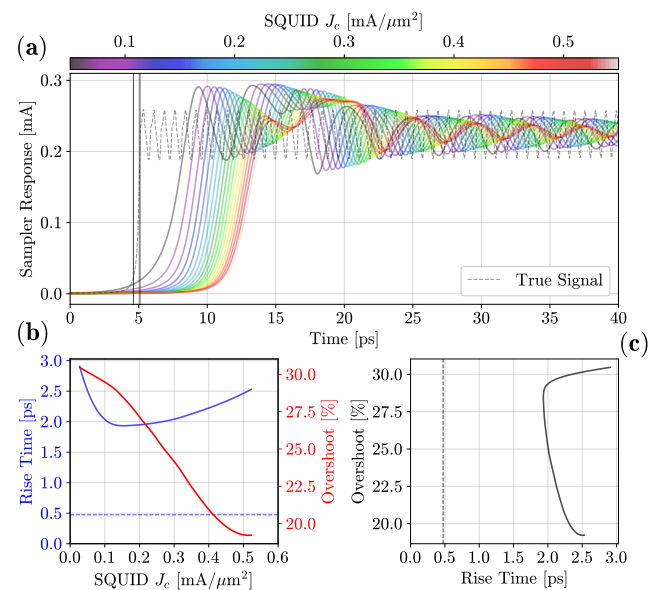


FIG. 5. Multi- J_c process sampler simulation results. We increase the SQUID latching speed by reducing L_{SQ} to 0.19 pH and then sweep the J_c of only the SQUID JJs. The comparator Stewart-McCumber parameter is held at $\beta_c = 10$. (a) Solid colored lines show the sampled SQUID signal as a function of the SQUID J_c . The black dashed trace shows the simulated SQUID signal at its output node for the highest J_c of 0.5 mA/ μm^2 . Vertical black lines show the 10% and 90% times for the SQUID signal. (b) The blue (red) line shows the sampler rise time t_r (overshoot) as a function of J_c . The blue dashed line shows the SQUID rise time, i.e. the minimum measurable t_r . (c) Signal distortion (overshoot) as a function of t_r . The SQUID rise time is denoted here by the black dashed line.

B. Finite Impulse Response

To conclude our design studies of latching JJ samplers we focus on the sampler's finite impulse response – in this case realized using a Faris pulser identical to the strobe generator and coupled to the comparator using a current divider comprised of a $6\ \Omega$ series resistance, and $3\ \Omega$ parallel resistance to ground. The current divider is chosen to make β_C for the Faris pulser DUT and strobe approximately the same while enforcing a strobe-signal ratio of ~ 2 . Here we perform a single comparator β_C sweep and characterize the reconstructed waveform FWHM and undershoot. Fig. 6 shows a much higher sensitivity to signal distortion at the sampler output relative to the SQUID DUT step signal response case. While the sampled Faris pulser pulse FWHM is nearly static as β_C is tuned, significant improvement in distortion is achieved when the comparator is close to critically damped.

C. Reactive Coupling

Leveraging the learnings of Sec. III A we conclude that an optimally flexible JJ sampler, capable of reconstructing the fastest signals with minimal distortion is achieved when $\beta_C \sim 1\text{--}4$ and with a strobe-signal ratio of 2–3. However, this is in the case of *galvanically*-coupled DUTs. It is certainly possible to *reactively*-couple the DUTs using either capacitors in parallel or inductors in series with the comparator (C_{sh}

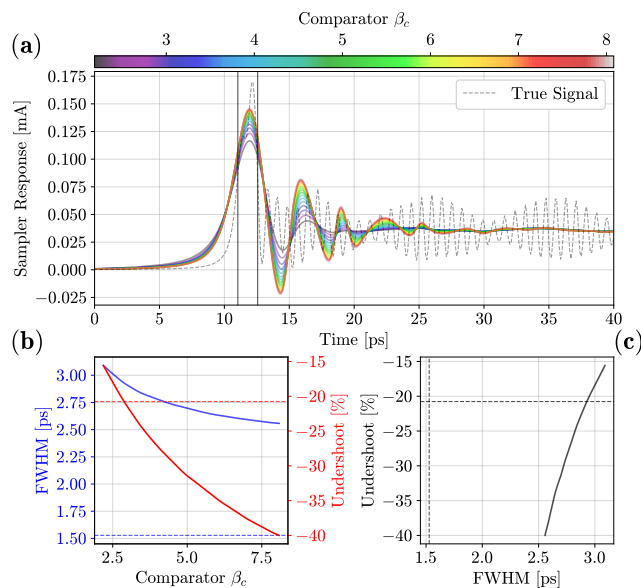


FIG. 6. Sampler response simulation versus comparator β_C while sampling the output of a Faris pulser DUT coupled to the comparator via a $6\ \Omega$ series, $3\ \Omega$ to ground current divider. (a) Sampled Faris pulser response as a function of β_C (solid colored lines). The dashed black line shows the ideal pulse while the vertical black lines show the half-maxima values. (b) Sampled pulse FWHM (blue) and undershoot (red). The undershoot is calculated as the largest excursion after the main pulse below the asymptotic response – which is then normalized by the primary peak height. Dashed lines indicate the values intrinsic to the ideal Faris pulser signal. (c) Relation of the sampled pulse FWHM and its undershoot. The dashed vertical (horizontal) line shows the intrinsic pulse FWHM (undershoot).

and L_s in Fig. 2(a)). Such a coupling scheme is attractive in scenarios where the sampler and DUTs are housed on separate chips – such as a scanning SQUID sampler⁴⁶ or in the case of a flip-chip bonded sampler-DUT multi-chip-module. However, bounds on the magnitudes of the reactive couplers need to be established from a perspective of shortest rise time/ highest bandwidth and minimum signal distortion. Intuition suggests that the couplers should behave as small perturbations to the comparator – i.e. by only weakly modifying its β_C , RC time, or L/R time. Indeed, the results of our simulations (detailed in Appendix D) place upper bounds on the coupler capacitance and inductance of $\sim 1\ \text{pF}$ and $\sim 1\ \text{nH}$, respectively, which corresponds almost exactly to the values of the comparator JJ self-capacitance and its Josephson inductance. Despite these relatively small limits on coupler reactance, sufficient signal coupling is possible at these levels due to the speed of the signals of interest.

IV. EXPERIMENTAL RESULTS

A. Device Design, Fabrication, and Packaging

As a launching point for developing a flexible JJ sampler technology for waveform metrology and diagnostics of SFQ digital logic circuits, we fabricated a sampler using unshunted amorphous silicon barrier (Nb/a-Si/Nb) JJs with a critical current density of $J_c = 0.22\ \text{mA}/\mu\text{m}^2$. The fabricated circuit is shown in Fig 7(a) and the packaged $1\ \text{cm} \times 1\ \text{cm}$ chip is shown in Fig 7(b). We select this junction technology due to its potential to scale to significantly higher J_c , a critical parameter in increasing latching junction operating speed^{40,47}, when compared to more common Nb/Al-AIO_x/Nb JJs^{36,49}.

The chosen topology is shown in Fig 7(c) and is similar to [15]. The sampler circuit is comprised of four primary components: the comparator ($I_c^{\text{comp}} = 2.21\ \text{mA}$), a strobe pulse generator, a step signal DUT, and an impulse generator DUT. The strobe pulse and impulse generator DUT are realized using Faris pulsers²⁴, consisting of a two-junction, symmetric dc SQUID (single junction $I_c = 1.11\ \text{mA}$), and a smaller output pulser junction with $I_c = 385\ \mu\text{A}$. The SQUIDs comprising the Faris pulsers are identical to the SQUID DUT. The strobe and DUT signals are triggered using fast current pulses carried to the sampler circuit on high-bandwidth lines (coaxial cables off-chip, CPW on-chip). Further fabrication details may be found in Appendix C. Including all coupling resistors ($R_{sh,eq} = 0.9\ \Omega$), and using fabrication parameters stated in Sec. III, we obtain an expected comparator $\beta_C = 4.56$ for the fabricated devices.

The sampler die is soldered using 52In/48Sn solder^{50–52} inside a copper enclosure which is mounted on the second stage of a Gifford-McMahon-cooled cryostat and operated at 3.6 K. The device package possesses four high speed lines, used for applying flux trigger pulses, and 14 low-speed current bias and voltage tap leads. High speed lines exit the package via SMP connectors and are converted to SMA-connectorized semi-flex and rigid coaxial cables. We thermalize the flux trigger lines using 10 dB attenuators at 3.6 K. All low-speed lines are combined in a multi-wire cryogenic loom and are thermalized with two sets of $100\ \Omega$ series resistors at 3.6 K. Additionally a set of on-chip $100\ \Omega$ series resistors are fabricated as a

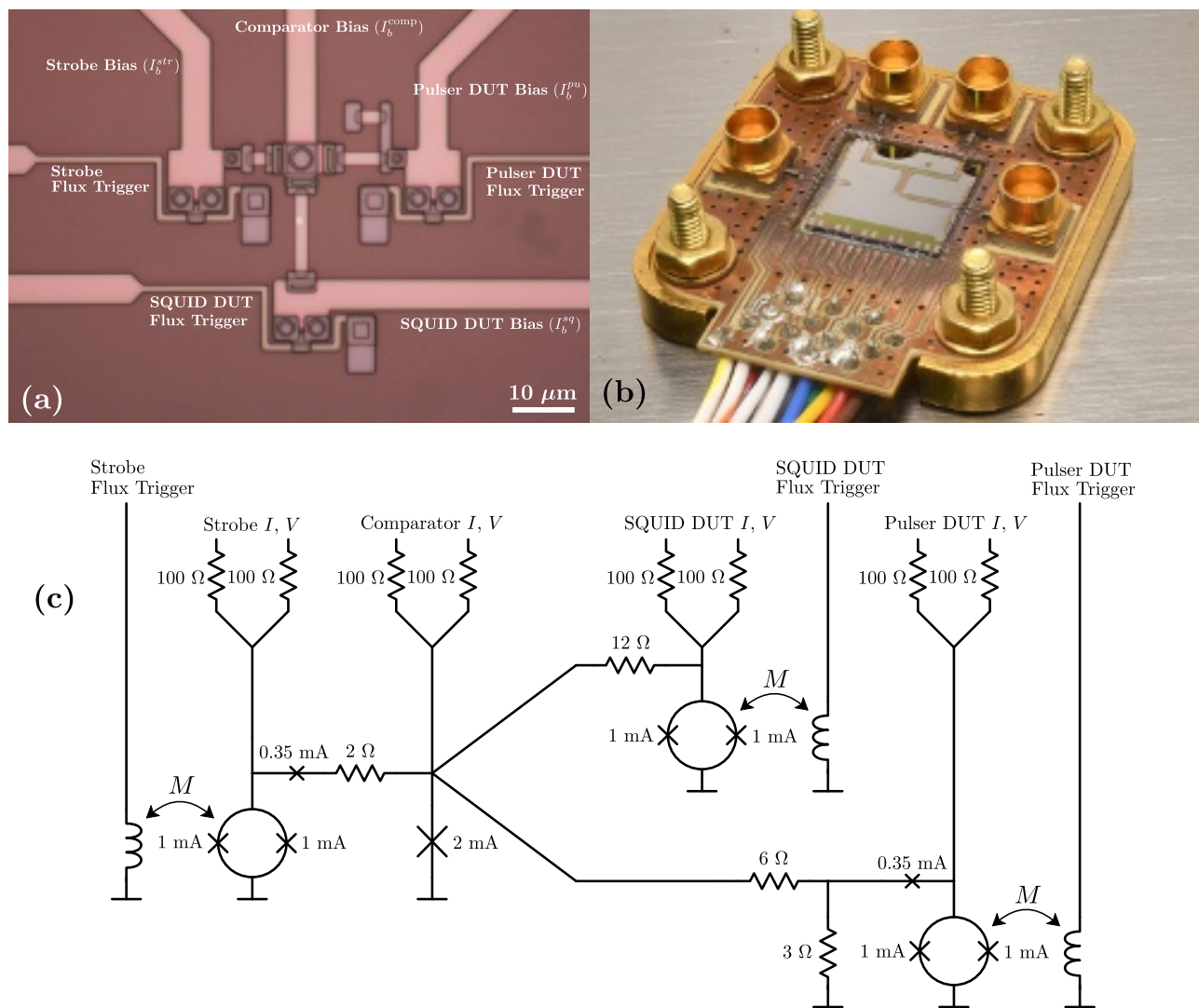


FIG. 7. (a) Micrograph of the sampler with dc bias and high-speed flux trigger lines denoted. Photo is taken immediately prior to lithography and deposition of the final insulator layer and sky plane. (b) Photo of a packaged (copper box lid removed) sampler device die showing the high-speed flux trigger SMP connections, dc signal lines, and wirebond interconnects. The $1\text{ cm} \times 1\text{ cm}$ sampler chip is PdAu backside-metallized and InSn-soldered directly to the package's copper bottom. (c) Electrical schematic of the sampler. Each dc bias lead and voltage tap have an on-chip $100\ \Omega$ bias and thermalization resistor to mitigate thermal current noise. The three flux trigger lines, brought in on high-bandwidth coaxial cables (20 GHz) and SMP connectors, are thermalized with 10 dB attenuators on the cryostat's 3 K stage. These flux triggers are supplied using step function voltage pulses from a multichannel, high-speed AWG (65 GSa/s, 25 GHz analog bandwidth).

final thermalization step and to create a stiff current bias in proximity to the sampler subcircuits.

B. Experimental Setup

Our choice of Nb/a-Si/Nb JJs permits operation over a wide temperature range thanks to the temperature-insensitivity of I_c for this JJ technology – which is reduced to half its asymptotic low-temperature value (i.e. below 4 K) at around 7 K^{11,36}. Power dissipation ($P = I_c R_n$) becomes the primary consideration for sampler operation in terms of the low-temperature bound and limits operation of samplers using JJs with an I_c of order 1 mA to around 1 K. Samplers using lower I_c JJs may easily be constructed to permit operation at dilution refrigerator temperatures^{10,53,54}.

We apply current biases using a series of low-speed (1 GSa/s) AWGs configured to output square voltage pulses at a frequency of 20 kHz, with edge times of $30\ \mu\text{s}$, and a duty cycle of 0.8. The strobe and DUT flux triggers are supplied using step function voltage pulses from a multichannel, high-speed AWG (65 GSa/s, 25 GHz analog bandwidth). Discarding the bandwidth limit of cabling and interconnects, this means the trigger pulse rise time is of order 15 ps. Delay (advancement) of the firing time of the DUT relative to the strobe is accomplished by applying a negative (positive) dc level to the flux trigger by means of a dc voltage source, bias tee, and mechanical phase shifter (delay line)¹⁵. In our case we apply flux offsets to advance the DUT while the strobe trigger time is held constant. As a dc flux bias reduces the critical current of the SQUIDS in the DUTs and strobe, this technique

is limited in the maximum strobe-DUT *traversal* of approximately 30–100 ps; depending on the proximity of I_b^{sig} to I_c^{sig} (less traversal is possible the higher the DUT bias). For timing calibration and system tuneup we operate the strobe and DUT triggers on independent channels, allowing us to program arbitrary strobe-DUT delays and determine optimal alignment parameters for the flux trigger waveform data. In this configuration we treat the flux trigger AWG sample clock as a master timing reference and perform a delay calibration of the mechanical delay line. Next, and to eliminate channel-to-channel jitter, we move to single output configuration where the strobe and DUT flux triggers are split with a power divider at the AWG output (with the bias tee and delay line following the divider for the DUT trigger line).

Rather than adopt the analog approach of historical JJ sampler demonstrations using a slow feedback loop, we implement a fully digital system for acquiring DUT waveforms using our sampler device. The comparator voltage is captured on a 125 MSa/s digitizer and we implement the same binary search algorithm used in our simulations³⁹. The data from the full sampling period is post-processed to select the trace segment known to follow the arrival of the flux triggers, and use this voltage to determine if the comparator has switched for a given bias. Implementation of the binary search is thus straightforward with the single caveat that, in the presence of noise, we must collect multiple sampling events and enforce a switching probability threshold for each programmed strobe-signal delay (dc flux offset). Empirically, we find 1000 sampling events and a switching probability threshold of 0.5 to provide high-quality, repeatable sampled waveforms. With these settings and 10 binary search steps, the acquisition time is ~ 1 s per commanded delay – limited by data transfer and post-processing. The advantage of this technique is that it directly mirrors the sampling process as performed in simulation, facilitating strong agreement between simulated and measured results.

C. Sampled Waveforms: DUT Current Bias Sweep

After initial tune-up and dc characterization of the device subcircuits (Appendix B), we perform a series of sweeps to fully explore the sampler and DUT dynamics. We begin by selecting a fixed strobe current bias of 2.2 mA; close to its practical maximum of $I_c^{\text{str}} = 2.21$ mA to provide the sharpest strobe pulse^{40,55}. Noise- and thermal-oscillation-induced spurious switching is not present in our sampler even with the strobe bias this close to its critical current via sufficient filtering of the bias lines and the negligible temperature sensitivity of Nb/a-Si/Nb at 3.6 K³⁶. We then sample the SQUID DUT waveform for a variety of DUT current biases. All of the sampler measurements presented in Fig. 8 and Fig. 10 were collected by advancing the DUT relative to the strobe.

Calibration of the delay as a function of the flux trigger offset voltage (i.e. in ps/V corresponding to the signal advancement as depicted in Fig. 1(b)) is performed as in [15] using a mechanical delay line (phase shifter). This procedure involves sampling the DUT (at fixed current bias) waveform at two different delay line settings and measuring the separation between the curves, in flux offset voltage units, corresponding to the known delay induced by the two shifter positions. Us-

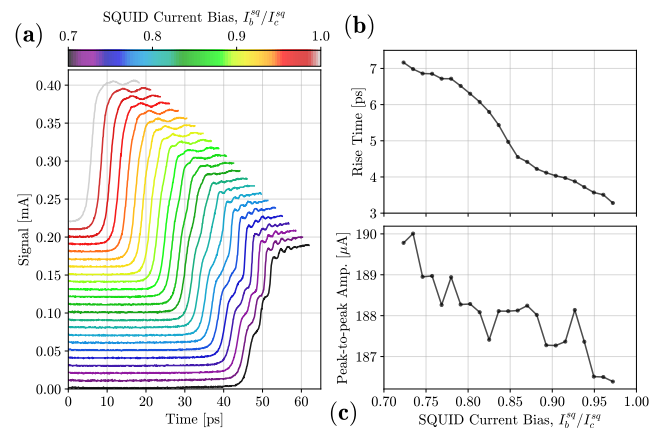


FIG. 8. Measured SQUID DUT signal and characteristics as a function of SQUID DUT bias, I_b^{SQ} . The strobe bias is fixed at 2.2 mA, slightly below its I_c of 2.21 mA. (a) Sampled waveforms with each successive curve offset vertically by $10 \mu\text{A}$ for clarity. The time at which the SQUID latches moves to earlier times (smaller strobe-to-signal delay) as I_b^{SQ} increases, so this horizontal shift is real. As the SQUID bias is ramped and crosses $I_b^{\text{SQ}}/I_c^{\text{SQ}} \approx 0.85$ we observe a transition between two distinct oscillation frequencies of ~ 580 GHz to ~ 180 GHz. (b) Measured sampler rise time as a function of the SQUID DUT bias current. (c) Sampled SQUID DUT signal amplitude as a function of the DUT bias current.

ing this technique the delay, per volt applied as a flux offset, may be known to sub-picosecond levels. This delay calibration is linear and reproducible with respect to the full range of applied DUT trigger dc flux offsets used to gather the sampled waveforms shown in Fig. 8 and Fig. 10. We obtain a constant value of 17.8 ps/V using a 1 kΩ current-defining resistor. See Fig. 16 in the appendix for more details.

In Fig. 8 and Fig. 10, the sampled waveforms each have approximately 600 points over a span of 40–60 ps. At each point the sampler performs a binary search depth of 10, where each binary step consists of 10^3 comparator decisions, for a total of 10^4 comparator decisions made for each signal data point. The full scale search range selected for these signal data was $300 \mu\text{A}$, which gives a current resolution of ~ 300 nA. To characterize repeatability and uncertainty of these measurements, we sampled and recorded several complete signal waveforms with identical settings for all control parameters. At each programmed delay we calculate the Type A uncertainty⁵⁶ for the signal values. On the steepest regions of the curves corresponding to the largest uncertainty, we determine the DUT current Type A uncertainty for a 95% confidence interval ($\pm 2\sigma$) of $\pm 1.2 \mu\text{A}$ ($k = 2$). This is a relative uncertainty of $\sim 0.6\%$ in Fig. 8 and $\sim 1.2\%$ in Fig. 10. The error in the commanded delay arises from the uncertainty in the delay-to-dc-flux-offset calibration applied to the DUT flux trigger line. These uncertainties result in an expansion or compression of the waveforms by less than 0.3%.

The family of sampled waveforms for the latching SQUID are shown in Fig. 8. At low DUT bias the sampled waveform shows two “bumps” in the rising edge of the step waveform that disappear with increasing I_b^{SQ} . Fast oscillations near the top of the rising edge also disappear and are replaced with slower oscillations. We may quantify the frequency of these oscillations by performing a polynomial and sinusoidal fit to

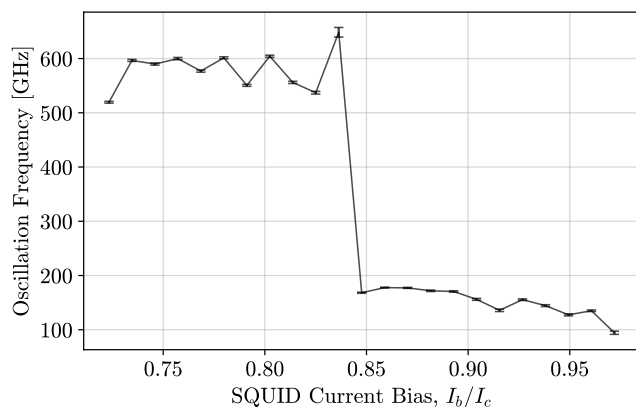


FIG. 9. Extracted oscillation frequency as a function of the SQUID DUT bias current. The frequency is determined via a fit to the signal above the 90% level using Eq. (1). Error bars correspond to the fit standard error for f .

the signal above its 90% threshold via

$$S(t) = c_0 + c_1t + c_2t^2 + c_3t^3 + c_4 \sin(2\pi ft + \phi). \quad (1)$$

Fig. 9 shows the behavior of the SQUID DUT's oscillations as a function of its current bias. From this we see the comparator responds to oscillating signals with periods shorter than the extracted rise time of ~ 3.5 ps; demonstrating our sampler is sensitive to signals in excess of 600 GHz. In this case, the measured value of the sampler t_r is in fact partially limited by the SQUID DUT dynamics and its intrinsic rise time (as discussed in Sec. III A 1). Indeed, finite sensitivity to signals up to the superconductor gap frequency is expected as, in order to support voltages in a superconducting environment or across JJs, quasiparticles must be present. The natural cutoff for these quasiparticle excitations is the gap frequency of the superconductor.

These results, notably for DUT current biases of $I_b^{SQ}/I_c^{SQ} > 0.85$ are in good agreement with oscillations sampled in [15]. The physical dynamics giving rise to the two oscillation frequencies arise from the small delay in latching time of each of the SQUID junctions – which in turn is a function of the SQUID bias and decreases as the bias increases (see Appendix G). This time delay, ranging from 1.1 ps to 0.7 ps (from low to high bias), causes an appreciable beat oscillation between each SQUID JJ, which is detectable by our sampler even though this frequency is above the sampler bandwidth as extracted using a linear systems treatment. At high bias, the observed oscillations are reduced in frequency and are due to intrinsic oscillations of the underdamped comparator.

Next we perform the same measurement as above, but this time with the Faris pulser DUT. The strobe bias is again held at 2.2 mA and we sample the pulser DUT signal as a function of its bias current I_b^{pu} . These results, in tandem with the fast oscillations shown in Fig. 8(a), demonstrate the intrinsic response time of the sampler is actually faster than what is extracted via the 10%–90% rise time while sampling the SQUID DUT. Again we observe features on faster timescales than the minimum t_r shown in Fig. 8(b) and whose dynamics change as a function of the impulse DUT bias – demonstrating they are sourced by the DUT and are not resulting from the convolution of the comparator dynamics. This is further

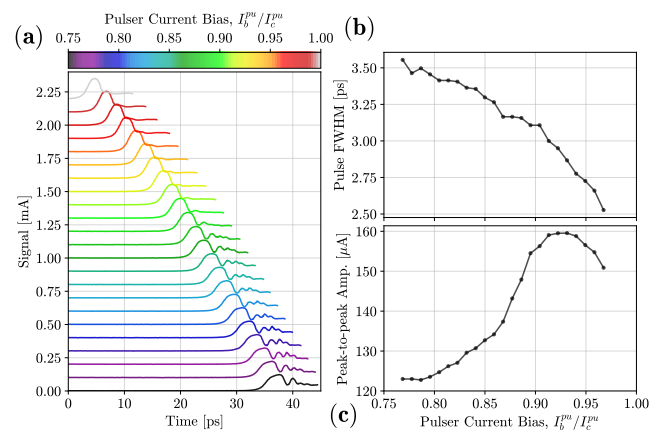


FIG. 10. Measured Faris pulser DUT signal and characteristics as a function of pulser DUT bias, I_b^{pu} , using a strobe bias of 2.2 mA. (a) Sampled waveforms with each successive curve offset vertically by $10 \mu\text{A}$ for clarity. As in Fig. 8 the horizontal shift of each curve is a physically real effect, i.e. the pulse is emitted at earlier times as I_b^{pu} is increased. (b) Measured pulse FWHM for the sampled waveforms vs. normalized pulser DUT bias current I_b^{pu}/I_c^{pu} . (c) Sampled pulser DUT signal amplitude as a function of I_b^{pu} .

evidenced by the fact the measured pulser DUT amplitude increases, reaches a measured maximum, and then begins to decrease – while the FWHM monotonically decreases with increasing I_b^{pu} . Similar to the variation in the sampled oscillation for the step signal DUT, the reduction in FWHM is the result of a reduction in the time delay between the switching of the two JJs comprising the SQUID of the Faris pulser. As the time between each JJ switching event is minimized, the pulse amplitude is expected to monotonically increase. Our observation of a maximum pulse amplitude at $I_b^{pu}/I_c^{pu} = 0.925$, corresponding to a DUT FWHM of 2.8 ps, shows this is the regime where the intrinsic speed of the comparator is exceeded by the speed of the pulser DUT signal. Beyond this point the reduction in the sampled DUT FWHM is expected as, at this point, the sampler has entered the regime of a bandwidth-limited detector.

V. SAMPLER BANDWIDTH

The 3 dB bandwidth, $B_{3\text{dB}}$, of the sampler may be approximated using the measurements in the previous section by treating the sampler as a first-order linear system⁴¹. We perform this analysis on the data in Fig. 8 and Fig. 10 where the strobe current bias is held fixed as each DUT current bias is swept. To extract $B_{3\text{dB}}$ we compute the transfer function corresponding to each I_b^{str} and I_b^{SQ} trace by Fourier transforming the sampled response and locating the point where the transfer function drops by 3 dB from its dc value. In our case, we choose the dc value to be the lowest frequency in the transfer function. Due to the steep rolloff in the transfer function no windowing is necessary to suppress ringing at high frequencies. As the SQUID DUT traces are of non-uniform length the data must be zero-padded so each record has a length equal to the longest un-padded trace. Additionally, because the transfer function applies only to periodic (or finite-duration) pulses, we differentiate the SQUID DUT data

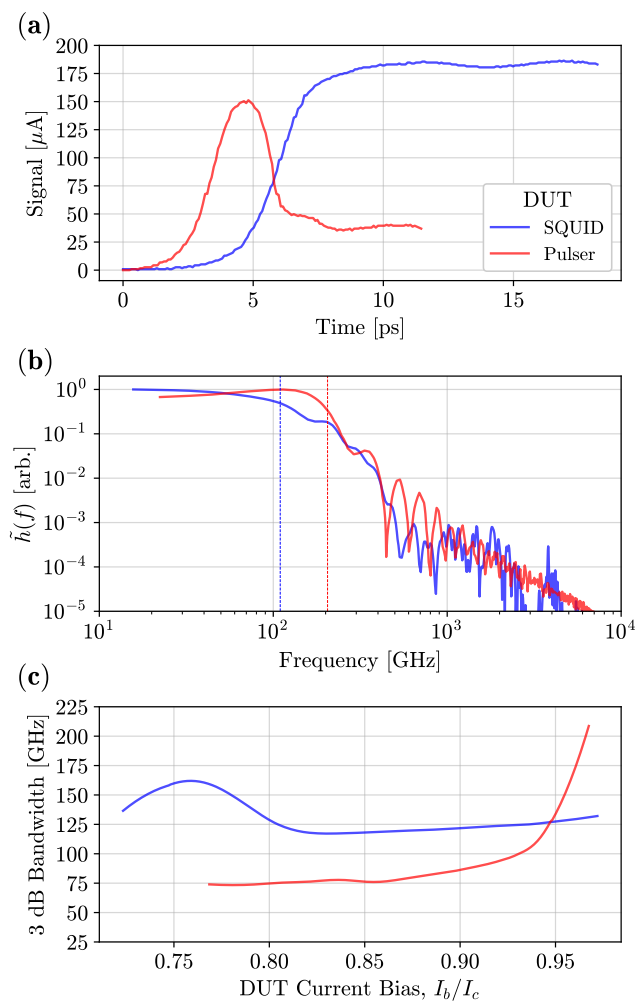


FIG. 11. (a) Highest DUT current bias sampled waveforms of Fig. 8 and Fig. 10 corresponding to I_b/I_c of 0.98 (0.97) for the SQUID (pulser). (b) Measured convolved sampler transfer function, $\tilde{h}(f)$, (in units of power spectral density scaled to the dc power) using the Fourier transform of the two traces in (a). Dashed lines denote the extracted 3 dB bandwidth in each case. This measurement yields an estimate of the sampler intrinsic transfer function as it provides the convolution of the DUT signal with the sampler transfer function. (c) Dependence of the 3 dB bandwidth on the DUT current bias.

after zero-padding. Neither procedure is needed for the pulser DUT bandwidth extraction⁴¹.

Fig. 11 shows the results of this analysis. Note that, because the DUT signals are not infinitely sharp, these measurements extract the convolution, $\tilde{h}(f)$, of the DUT signal with the sampler's true transfer function, $h(f)$. We observe that $B_{3\text{ dB}}$ is clearly not saturating at the highest DUT biases (narrowest pulses and fastest rise time step signals), which demonstrates a lower bound of 175 GHz for the intrinsic sampler bandwidth. This agrees well with the fitted oscillation frequencies in the sampler reconstruction of the SQUID DUT waveforms as a function of DUT bias (Fig. 8) and, were it possible to realize a sharper Faris pulser DUT pulse, would be expected to display a rolloff near 600 GHz. While it is true that the system dynamics are still increasing even at the highest DUT biases measured, it is not possible to further increase the bias and still fully sample the target waveform. This is because the dc flux

offset delay technique also reduces the DUT critical current and, for a given I_b/I_c , this sets a limit on how much the DUT may be advanced before it latches during the set bias phase of the sampling period.

VI. CONCLUSIONS

We have performed detailed simulations using a novel binary search threshold detection algorithm to understand the critical design criteria for optimizing the performance of a JJ-based sampler realized via a single latching comparator junction and two galvanically-connected DUTs: a latching SQUID and Faris pulser. The JJ parameters chosen in simulation closely match those observed using NIST's 0.2 mA/ μm^2 J_c Nb/a-Si/Nb JJ process³⁶. Using the latching SQUID DUT to provide a step signal we establish bounds on the expected intrinsic sampler rise time to be approximately 2.4–3.4 ps. With the Faris pulser we find the minimum pulse FWHM the sampler can resolve is 2.5–3.0 ps. Via full simulation of the sampling process we reveal a tradeoff between a small increase in the sampler speed at the expense of significant ($\gtrsim 10\%$ peak signal amplitude) distortion when pushing to the lower limit of t_r (FWHM) by increasing the comparator β_C . Exploration of the relative coupling strengths of the strobe pulse and DUT signal, r , showed a relative narrow optimum range of $r \in [1, 4]$. In these simulations we note that the fastest response (minimum t_r and FWHM) is, in some cases, limited by the DUT dynamics and not those of the comparator. Using a SQUID DUT model optimized to provide a 0.47 ps 10%–90% rise time, we demonstrate the comparator speed limit is actually expected to be 1.9 ps for the 0.2 mA/ μm^2 process. We also simulated capacitive and inductive DUT-comparator coupling schemes (Appendix D) to determine upper bounds on the coupler capacitance and inductance below which the sampler performance (bandwidth, signal distortion) is not significantly compromised.

As an experimental realization of JJ sampler technology, we have designed and fabricated a latching Josephson sampler galvanically-connected to two DUTs using our modern JJ tri-layer process with niobium electrodes and amorphous silicon barriers (Nb/a-Si/Nb). Waveforms of both DUTs were experimentally measured at 3.6 K using the same binary search technique employed in simulation, each as a function of DUT and strobe bias. Our experimental results are in good agreement with simulation and showed the fastest response corresponding to a rise time and FWHM of 3.3 ps and 2.5 ps when measuring the SQUID and Faris pulser DUTs, respectively. These values correspond to the rise time and FWHM for sampled waveforms with the sampler operating in a distortion-minimizing state (high strobe bias, see Appendix E). A linear-systems analysis of the sampled SQUID and pulser waveforms yield a sampler bandwidth of 160 GHz and 210 GHz, respectively. However, we measure oscillatory signals above 600 GHz which transition to a lower frequency as DUT bias is increased. This dependence on DUT bias indicates the oscillations source from the DUT itself and are thus a real component of the signal rather than an artifact of the comparator dynamics convolved with the true signal. Observation of these high frequency signals both supports the assertion that our characterization of the intrinsic sampler speed limit is limited by

the DUT circuits, not the comparator, and demonstrates potential bandwidth capabilities well beyond the previous in-field demonstrations. This simulation framework and laboratory demonstration provides a concrete path forward for ultra-fast and high-precision on-chip waveform metrology for superconducting electronics.

VII. SUPPLEMENTARY INFORMATION

Descriptions of additional experimental and fabrication details, procedures, and methods – as well as further simulation studies – may be found in the Supplement.

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DATA AVAILABILITY STATEMENT

The data that support the findings of this study are openly available in *Josephson Samplers: Optimal Design and Demonstration* at <https://datapub.nist.gov/od/id/mds2-3649>, with DOI doi:10.18434/mds2-3649.

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