Low-resistance contacts for p-type monolayer tungsten diselenide transistors using metallic layered $Nb_{0.3}W_{0.7}Se_2$

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Abstract. Achieving low contact resistance is a critical challenge in the development of p-type transistors that use monolayer transition metal dichalcogenides, such as tungsten diselenide (WSe_2), as their channel material. Contacts made with high work function metals require deposition at high temperatures, which typically creates defects or strain at the metal–channel interface. One solution is to use metallic two-dimensional (2D) materials that have atomically flat surfaces and can be deposited at low temperatures, as have been reported for n-type semiconductors. However, the comparatively large bandgap of WSe_2 has hindered experimental progress with p-type transistors. Here we show that metallic layered $Nb_{0.3}W_{0.7}Se_2$ can be used to create contacts for monolayer and bilayer WSe_2 field-effect transistors with channel lengths down to 100 nm. Our 2D–2D contacted field-effect transistors exhibit on-current densities of up to 358 $\mu A\ \mu m^{-1}$ and 1.1 $mA\ \mu m^{-1}$ on monolayer and bilayer WSe2 channels, respectively. In combination with scaled gate dielectrics (effective oxide thickness of 1.3 nm), the fabricated 2D–2D contacted monolayer WSe_2 devices achieve a subthreshold swing of 88 $mV\ dec^{-1}$.

Monolayer (ML) semiconducting transition metal dichalcogenides (TMDs)—such as molybdenum disulfide (MoS_2), tungsten Diselenide (WSe_2) and tungsten disulfide (WS_2)—are potential channel materials for field-effect transistors (FETs) that can be scaled to extremely small channel lengths without major short-channel effects[1–14]. Recently, contact resistance approaching

the quantum limit has been reported in n-type transistors with ML MoS_2 channels using van der Waals (vdW)-type semimetal contacts, such as bismuth and antimony[15,16]. Achieving high-performance transistors with a p-type ML TMD, such as WSe_2, typically requires a high work function metal, such as platinum or palladium, as the source–drain contact to reduce the Schottky barrier height (SBH) for hole injection. However, depositing these metals requires high energies for evaporation, which can lead to defects or the formation of undesirable platinum or palladium chalcogenides at the metal–TMD interface[17]. These defects and interfacial compounds make it challenging to achieve a low SBH in p-type ML TMD transistors.

To address this, various contact formation methods have been developed for WSe_2 p-FETs that do not involve 'hot' metal deposition. These include TMD-based contacts, such as VSe_2 and $Nb_{0.005}W_{0.995}Se_2$, and charge-transfer contacts using $RuCl_3$ (refs. 18–21). However, these contacts have yet to be combined with the most scaled transistors, where ultrashort channels of ML or bilayer (BL) WSe_2, ultrathin gate dielectrics and good on-state currents and low subthreshold swings are achieved simultaneously. ML or BL channels are essential for ultra-scaled logic applications, since channels with a larger body thickness do not allow for channel-length scaling into the nanometre regime without also introducing short-channel effects.

In this Article, we report short-channel (≈100 nm) ML and BL WSe_2 FETs using 2D metallic $Nb_{0.3}W_{0.7}Se_2$ contacts with much higher Nb content than previous approaches[19]. We create transistors on both thick (90 nm SiO_2) and ultrathin (5 nm HfO_2) dielectrics. A wet transfer method is adapted to pick up pre-etched $Nb_{0.3}W_{0.7}Se_2$ contacts and position them onto the WSe_2 film. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) imaging shows a locally flawless $Nb_{0.3}W_{0.7}Se_2$ /WSe_2 interface, with a bonding distance comparable to the interlayer vdW spacing of $Nb_{0.3}W_{0.7}Se_2$. Notably, the ML and BL WSe_2 FETs on 90-nm-thick SiO_2 substates exhibit on-state currents of 358 $\mu A\ \mu m^{-1}$ and 1.1 $mA\ \mu m^{-1}$, respectively. The ML WSe_2 FET on 5-nm-thick HfO_2 exhibits a subthreshold swing of 88 $mV\ dec^{-1}$. Simulated results using dissipative density functional theory (DFT)–non-equilibrium Green's function (NEGF) method agree with the experimental data, and indicate that a contact resistance below 100 $\Omega\ \mu m^{-1}$ can be achieved at high carrier density.

Fabrication and structure of 2D–2D contacted ML WSe_2 FETs

Figure 1a–f illustrates the fabrication process for an ultrashort channel $Nb_{0.3}W_{0.7}Se_2$-contacted WSe_2 FET for a 90-nm SiO_2 dielectric. First, $Nb_{0.3}W_{0.7}Se_2$ single-crystalline flakes, grown by the chemical vapour transport method, are mechanically exfoliated and selected for suitable dimensions and thickness using optical microscopy[22]. The detailed growth process is described in the Methods section. The selected $Nb_{0.3}W_{0.7}Se_2$ flake is then etched into the shape of $Nb_{0.3}W_{0.7}Se_2$ contact bars, as shown in Supplementary Fig. 3. A single $Nb_{0.3}W_{0.7}Se_2$ flake can be etched into five $Nb_{0.3}W_{0.7}Se_2$ contact bars, with the minimum distance between two ars as small as 100 nm, defined by the photoresist etching mask. The entire set of $Nb_{0.3}W_{0.7}Se_2$ contact bars is then wet-transferred onto the ML or BL WSe_2 film using a polystyrene film and deionized water

as described in the Methods section. The ML or BL WSe_2 flake, with thickness ranging from approximately 30 nm to 40 nm, is transferred onto either a 90-nm SiO_2/Si substrate or a 5-nm HfO_2/Au substrate before $Nb_{0.3}W_{0.7}Se_2$ contact formation. After transferring the $Nb_{0.3}W_{0.7}Se_2$ contacts, plasma etching is used to define the channel width of WSe_2. The etching mask also protects the $Nb_{0.3}W_{0.7}Se_2$ contact bars to prevent potential oxidation. The $Nb_{0.3}W_{0.7}Se_2$ contact bars are then connected to external metal contact bars for electrical measurement. Finally, the entire device undergoes annealing in a nitric oxide (NO) atmosphere at 130 °C for 1 h.[6] Figure 1g shows a scanning electron microscopy top view image of $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs with different channel lengths. The yellow, finger-shaped contacts represent the $Nb_{0.3}W_{0.7}Se_2$ contact bars, which are connected to larger metal contacts for electrical measurements, as shown by the green region. The dark blue region highlights the ML WSe_2 channel with a defined shape. To fabricate $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs on a thin dielectric, such as 5-nm-thick HfO_2, a thick isolation layer of 30 nm SiO_2 is required to minimize leakage currents from the back gate to the large metal pads. Supplementary Note 1 and the Methods section provide more detail on the various process flows. Figure 1h presents a cross-sectional image of a set of $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs with various channel lengths. The contact bars, which originate from a single $Nb_{0.3}W_{0.7}Se_2$ crystal, show clearly defined cross-sectional outlines in Fig. 1h. A zoomed-in image of one of the contact bars from Fig. 1h is shown in Fig. 1i, revealing a clear boundary between $Nb_{0.3}W_{0.7}Se_2$ and ML WSe_2. Figure 1j,k shows atomically resolved HAADF images along the [100] zone axis of the multilayer $Nb_{0.3}W_{0.7}Se_2$ and ML WSe_2, respectively, where the atomic columns of Nb/W and Se, as well as interlayer vdW gaps, are well resolved. The ML WSe_2 is tightly bonded with the multilayer $Nb_{0.3}W_{0.7}Se_2$ with a vdW gap that is comparable to the vdW gaps between the $Nb_{0.3}W_{0.7}Se_2$ layers, indicating an intimate contact has been achieved between the WSe_2 channel and the transferred and patterned $Nb_{0.3}W_{0.7}Se_2$ contact.

Electrical characterization of 2D–2D contacted ML–BL WSe_2 FETs

Previous work had used $Nb_{0.005}W_{0.995}Se_2$ as a contact material to reduce the contact resistance to multilayer WSe_2 devices[19]. It was reported that degenerate doping can be achieved with a Nb content of $x = 0.005$ (that is, 0.5 at.% Nb). Before fabricating our 2D–2D devices, we studied devices just from $Nb_xW_{1-x}Se_2$ alloys with different body thicknesses for three x values, ranging from $x \approx 0$ (that is, doped with undetectable Nb content by energy-dispersive X-ray spectroscopy (EDX), denoted as $x = x_1$) to 3 at.% Nb and 30 at.% Nb. As apparent from Extended Data Fig. 1, and as expected, introducing Nb into the WSe_2 lattice results in an effective p-doping of the WSe_2 channel. For comparison, the transfer curve of pristine ML WSe_2 is presented in Supplementary Fig. 5. However, changing the Nb content has a major impact on the current drive in those devices. For example, devices with body thicknesses larger than 15 nm (first column) show a decrease in resistance from approximately 4200 Ω for $x = x_1$ to 916 Ω at $x = 0.03$ and to 73 Ω for $x = 0.3$. It is also clear that a small Nb content in WSe_2 does not entirely remove the impact

of the gate voltage, in particular for thin body thicknesses. On the basis of these findings, we chose $x = 0.3$ for optimized device performance.

Figure 2a shows the transfer characteristics of a set of $Nb_{0.3}W_{0.7}Se_2$-contacted ML FETs with different channel lengths on a 90-nm SiO_2 substrate. A clear channel-length-dependent on-current level is observed at $V_{ds} = -1.0$ V, with an on/off current ratio between 10^7 and 10^9. Figure 2b presents the transfer characteristics of a device with $L_{ch} = 200$ nm at different V_{ds}. An on-current of 275 μA μm^{-1}, along with a small threshold voltage dependence on V_{ds} and a high on/off current ratio, indicates superior device performance for our $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs compared with previously reported 2D–2D contact FETs that showed severe short-channel effects, for example, in terms of drain-induced barrier lowering[18].

Figure 2c depicts the output characteristics of the same device at various gate voltages, showing a high on-current of up to 358 μA μm^{-1}. The linear output characteristics for small drain voltages suggest a small SBH between $Nb_{0.3}W_{0.7}Se_2$ contacts and ML WSe_2. Supplementary Fig. 6 in Supplementary Note 2 illustrates the on-current dependence on channel lengths ranging from 0.4 μm to 2.0 μm. A clear channel-length-dependent on-current level is observed at the same drain and back gate voltage, as shown in Supplementary Fig. 7. Extended Data Fig. 2 provides evidence of the reproducible nature of the 2D–2D contact formation achieved by our fabrication method. Figure 2d illustrates the contact resistance (R_c) versus carrier density for two sets of transfer length method (TLM) structures. The lowest contact resistance achieved is 2000 Ω μm^{-1} at a carrier density of 5×10^{12} cm^{-2}, which includes a metal–$Nb_{0.3}W_{0.7}Se_2$ interface resistance of approximately 80 Ω μm^{-1}, as shown in Supplementary Fig. 8. In comparison to some of our previous devices[13], the devices reported here use a ML WSe_2 channel to deliver high on-currents, can be entirely turned off and exhibit a contact resistance that, as expected, is gate voltage dependent, since gating affects the Schottky barrier thickness at the contact-to-channel interface.

Figure 2e compares transfer characteristics of Pd-contacted and $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 transistors. These show that the $Nb_{0.3}W_{0.7}Se_2$-contacted devices exhibit a lower SBH than Pd-contacted devices. Figure 2f shows the total resistance versus channel length at an overdrive voltage of −20 V. The relatively small device-to-device variation in the total resistance for devices with the same channel length allows for a good extraction of the contact resistance, $2R_c \sim 4000$ Ω μm^{-1} for this gate voltage. In contrast, Supplementary Fig. 9 shows that for Pd/Au contacts, the large variation in the total resistance versus channel length plot prevents a reliable extraction of contact resistance values and the total resistance for the shortest channel is much higher than for $Nb_{0.3}W_{0.7}Se_2$-contacted devices.

We also demonstrated $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs on 5-nm HfO_2, with an equivalent oxide thickness of 1.3 nm and a dielectric constant of 16 (as characterized in our previous publication[12]). The detailed fabrication process flow is shown in Supplementary Fig. 2. To minimize the leakage current for the overlap area between the source–drain metal electrodes and the back gate, we added a SiO_2 isolation layer underneath the contact electrodes, as shown in

Supplementary Fig. 4. We achieved a subthreshold swing as low as 88 mV dec^{-1} for $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs with a channel length of 100 nm, as shown in Fig. 3a. The unexpectedly low on-current level for these devices may be attributed to variations in the vdW gap between $Nb_{0.3}W_{0.7}Se_2$ and WSe_2 in the contact region due to the finite roughness of the local bottom gate stack. Supplementary Fig. 10a displays a good contact interface region, while Supplementary Fig. 10b shows a poor contact interface caused by deformation of the WSe_2 layer. In contrast, the minimum vdW gap, shown in Fig. 1j,k, was achieved on a 90-nm SiO_2 substrate.

We also explored $Nb_{0.3}W_{0.7}Se_2$-contacted BL WSe_2 FETs on a 90-nm SiO_2 substrate. A representative device with a channel length of 100 nm is shown in Fig. 3b, where an on-current of 717 μA μm^{-1} was achieved at $V_{ds} = -1$ V. A degraded off-state behaviour, including drain-induced barrier lowering and deteriorated subthreshold swings, can be attributed to short-channel effects. An apparent channel-length-dependent on-state performance of $Nb_{0.3}W_{0.7}Se_2$-contacted BL WSe_2 FETs is shown in Supplementary Fig. 11. Figure 3c depicts the output characteristics of the same device at various gate voltages, showing a high current of −1.1 mA μm^{-1} at a V_{ds} of −1.5 V. The total resistance of 1.47 kΩ μm^{-1} indicates a low contact resistance between $Nb_{0.3}W_{0.7}Se_2$ and BL WSe_2. Last, to benchmark the performance of our $Nb_{0.3}W_{0.7}Se_2$-contacted WSe_2 transistors, we compared the contact resistances reported here with previously reported ML WSe_2 and BL WSe_2 FETs, as shown in Fig. 3d (refs. [7,18,21,23-28]). A low contact resistance of 2 kΩ μm^{-1} is achieved for ML WSe_2 transistors, and a low 750 Ω μm^{-1} value has been demonstrated for BL WSe_2 transistors.

Structural calculation and transport simulation of 2D–2D contacted ML WSe_2 FETs

To explore the fundamental limit of the achievable 2D–2D contact resistance, we performed a dissipative DFT–NEGF theoretical study using the atomistic solver called the 'atomistic modelling solver' (ATOMOS)[29,30] to simulate the $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs. Previous calculations have shown that metal–semiconductor top contacts with vdW interaction, such as the 2D–2D $HfTe_2/HfS_2$ n-type contact, can suppress Fermi-level pinning with 2D semiconductors and lead to low SBH, if the right work function of the metal is achieved31. Our DFT calculations confirmed the metallic properties of $Nb_{0.3}W_{0.7}Se_2$, with the Fermi level positioned within the valence band and a low residual p-type Schottky barrier to WSe_2, as presented in Fig. 4d,e and in Supplementary Fig. 12. We also analysed the $Nb_{0.3}W_{0.7}Se_2/WSe_2$ heterostructure with different stacking orders, specifically AA and AA'. In the AA stacking configuration, where W/Nb atoms in the $Nb_{0.3}W_{0.7}Se_2$ layer are vertically aligned with W atoms in the ML WSe_2 layer, we found a SBH of 0.235 eV and a vdW gap of 3.5 Å, as shown in Fig. 4a,d. Conversely, as shown in Fig. 4d,e, in the AA' stacking configuration the alignment of the W/Nb atoms in the $Nb_{0.3}W_{0.7}Se_2$ layer with Se atoms in the ML WSe_2 layer allows for a smaller vdW gap of 2.86 Å and an increased SBH of 0.35 eV. The increasing SBH with reduced vdW gap distance is consistent with the trend observed for n-type vdW contact materials[31], where reduced vdW distance was also correlated to increased bonding energy and ultimately to

stronger Fermi-level pinning. These variations underscore the importance of stacking order on the electronic properties at the interface.

To explore the relationship between contact resistance and various parameters—including contact overlap length, stacking order, doping concentration, the number of layers in $Nb_{0.3}W_{0.7}Se_2/WSe_2$ and Nb concentration—we constructed a single contact structure of $Nb_{0.3}W_{0.7}Se_2/WSe_2$, as shown in Fig. 4c, where $N_{A,WSe2}$ represents the summation of electrostatic doping and external doping from NO gas annealing in the semiconducting WSe_2 layer. NO doping can effectively shift the Fermi level of pristine WSe_2 close to the valence band, as shown in Supplementary Fig. 13 (ref. 32). As presented in Fig. 4f, both for the AA and AA' stacking, the contact resistance was found to be strongly reduced with increasing doping concentration. A carrier density higher than 10^{14} cm^{-2} is required to achieve a contact resistance below 100 Ω μm^{-1} for the device of Fig. 4c (that is, with one layer of each material). The contact resistance R is dominated by the combination of the tunnelling resistances through the vdW gap, R_{vdW}, and through the SBH, R_{SB}. Both decrease with $N_{A,WSe2}$, as the tunnelling probability increases in both cases, although at a different rate. Qualitatively, R_{SB} tends to dominate over R_{vdW} at lower doping concentration, which explains the higher R of the AA' stacking in this range. The trend tends to revert, however, as R_{SB} becomes increasingly transparent for high $N_{A,WSe2}$ concentrations (the higher the initial barrier, the higher $N_{A,WSe2}$ must be for R_{SB} to vanish), as can be seen in Extended Data Fig. 3: as doping increases, the SBH is thinned electrically, so that for a sufficiently high $N_{A,WSe2}$ concentration it becomes fully transparent to the tunnelling carriers at the edge of the overlap region (Extended Data Fig. 3c). As can also be seen in the Extended Data Fig. 3, to transition from the source-side metal layer to the WSe_2 layer, the spectral current flows through the less resistive tunnelling path around the source Fermi level. This typically only encompasses a small edge portion of the overlap region. As a consequence, Fig. 4g presents the impact of overlap region on the contact resistance. Our results showed that the contact resistance is weakly dependent on overlap distance once it is larger than 10 nm, confirming that edge injection is the dominant mechanism in $Nb_{0.3}W_{0.7}Se_2$-contacted devices. We also examined the effect of different numbers of layers in $Nb_{0.3}W_{0.7}Se_2$ and WSe_2 on the SBH, both for AA and AA' stacking, as shown in Fig. 4h. Both stacking orders are likely to happen in the ML WSe_2 heterostructures (that is, about 20 meV formation energy differences). For the BL WSe_2 with at least two metal layers, however, the system always relaxes in the AA' configuration following a DFT supercell optimization (hence only the AA' stacking order results are shown for these cases in Fig. 4h). The general trend is a decrease of the SBH, while the vdW gap remains constant, with the number of layers, that is related to the material band structure changes (for example, a decrease of the WSe_2 bandgap with increasing number of layers). Typically, however, the SBH value does not change much for more than two to three layers of the same material. Notably, the configuration of a two or more-layer $Nb_{0.3}W_{0.7}Se_2$ with ML WSe_2 for AA stacking, and with a BL WSe_2 for AA' stacking, yielded the lowest SBHs. In such configurations, the SBHs were lower than 0.11 eV for the AA stacking and 0.03 eV for AA' stacking. As a consequence, the multilayer resistance trends are similar to those

obtained with one layer of each material but require a lower carrier density of a few 10^{13} cm^{-2} to achieve a contact resistance below 100 Ω μm^{-1} (Supplementary Fig. 14).

In addition, Supplementary Figs. 15 and 16 in the Supplementary Note 3 explore the impact of the Nb content, x, in the $Nb_xW_{1-x}Se_2$ AA ML on the properties of the 2D–2D contacted device. The observed differences in the contact resistance characteristics versus $N_{A,WSe2}$ doping for $x = 0.2$, 0.3 and 0.4 (Supplementary Fig. 16) are consistent with the small variations of SBH and vdW gap observed with x (Supplementary Fig. 15a,b), as discussed previously. The resistance curves show a larger spread at low doping concentration than at high $N_{A,WSe2}$, as expected from the Schottky barrier thinning with doping. Notably, the lower contact resistance of $Nb_{0.2}W_{0.8}Se_2$ for $N_{A,WSe2}$ for $N_{A,WSe2} \leq 2 \times 10^{13}$ cm^{-2} results from the lower SBH. One notable exception, however, is the much larger residual value of the contact resistance for $N_{A,WSe2} > 2 \times 10^{13}$ cm^{-2} for the case of $Nb_{0.2}W_{0.8}Se_2$ ($R > 200$ Ω μm^{-1}) compared with that of the larger x ($R \leq 20$ Ω μm^{-1}). This is attributed to the reduced Fermi-level degeneracy that induces a lesser carrier concentration in the $x = 0.2$ case, which is a less pronounced metallic behaviour induced by the lower Nb concentration, and a reduction of the available carriers for tunnelling from the metal part. This, in turn, limits the vdW tunnelling efficiency, hence, the reduction of R_{vdW} at high $N_{A,WSe2}$ concentration. Finally, our simulations showed a strong correlation with experimental data for contact resistance as a function of carrier density, with the multilayer $Nb_{0.3}W_{0.7}Se_2$–ML $N_{A,WSe2}$ experimental results closely aligning with the simulated three-layer $Nb_{0.3}W_{0.7}Se_2$–ML $N_{A,WSe2}$ predictions, as illustrated in Fig. 4i. We note that when a constant carrier concentration of 7.5×10^{12} cm^{-2}, which corresponds to the experimentally observed threshold voltage shift after NO doping, is added to our experimental data (black squares), an excellent match between simulations and experimental data (blue squares) is observed.

Conclusions

We have shown that metallic layered $Nb_{0.3}W_{0.7}Se_2$ can be used as contacts in ML and BL WSe_2 FETs with on-state currents of 358 μA μm^{-1} and 1.1 mA μm^{-1}, respectively. When these 2D contacts are integrated with an ultrathin, 5-nm-thick HfO_2 gate dielectric, ML WSe_2 FETs can achieve a subthreshold swing of 88 mV dec^{-1}. We performed a dissipative DFT–NEGF theoretical study to explore the performance limit of $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs, investigating the impact on contact resistance of contact overlap length, stacking order, doping concentration, number of layers of $Nb_{0.3}W_{0.7}Se_2$–WSe_2 and niobium content in the $Nb_{1-x}W_xSe_2$ alloy. The simulation results closely matched our experimental data and predict a contact resistance lower than 100 Ω μm^{-1} at high carrier density.

Challenges do remain, however, in terms of adapting $Nb_{0.3}W_{0.7}Se_2$ for large-scale integration. First, methods for wafer-scale growth of high-quality $Nb_{0.3}W_{0.7}Se_2$ films are required. Second, wafer-scale transfer technology that can be used in combination with polishing techniques for ultrathin dielectrics is needed to enable large-scale integration of p-type TMD transistors with 2D–2D contacts on ultrathin dielectrics.

Methods

Materials growth

$Nb_xW_{1-x}Se_2$ single-crystal alloys were grown by the chemical vapour transport method using appropriate amounts of Nb (99.9%), W (99.9%) and Se (99.999%) powders with a total weight of ≈1 g and ≈100 mg of $SeBr_4$ (99%) transport agent that were vacuum-sealed in quartz ampoules. For different runs, the temperatures at the charge zone and the growth zone were 980 °C to 850 °C and 850 °C to 800 °C, respectively. The ampoules were cooled down by switching off the furnace after 6 days of growth. More details on the growth and characterization of $Nb_xW_{1-x}Se_2$ alloys are reported in a previous publication[22]. The alloy composition was determined on the bulk crystals by EDX. For the sample with the lowest Nb content used in this study, labelled as $Nb_{x1}W_{1-x1}Se_2$, an actual Nb concentration was below the detection limit of the EDX instrument. However, the presence of Nb atoms was deduced from the broadening of the exciton lines[22]. The compositions of the other two samples, $Nb_{0.03}W_{0.97}Se_2$ and $Nb_{0.3}W_{0.7}Se_2$, were determined by EDX measurements.

Device fabrication on 90-nm SiO_2 substrate

Supplementary Fig. 1 illustrates the detailed fabrication process flow for $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 devices on 90-nm SiO_2 substrate. $Nb_{0.3}W_{0.7}Se_2$ flakes were mechanically exfoliated onto 90-nm SiO_2/Si substrates. Optical microscopy was used to identify flakes approximately 30 nm thick and large enough to fabricate ML FETs with different channel lengths. The sample was then spin-coated with ma-N 2400 photoresist and baked at 100 °C for 5 min. The contact bar shapes were patterned using a JEOL JBX-8100FS E-Beam Writer system and developed in MA-26 for 5 min followed by plasma etching with CHF_3 and O_2 for 2 min. The ma-N 2400 photoresist was then removed using acetone. Subsequently, a polystyrene solution in toluene was dropped onto the sample. The sample was baked at 90 °C for 2 min to form a polystyrene film. The sample was then immersed in deionized water until the polystyrene film with the attached $Nb_{0.3}W_{0.7}Se_2$ contact bars floated above the surface. The polystyrene film was carefully transferred onto ML WSe_2, which had been wet-transferred onto a 90-nm SiO_2/Si substrate. After the transfer, the polystyrene film was dissolved in acetone, and optical microscopy was used to identify the etched $Nb_{0.3}W_{0.7}Se_2$ contact bars. Next, the channel was defined using a JEOL JBX-8100FS E-Beam Writer, followed by plasma etching with Cl_2 and O_2 for 30 s. Following that, another pattern process was required to connect the $Nb_{0.3}W_{0.7}Se_2$ contact bars with larger measurement metal pads, followed by e-beam evaporation of 70-nm Ni as contact metal. Finally, the sample was annealed in a NO furnace at 130 °C for 1 h to complete the fabrication process.

Device fabrication on 5-nm HfO_2 substrate

Supplementary Fig. 2 illustrates the detailed fabrication process flow for $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 devices on 5-nm-thick HfO_2 substrate. The preparation of $Nb_{0.3}W_{0.7}Se_2$ contact bars followed the same process as described above. However, for the thin dielectric, a local bottom gate

of 2 nm/13 nm Cr/Au was present underneath 5-nm HfO_2 layer. ML WSe_2 was transferred onto this local bottom gate substrate instead of the 90 nm SiO_2 substrate for this device fabrication. The other fabrication steps followed the same process used for devices on the 90-nm SiO_2 substrate, with one key exception: a 30-nm isolation layer was inserted between the local bottom gate and the metal electrodes to minimize leakage current, which is caused by the large overlap area between the metal electrodes and the local bottom gate.

Characterization and measurements

A Lake Shore CPX-VF probe station and Agilent 4155C Semiconductor Parameter Analyzer were used to perform the electrical characterization at room temperature in high vacuum (0.1 mPa). Standard d.c. sweeps were used for the measurements of electrical characteristics for all devices. All devices were measured as-fabricated.

STEM characterization

Electron transparent cross-sectional sample was prepared with an FEI Helios NanoLab 660 DualBeam (scanning electron microscopy and focused ion beam). An FEI Titan 80-300 probe-corrected STEM/TEM microscope operating at 300 keV was used to conduct atomically resolved HAADF-STEM imaging, with a probe convergence semi-angle of 14 mrad and a collection angle of 70–399 mrad.

DFT-Hamiltonian computation

To compute the electronic properties and the DFT-based Hamiltonian of the vdW heterojunction supercells used in this work, we used the CP2K DFT package with the GTH-PBE exchange-correlation functional, the DZVP-MOLOPT-SR-GTH basis sets and the Grimme DFT-D3 vdW correction[33]. First, a WSe_2 hexagonal (2H) primitive cell with n_{LB} layers ($n_{LB} = 1,2$) and $3 \times n_{LB}$ atoms, was transformed in its orthorhombic conventional cell and repeated 5 times along the x (transport)-direction, resulting in a $30\times n_{LB}$-atom supercell with n_{LB} $W_{10}Se_{20}$ layers. A supercell with n_{LT} top layers ($n_{LT} = 1,2,3,4$) of $W_{10-y}Nb_yS_2$ was also created from the latter cell by substitution of y Nb atoms (we used here $y = 10 \times x = 2$, 3 and 4). Both cells were then relaxed separately and remained in their initial 2H phases as expected for $y < 6$ (ref. 34). For all simulated cases of y, the Nb substitution resulted in a several hundreds of mega electron volts increase of the $W_{10\text{-}y}Nb_yS_2$ sub-band energy, when compared with that of $W_{10}Se_{20}$, with a Fermi level, E_F, deeply degenerate in the valence band, E_V, effectively rendering the alloy metallic (Fig. 4b,e). Subsequently, both materials were joined vertically (along the z axis) in a supercell, applying half of the strain to each material to achieve a commensurate in-plane lattice (typically applying a small strain of less than 1% on each layer in the x and y directions), after which an additional full cell and atom geometry relaxation was performed again. An energy cut-off of 500 Ry and a $1 \times 16 \times 1$ Monkhorst-Pack k-point grid were used based on convergence tests. The convergence criteria were set to 10^{-7} for the relative self-consistent field charge error and 7×10^{-3} eV Å^{-1} for the forces acting on each ion during geometry relaxation. A relaxed supercell with $n_{LB} = n_{LT} = 1$ and $y = 3$ is shown

in Fig. 4a,b for AA and AA' stacking, respectively. As shown on Fig. 4b,e, the difference between E_F and the top of the WSe_2 valence band, $E_{V,WSe2}$, gives a DFT estimates of the SBH.

Quantum transport solver

The Kohn–Sham and overlap matrices were then extracted and used as input for our quantum transport solver, ATOMOS[29,30], to build the Hamiltonian for the resistor device with a top contact configuration (Fig. 4c). Self-consistent calculation including electron–phonon scattering within the self-consistent Born approximation were performed using a non-orthogonal DFT–NEGF model[35]. The computational burden of the NEGF model was further reduced using the mode–space technique[36,37]. The NEGF-computed currents through the resistor device for different V_{ds} bias conditions was used to compute the R_C values. We assumed periodic boundary conditions in the width (y axis) direction. They were modelled using a plane-wave expansion using 10 y momentum points on half the Brillion zone: the other half was obtained by symmetry.

Data availability

Source data are provided with this paper.

Acknowledgements

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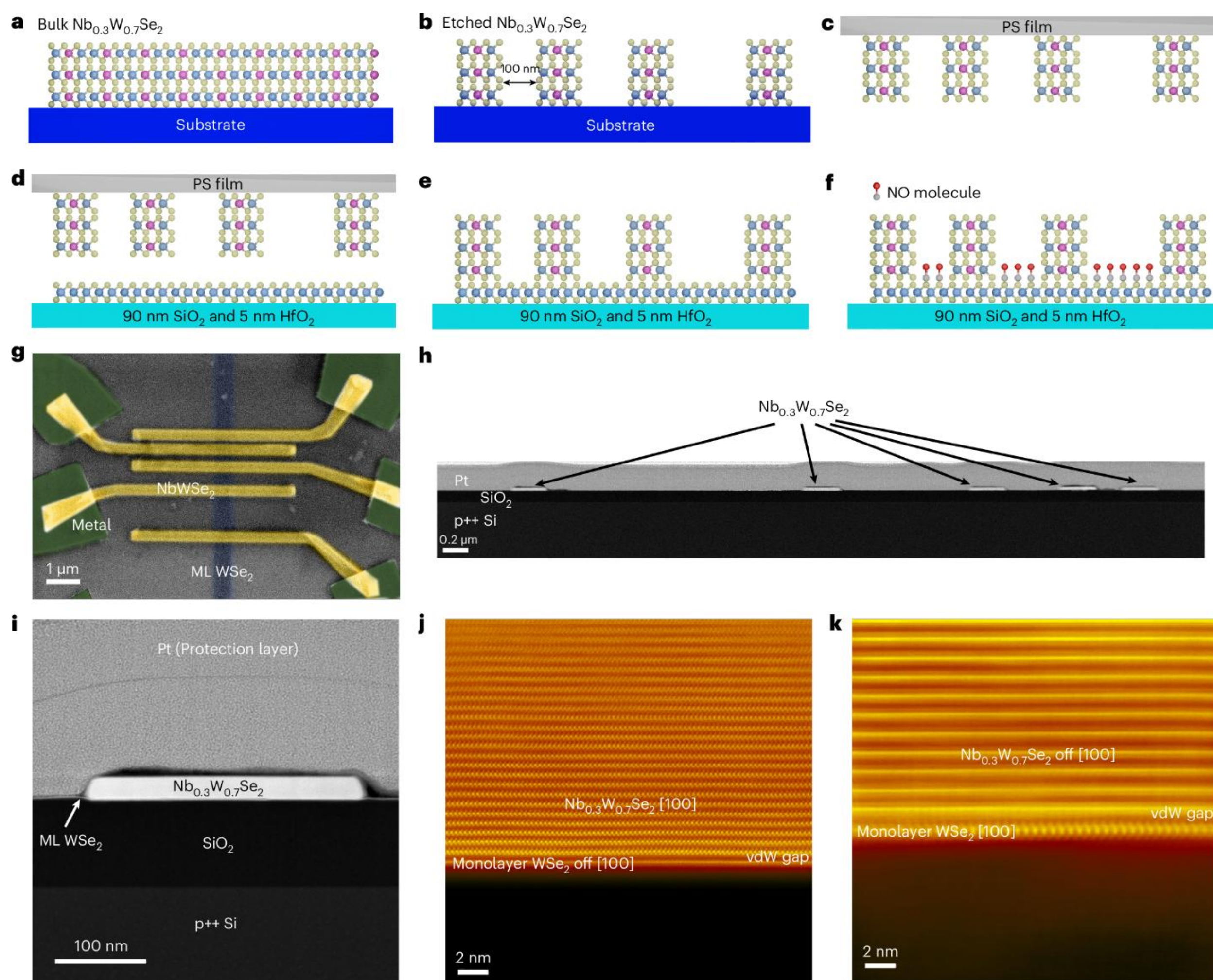


Figure 1. a, Exfoliated $Nb_{0.3}W_{0.7}Se_2$ flakes transferred onto SiO_2/Si substrate. **b**, Patterned and etched $Nb_{0.3}W_{0.7}Se_2$ contact bars with a minimum gap distance of around 100 nm. **c**, Polystyrene (PS)-assisted wet transfer process to pick up the etched $Nb_{0.3}W_{0.7}Se_2$ contact bars from 90 nm SiO_2 substrate. **d**, $Nb_{0.3}W_{0.7}Se_2$ contact bars transferred onto ML WSe_2 film on 90 nm SiO_2 substrates or 5 nm HfO_2 substrates. **e**, Fabricated ML WSe_2 FETs with $Nb_{0.3}W_{0.7}Se_2$ contacts. **f**, NO annealed sample. **g**, False coloured scanning electron microscopy image of FETs. **h**, Cross-sectional HAADF-STEM image of a set of $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs with different channel lengths for TLM extraction. **i**, Zoom-in image of one of the $Nb_{0.3}W_{0.7}Se_2$/ML WSe_2 contact bars. **j**,**k**, Atomic-resolution HAADF images taken along the [100] zone axis of $Nb_{0.3}W_{0.7}Se_2$ (**j**) and WSe_2 (**k**). The [100] ML WSe_2 was misaligned 18° with respect to the [100] multilayer $Nb_{0.3}W_{0.7}Se_2$.

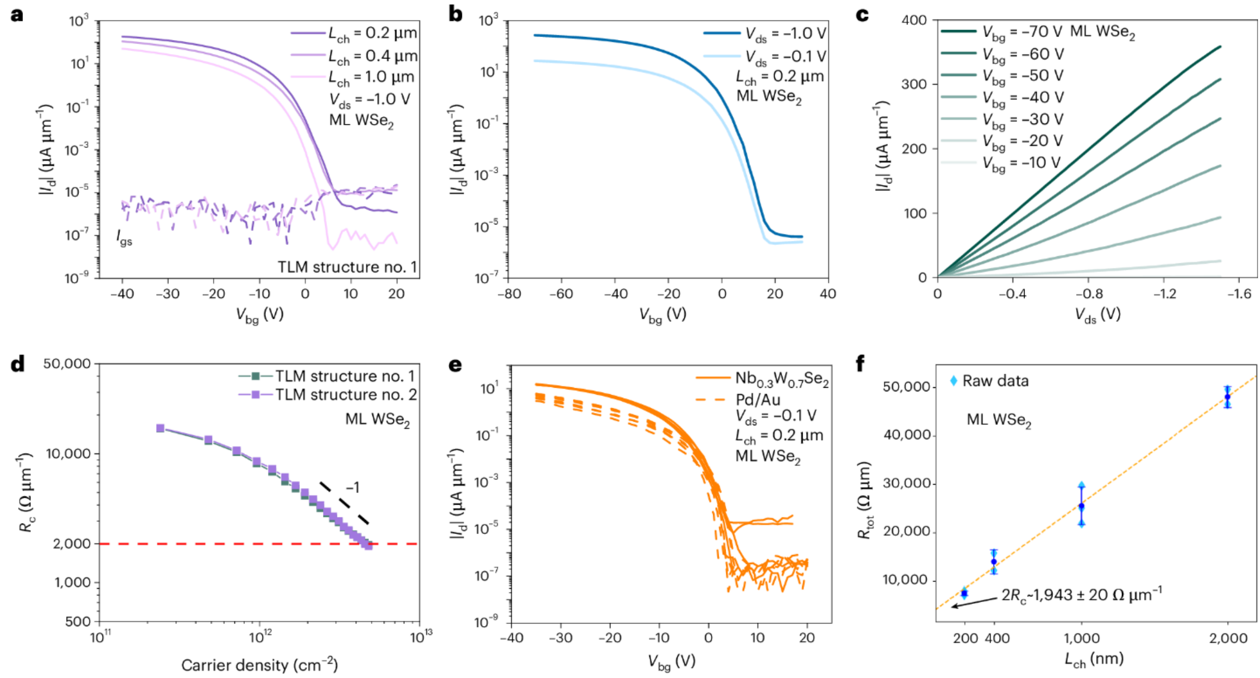


Figure 2. a, Transfer characteristics of a set of $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FETs with different channel lengths. **b**, Transfer characteristics. **c**, Output characteristics of a representative $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FET with a channel length $L_{ch} = 200$ nm. **d**, Contact resistance versus carrier density, extracted from two different sets of TLM structures. **e**, Transfer characteristics of multiple $Nb_{0.3}W_{0.7}Se_2$-contacted and Pd-contacted ML WSe_2 FETs. **f**, Total resistance versus channel length at $V_{bg} = -40$ V for various channel lengths from multiple 2D–2D contacted TLM structures. Data are presented as mean values ± s.e.m., calculated from $n = 4$ (200 nm), 2 (400 nm), 3 (1000 nm) and 2 (2000 nm) independent devices, respectively. Each device corresponds to a separately fabricated transistor. The dashed line shows a linear fit to the mean values. The extracted contact resistance is 1943 ± 20 Ω μm^{-1}.

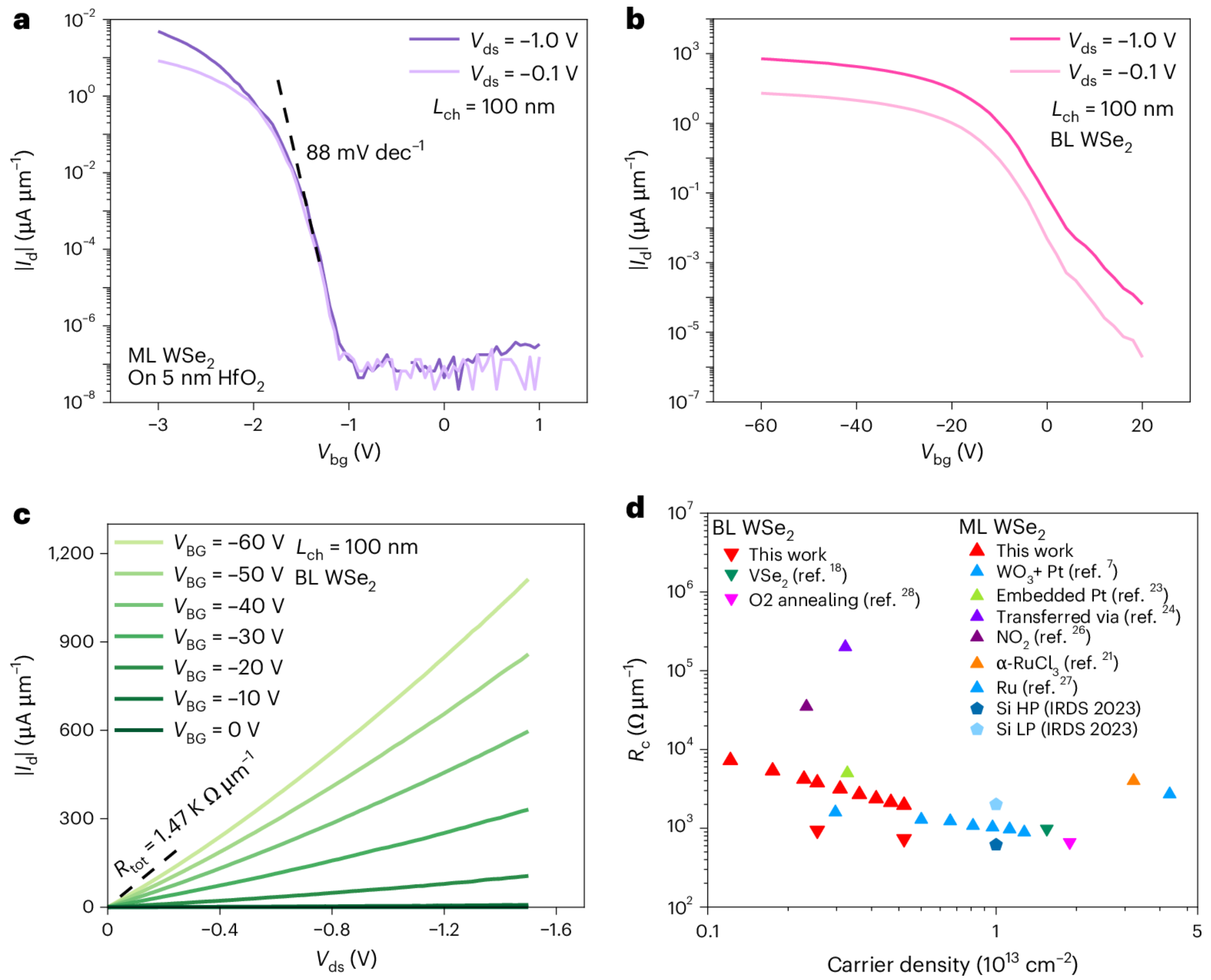


Figure 3. a, Transfer characteristics of a representative $Nb_{0.3}W_{0.7}Se_2$-contacted ML WSe_2 FET on a dielectric stack of 5-nm HfO_2. **b**, Transfer characteristics of a representative BL WSe_2 FET with L_{ch} = 100 nm at different V_{ds}. **c**, Output characteristics of a representative BL WSe_2 FET with L_{ch} = 100 nm at different V_{bg}. **d**, Contact resistance versus carrier density benchmarking.

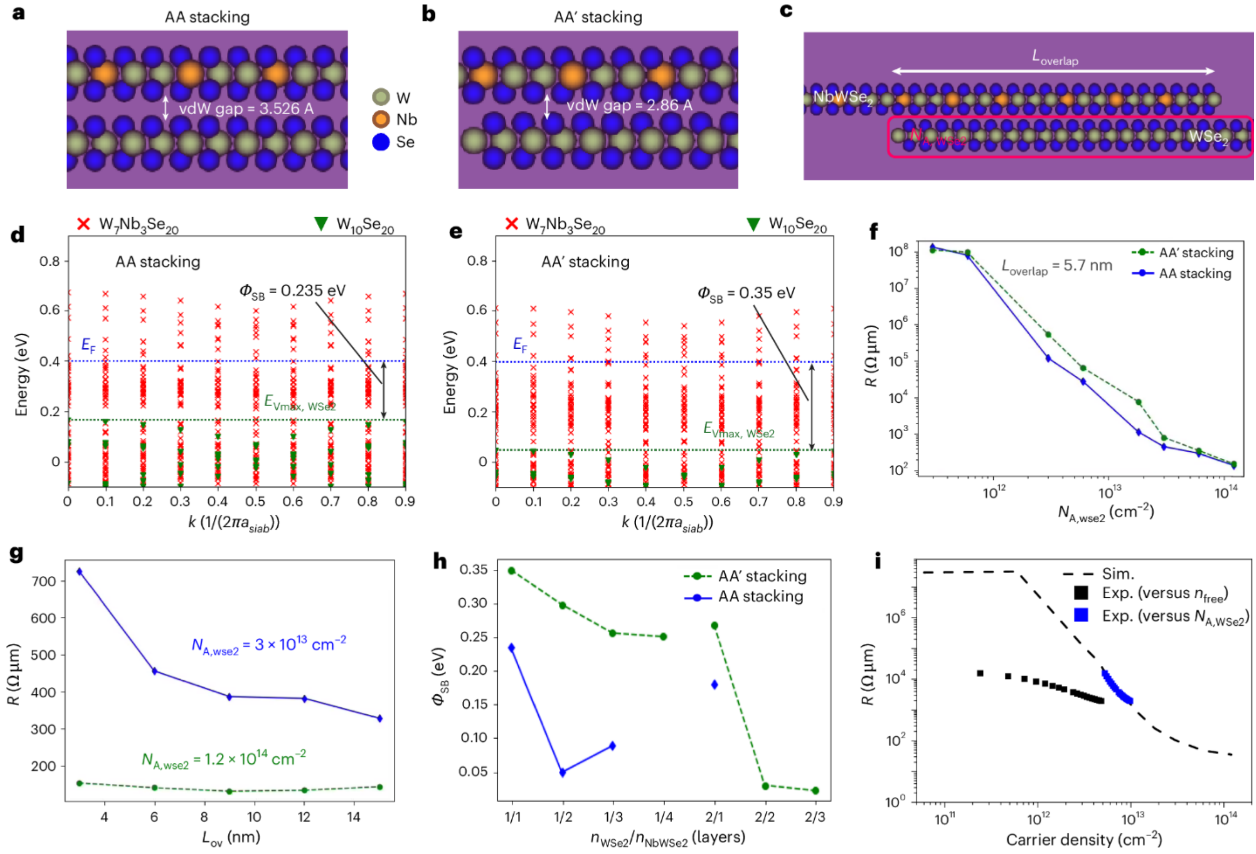
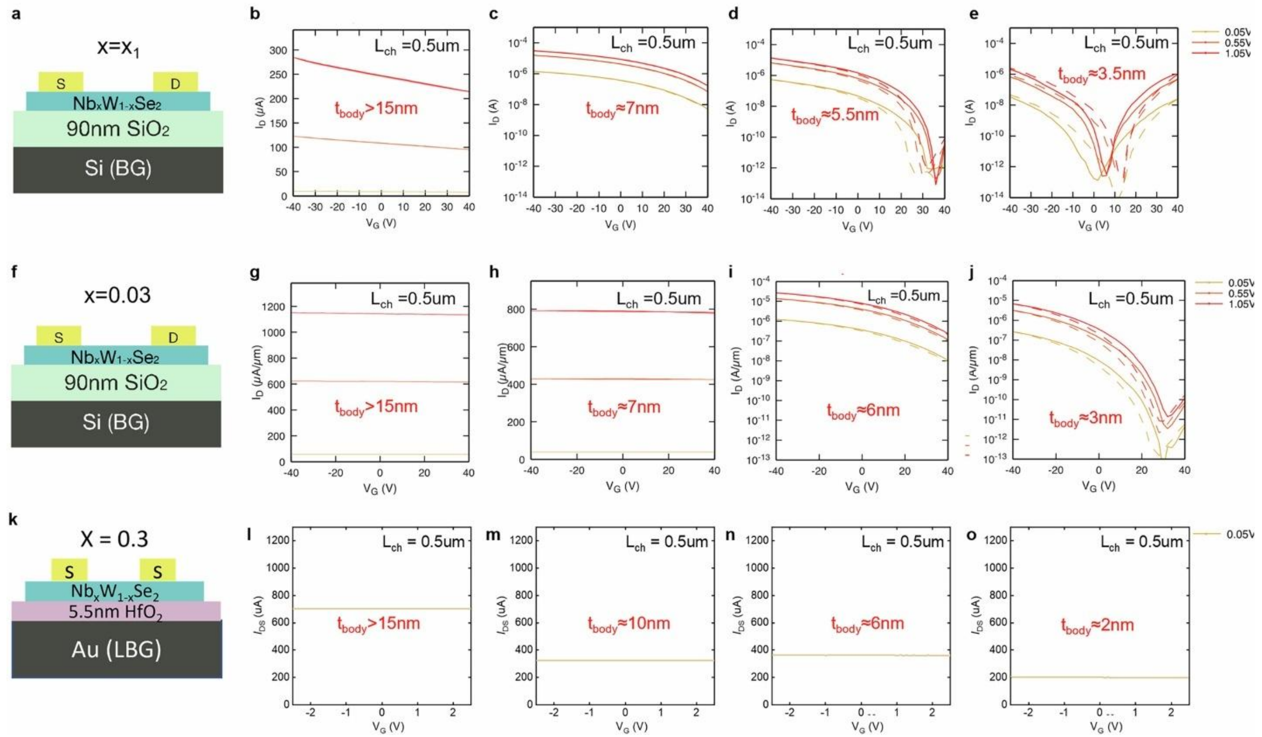
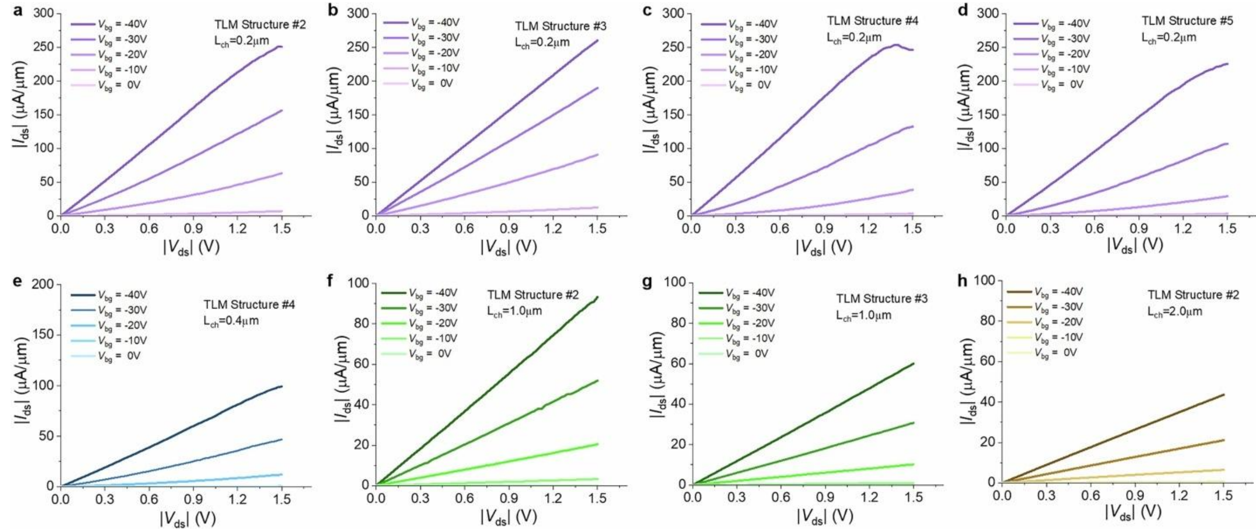


Figure 4. **a**,**b**, Different stacking orders of $Nb_{0.3}W_{0.7}Se_2/WSe_2$ heterostructures: AA stacking (**a**) and AA' stacking (**b**). **c**, Schematic view of the device simulated in ATOMOS. **d**,**e**, DFT-computed energy-momentum dispersion and SBHs in the heterostructure supercell or slab of $Nb_{0.3}W_{0.7}Se_2$ and WSe_2 with AA (**d**) and AA' stacking (**e**). **f**, Contact resistance versus carrier density for contact overlap length ($L_{overlap}$) = 5.7 nm with different stacking order. **g**, Contact resistance versus $L_{overlap}$ for two carrier densities with AA stack. **h**, SBH of $Nb_{0.3}W_{0.7}Se_2/WSe_2$ heterostructure for different layer number combinations of WSe_2 and $Nb_{0.3}W_{0.7}Se_2$. **i**, Contact resistance versus carrier density for $Nb_{0.3}W_{0.7}Se_2$ contacts (simulated (Sim.) structure: three-layer $Nb_{0.3}W_{0.7}Se_2$/ML WSe_2 with AA stacking; experimental (Exp.) structure: multilayer $Nb_{0.3}W_{0.7}Se_2$/ML WSe_2).



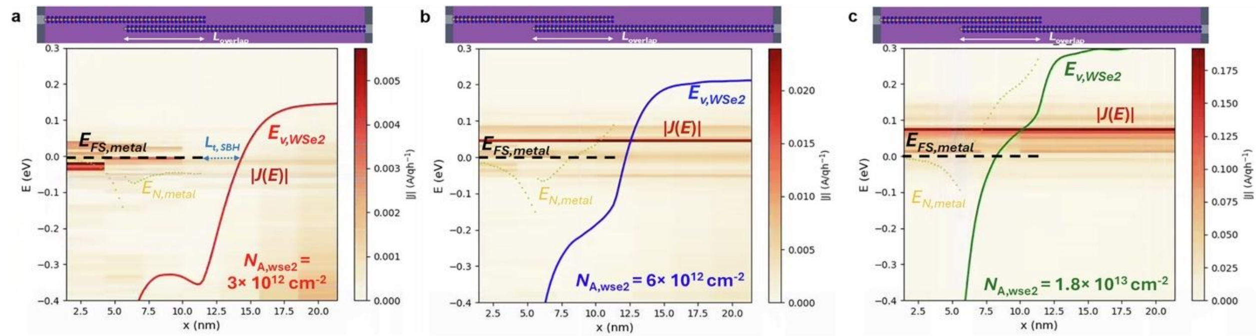
Extended Data Fig. 1 Transfer characteristics of mechanically exfoliated $Nb_xW_{1-x}Se_2$ flakes of varied composition with different thicknesses.

a, Schematic of $Nb_{x1}W_{1-x1}Se_2$ transistors, it had a near-zero Nb concentration, undetectable by EDX as described in the materials growth part of the Method section. **b-e**, Transfer characteristics of different $Nb_{x1}W_{1-x1}Se_2$ flake thickness. **f**, Schematic of $Nb_{0.03}W_{0.97}Se_2$ transistors. **g-j**, Transfer characteristics of different $Nb_{0.03}W_{0.97}Se_2$ flake thickness. **k**, Schematic of $Nb_{0.3}W_{0.7}Se_2$ transistors. **l-o**, Transfer characteristics of different $Nb_{0.3}W_{0.7}Se_2$ flake thickness.



Extended Data Fig. 2 Output characteristics of 2D/2D contacted ML FETs on 90 nm SiO_2 substrates.

a-d, four different 2D/2D contacted devices with a channel length of 200 nm. **e**, a 2D/2D contacted device with a channel length of 400 nm. **f** and **g**, two 2D/2D contacted devices with a channel length of 1 um. **h**, a 2D/2D contacted device with a channel length of 2 um.



Extended Data Fig. 3 DFT-NEGF-simulated spectral current (in absolute units), | J(E)|, along the transport direction (x) in the $Nb_{0.3}W_{0.7}Se_2/WSe_2$ heterostructure of Fig. 4c for different $N_{A,WSe2}$ doping concentrations in the WSe_2 bottom layer a. $N_{A,WSe2} = 3\times10^{12}$ cm^{-2}, b. $N_{A,WSe2} = 6\times10^{12}$ cm^{-2}, and c. $N_{A,WSe2} = 1.8\times10^{13}$ cm^{-2}.

The valence band in the WSe_2 layer, $E_{V,WSe2}$, as well as, the source Fermi level in the $Nb_{0.3}W_{0.7}Se_2$ metallic region (black dotted line), $E_{FS,\ metal}$, are also indicated. The x-distance between the end of the $E_{FS,metal}$ line and the $E_{V,WSe2}$ line in the vicinity of the source Fermi level $L_{t,SBH}$ is indicated with a blue arrow in **a**. $L_{t,SBH}$ represents an estimate of the carrier tunneling distance through the Schottky barrier. As $N_{A,Wse2}$ is increased, this distance is strongly reduced **b**, or vanishes **c**, that is, the carriers feel an increasingly transparent Schottky barrier when crossing from the edge of the metal layer to the WSe_2 layer. Finally, the position of the

neutrality level, $E_{N,metal}$, that is, the equilibrium DFT- Fermi-level moved by the self-consistent potential in the metal layer is also shown, as well as a schematic view of the device, with the top metal and bottom WSe_2 positions in the x-direction matching those of the spectral plot. $V_{DS} = -0.15$ V.