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Design, Modelling, and Fabrication of High Frequency Oersted Lines for Electron Spin Manipulation in Silicon Based Quantum Devices

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Coherent manipulation of electron spins is one of the central challenges of silicon-based quantum computing efforts. Electron spin resonance (ESR) lines, or Oersted lines, allow 10-60 GHz radio frequency (RF) pulses to induce an electromagnetic field that drives Rabi oscillations in a quantum dot interface. The frequency of these Rabi oscillations is directly proportional to the strength of the induced electromagnetic field. We outline a methodology for the design of a printed circuit board (PCB) and an ESR line that is able to transmit an RF pulse in the 40 GHz regime and induce an oscillating magnetic field onto a qubit device. We propose and implement a novel design by coupling a second symmetrical

Oersted line in the opposing direction of the first to act as an antenna for the purpose of monitoring power and magnetic field strength at the embedded device interface.

I. INTRODUCTION

Silicon based quantum computing efforts have made significant progress within the past two decades[1,2]. Several different proposals have emerged for fabricating scalable quantum dot devices in semiconductor materials. Silicon metal-oxide-semiconductor (MOS) structures and silicon-germanium (SiGe) heterostructures[3] are widely used for confining electrons using metallic gates[4]. Furthermore, atomically precise scanning tunnelling microscope (STM) fabrication presents a promising approach for creating donor-based solid-state quantum computing architectures in silicon[5], an example being donor dot devices in silicon[2]. In these systems, qubits can be either the spin of an electron on the valence shell of a phosphorus (P) donor or the nuclear spin of the P donor[6].

Superposition, entanglement, and coherent manipulation of quantum states are key fundamental concepts utilized for realizing practical quantum computers[7]. High fidelity coherent manipulation ensures the integrity of the quantum state and entanglement[6]. Applying a static magnetic field to Zeeman split electron spin energy states and applying an additional oscillating electromagnetic field to drive coherent Rabi oscillations is now an established technique[6]. The experimental realization of single spin qubit systems becomes challenging because spin resonance frequencies are in the 10-60 GHz range[8]. Additionally, for the desired energy splitting of the spin states, the Zeeman energy must be larger than the thermal energy of the system while still allowing a reasonable spin relaxation time[9]. As such, the qubit system requires low temperatures in

the millikelvin regime with electron temperatures typically below 300 mK to operate. Therefore, transmitting high frequency manipulation pulses to the device is very demanding.

An electron spin resonance, or Oersted, line is used to transmit RF pulses and apply the oscillating electromagnetic field needed to drive Rabi oscillations[8]. As a method to efficiently develop Oersted lines, we implement several simulations and fabrication designs for testing and verifying a magnetic field pulse applied to a silicon chip quantum dot device.

The applied static magnetic field is usually on the order of 1.5 T to induce a Zeeman split sufficient to allow spin up and spin down states to be distinguishable[10]. Since energy is directly proportional to frequency by Planck's constant, the energy difference between both spin states will scale by approximately 28 GHz/T at a base temperature of 100 mK[11]. Therefore, an applied static field of 1.5 T will produce an energy difference between spin up and spin down states on the order of 40 GHz. To successfully drive Rabi oscillations, an experimental setup and design for a PCB with an on-chip ESR line must be developed to allow such high frequency RF pulses to reach a quantum device with minimal losses. The frequency of Rabi oscillation is proportional to the strength of the oscillating magnetic field which depends on the proximity of the ESR line to the qubit structure[12]. The main goal of this work is to understand the magnetic field distribution around the ESR line. We have performed simulations using COMSOL Multiphysics®[21] [see footnote 1] and

[1] Certain commercial equipment, instruments, or materials are identified in this article to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by NIST, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

performed experiments using a receiving antenna to verify and measure the strength of the resulting magnetic field. We also detail the design and fabrication of a PCB to interface the on-chip coplanar waveguides (CPWs) to high frequency wiring in the dilution refrigerator used to operate the device.

To transmit RF frequencies in the 40 GHz range with minimal losses, CPWs can be utilized. CPWs are transmission lines with one signal line sandwiched between two two-dimensional ground planes[13]. Adjusting the spacing between the signal line and ground planes and varying the width of the signal line and the material on which it is fabricated enables the CPW to be impedance matched[14]. Additionally, shorting one end of the CPW signal line to the ground plane allows current to flow down a narrowed path and based on the Biot-Savart Law, there will be a magnetic field perpendicular to that path. By placing a quantum dot in the vicinity of the induced field as shown in Figure 1, a Rabi oscillation may in turn be driven[8]. Thus, understanding how to design and fabricate CPWs and adapting the design by terminating nanometer scale Oersted lines is crucial to developing a scalable quantum computing system based on donor qubits in silicon.

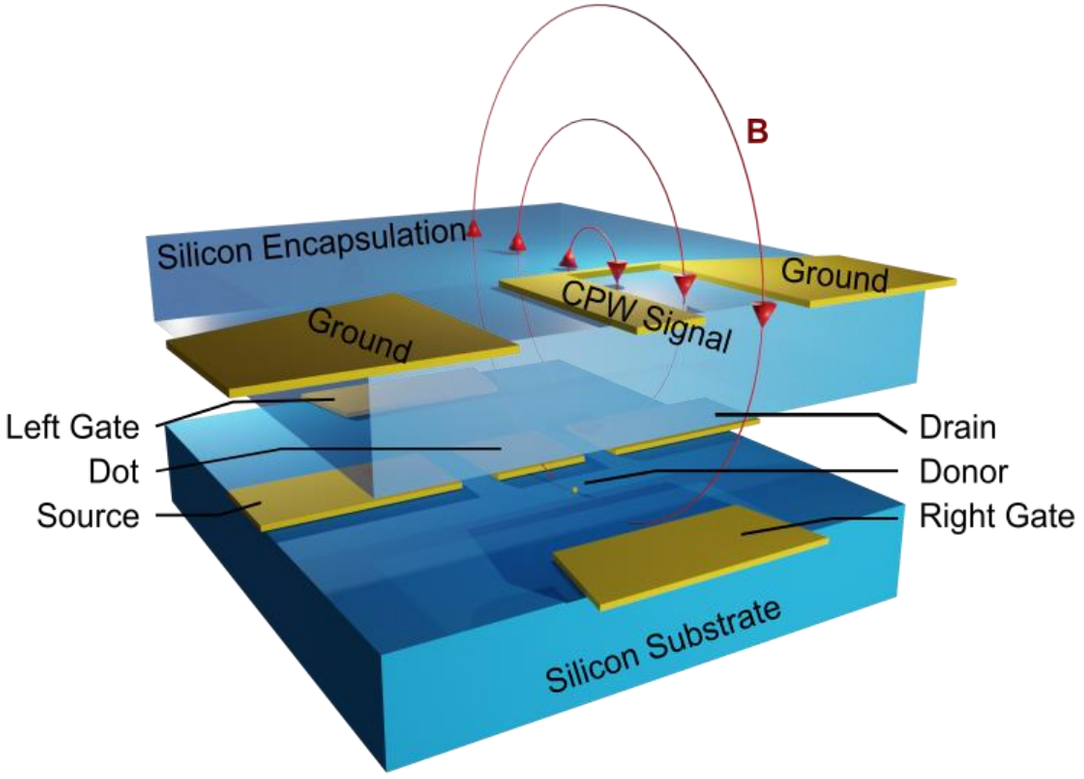

FIG. 1. A three-dimensional model of an ESR line on the surface of a silicon chip inducing a magnetic field onto a quantum dot device buried ~30 nm below the surface.

Here, we show our steps for designing on-chip CPWs using finite element modelling software to mimic our test setup, composed of signal lines on a PCB with a silicon chip wire bonded in the center. The design of the on-chip CPW was modified in the central region to form two symmetrical Oersted lines. The opposing Oersted line acts as a receiving antenna for the purpose of monitoring electromagnetic field strength applied to the device regime. On-chip Oersted-antenna devices with varying distances between the Oersted signal line and the coupled receiving antenna were fabricated and measured to verify the validity of their modelled behavior. Our novel Oersted-antenna devices are

shown to be beneficial for determining the magnetic field power distribution surrounding an ESR line.

II. MODELLING

Modelling was utilized during the design stage to optimize the geometry of our on-chip signal lines at high frequencies. We started by determining the dimensions of a CPW that has minimal reflections and allows for wire bonding each signal and ground line to a test PCB. This design was then modified to form an original Oersted-antenna structure, and the expected magnetic field distribution was simulated.

Coplanar waveguides consist of a central strip signal line surrounded by two metal ground planes on a dielectric slab[13]. Although most theory on coplanar waveguides assumes an infinite width for the ground planes, practical realization of such waveguides require finite width. If the width of the ground plane is large enough compared to the width of the signal line, finite ground width CPWs match very closely to the characteristics of infinite ground width CPWs[13].

The effective permittivity of a CPW is given by [13]:

$$\varepsilon_E \approx \frac{(\varepsilon_r + 1)}{2} \tag{1}$$

The characteristic impedance of a CPW can then be found using Eq (2) [14]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_E}} \frac{K(k')}{K(k)} \tag{2}$$

Where $K(k)$ is the complete elliptic integral of the first kind.

A unique solution for the characteristic impedance does not exist for different combinations of ground plane spacings and signal line widths. This allows for flexibility when designing CPWs[14].

The widths of the planes of the CPW on the silicon chip have been carefully tuned for 50 Ω impedance to minimize reflections and losses at each end. The transmission line gradually tapers from dimensions compatible with wire bonding down to the desired size of the Oersted line structure maintaining a characteristic 50 Ω impedance.

COMSOL was used in the design process to verify impedance matching, measure transmittance/reflectance parameters, and model electromagnetic fields of CPWs and Oersted lines. Figure 2(a) shows a COMSOL model for the experimental setup consisting of a silicon chip with a gold CPW wire bonded to a continuous CPW made on a PCB using gold-plated copper on a CLTE-AT Rogers dielectric material. The simulated S-parameters for this design are shown in Figure 2(b). S-parameters are used to quantify what fraction of an incident RF signal is reflected back (S11) to the incident port or transmitted through (S21) our device, in this case reaching the other end of the PCB. The power measured for each S-parameter is directly related to the power of the electromagnetic field produced by the signal. Therefore, the S-parameters are extremely useful in determining the strength of the electromagnetic field at our device interface. The ripple in the frequency response corresponds to a standing wave behavior due to a combination of cavity effects, gap spacing, and the reflections at each wire bonded edge. This was verified with a time domain reflectometry measurement and COMSOL simulation of the electric field shown in Figure 3.

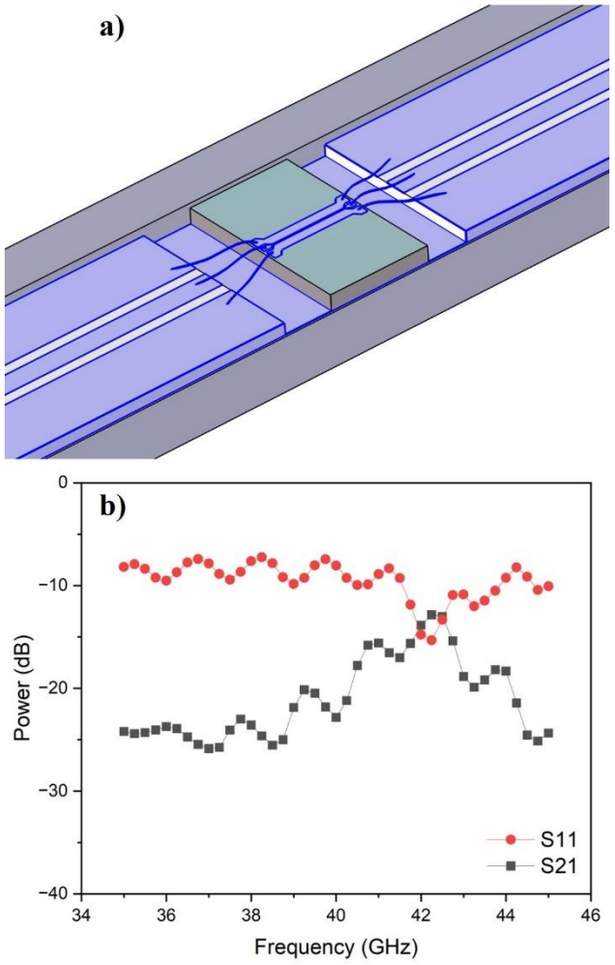

FIG. 2. (a) COMSOL model for a CPW on a PCB made from CTLE-AT Rogers material (white) wire bonded to a CPW on a silicon chip (center). The solid blue color represents a gold conductor. Ground planes of the CPW on the PCB are connected by vias to a ground plane that stretches the entire bottom plane of the structure. The CPW on the silicon chip has larger pads to make it easier to wire bond to, which then decrease slightly in width. Spacing and widths are chosen to have a 50 Ω impedance on both ports at the desired frequency of around 42 GHz. (b) Simulated S-parameters for the modeled design show the largest transmittance occurs at the desired frequency. The ripple is due to standing wave behavior and a cavity effect caused by the gap and reflections at the wire-bonded edges of the PCB and silicon chip interface.

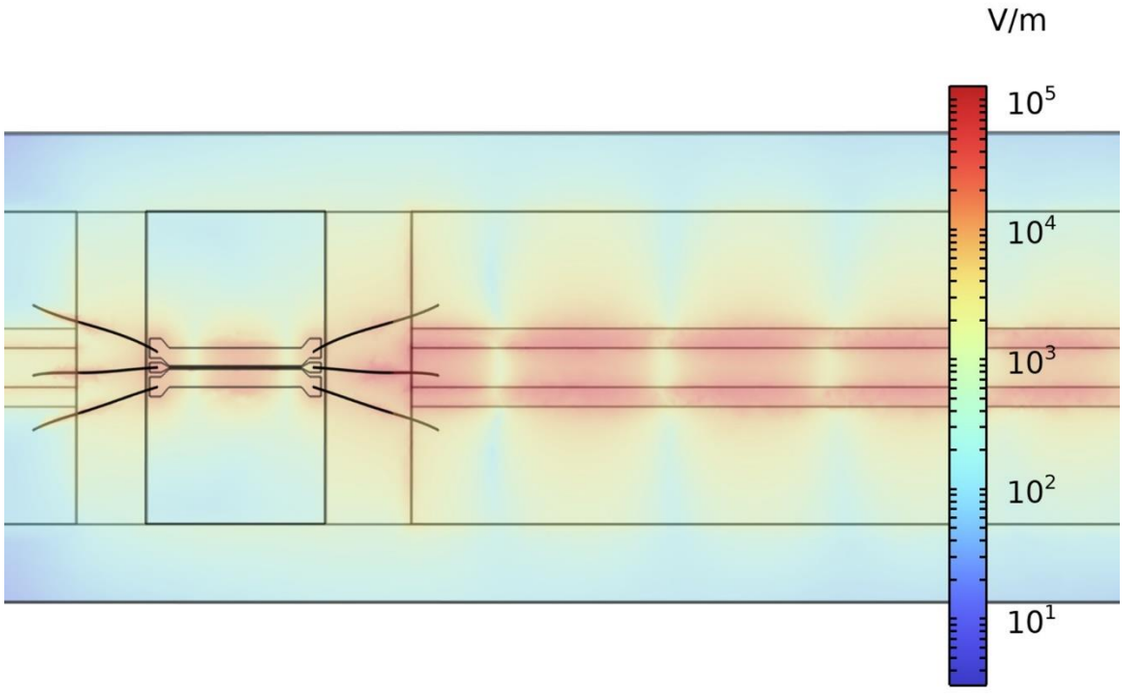

FIG. 3. COMSOL simulation result showing the electric field magnitude at 40 GHz. Standing wave behavior is observed due to reflections at the wire bonded edge of the PCB CPW.

As seen in Figure 1, for a device with a qubit structure positioned below one end of a CPW, shorting that end of the CPW signal line to the ground plane results in a perpendicular magnetic field directed onto the qubit structure[8]. A second Oersted line can be appended to the opposite side of the first Oersted line to act as a receiving antenna[14]. This is useful for characterizing the power and strength of the magnetic field being applied to the quantum dot device. In this work, several designs for the Oersted-antenna structure have been simulated and tested to ensure maximum transmittance and minimal losses in the 40 GHz regime. Figure 4 shows one such design and the simulated magnetic field coupling for a device that we then fabricated and measured (as described in sections III and IV).

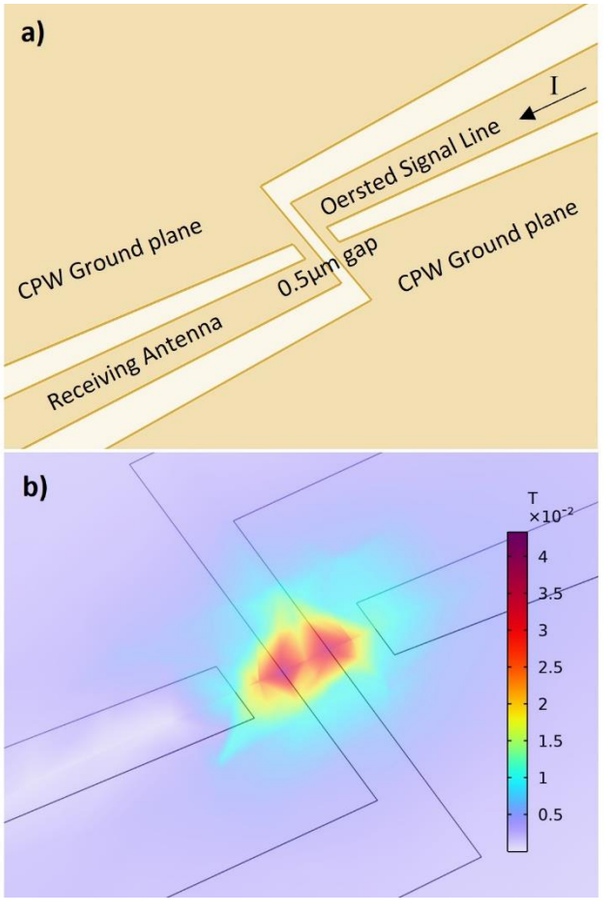

FIG. 4. The CPW on the silicon chip from Figure 2 is modified at the center to have an Oersted line coupled to a symmetrical receiving antenna line with 0.5 μm spacing. (a) Gold color is a conducting plane, and the lighter white color represents the silicon gap spacings in the modified CPW design. (b) A Magnetic Fields COMSOL simulation result conveying the magnetic flux density magnitude across the center of the device. The magnetic field is concentrated over the gap between both lines. The distortions are due to the triangular meshing pattern utilized for the simulation.

III. EXPERIMENTAL

The on-chip CPW and Oersted-antenna structures modelled in Section II were subsequently fabricated and measured. To physically measure the devices, the chips were interfaced to a custom-made PCB that has high frequency CPWs. Our test setup follows

the model shown in Figure 5. The PCB was designed for the purpose of testing, measuring, and controlling our quantum dot devices, so additional components and signal lines are described.

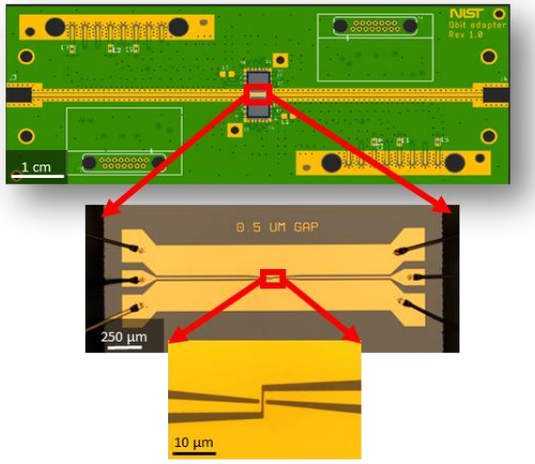

FIG. 5. Physical experimental test setup for measuring S-parameters of our Oersted-antenna devices. A PCB with two mini-SMP connectors on each end allows mini-SMP to 2.92 mm adapters and 2.92 mm cables to be attached to both ends of the PCB CPW. A silicon chip with our test devices is gold wire bonded in the central region of the PCB.

The PCB is designed to test and measure atomic scale devices[15,16], and consists of 14 twisted pair DC lines, 16 SMA lines (DC to 18 GHz), and the two 40 GHz CPWs interfaced through SMP edge launchers. The DC lines include a two-stage RC low-pass filter with 200 or 300 kHz cutoffs for supplying stable DC biases and gate voltages to our devices. The SMA lines are designed to supply nanosecond duration gate pulses which can, for example, be used to implement two qubit gates through exchange interactions[17,18]. The DC lines and SMA lines combine through an on-board bias tee to deliver arbitrary control pulses. The PCB also has a special SMA line designed for RF reflectometry[19,20]. An LC tank circuit is used to impedance match the donor dot device for maximizing signal

contrast. Spin readout can be performed by using spin to charge conversion and measured using the high bandwidth reflected RF signal[20].

The PCB is a six-layer board (layout shown in Figure 6), consisting of separate layers for low (DC signals), medium (DC to 18 GHz), and high frequencies (DC to 40 GHz), each separated by a ground layer. The ground layers help to isolate each type of signal line and reduce crosstalk noise between them. The high frequency microwave lines for electron spin manipulation were fabricated on Rogers CLTE-AT material. Each PCB CPW has a mini-SMP connector which is used to carry the high frequency signal to the device. Dimensions for the CPW were chosen for 50 Ω impedance matching. Each line terminates at a gold pad where the fabricated device on the silicon chip is wire bonded.

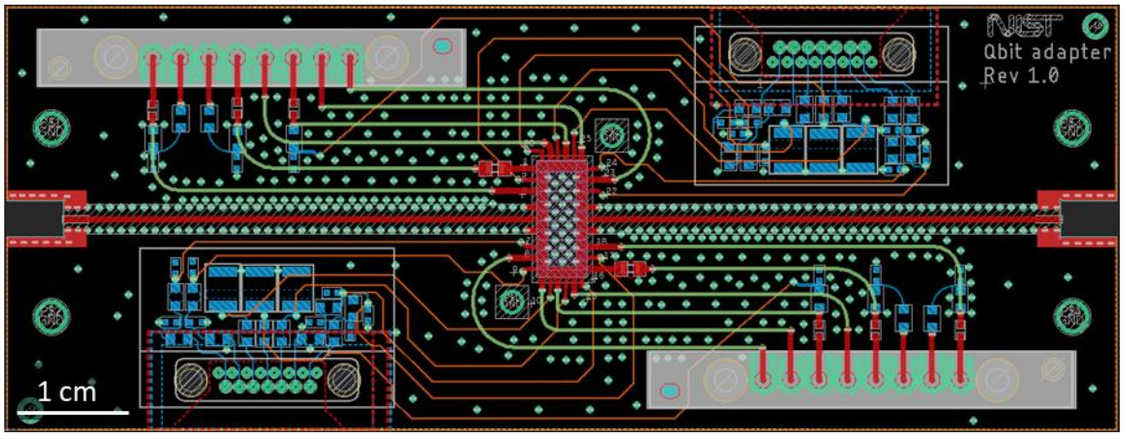

FIG. 6. Layout of the test PCB with six layers for the different frequency and ground planes overlayed with corresponding tracks. DC lines are at the top right and bottom left. Medium frequency lines are at the top left and bottom right. The high frequency CPWs are in the center running lengthwise.

Test structure CPWs were fabricated on silicon chips using standard photolithography and gold deposition techniques at the NIST nanofabrication facility. The

patterns were created at the wafer level with multiple die patterns. A bi-layer resist stack, comprised of LOR 3A and S1813, was spun onto a pre-cleaned undoped wafer. The choice of bilayer resist was to facilitate the lift off process. Optical patterning was done using a direct laser writer with a dose of 90 mJ/cm^2 and developed using MF 319 for a minute followed by a de-ionized (DI) water rinse. We used etching steps on the wafer with an oxygen plasma to ensure that any residual photoresist is removed from the substrate in the patterned area to achieve the necessary surface cleanliness and fidelity of the patterns. We evaporated 5 nm of titanium as a buffer layer followed by 150 nm of gold. Evaporation was carried out using an e-beam evaporator at an angle to avoid conformal coating to provide optimum metal lift off. The lift off was carried out by immersing the chip in Remover PG at 80 °C, followed by rinsing in isopropyl alcohol and DI water. The wafer was then diced to chips to mount on the PCB.

Dimensions of the CPW on the silicon chip were extracted from the COMSOL Geometry menu and copied over to a GDS-II file for standard lithography processing. The larger bonding pads on each end of the CPW were used to connect the signal and ground planes of the PCB CPW and the silicon chip CPW.

The Oersted-antenna device shown in Figure 4 was fabricated using the same photolithography and gold deposition techniques as the silicon chip CPW. Physical parameters and dimensions were once again extracted from the COMSOL Geometry menu and copied over to a GDS-II file for standard lithography processing. A 0.5 μm gap spacing is the smallest feature size we could reliably fabricate using photolithography. Figure 5 shows the test setup including a rendering of the PCB with available mounting slots for mini-SMP connectors that can be attached to each end of a CPW with a fabricated Oersted-

antenna device wire bonded in the central region. Edge-launch mini-SMP to 2.92 mm adapters were utilized to attach 2.92 mm cables to the PCB, which were then measured using a 43 GHz range vector network analyzer.

Figure 7 shows a proof of concept for a fabricated Oersted line perpendicular to a donor dot device. The donor dot devices are fabricated using a STM and atomically precise hydrogen-depassivation lithography methods. Ref. 16 details the fabrication process and design parameters for our donor dots. The placement of the Oersted line is shown perpendicular to the position of the donor dot leads. RF pulses through the Oersted line induce a magnetic field at the donor. If the RF pulse is at the Larmor frequency (around 42 GHz for a 1.5 T applied static magnetic field), then the oscillating magnetic field induced by the Oersted line is expected to drive Rabi oscillations[8].

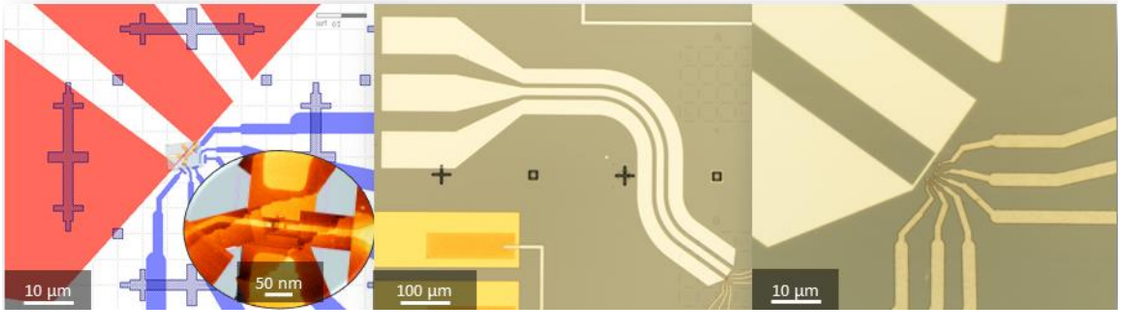

FIG. 7. Fabricated Oersted line perpendicular to a donor dot structure. Left is a GDS-II file and a zoomed-in STM image of our test design. Center and right images show the expected placement of our Oersted line relative to our quantum device which lies ~30 nm below the surface.

IV. RESULTS AND DISCUSSION

The fabricated on-chip CPW and novel Oersted-antenna devices wire bonded to our custom PCB were interfaced to a vector network analyzer. Measured S-parameters are

shown, and the resulting power spectrum of our devices are analyzed. The on-chip CPW measurement results are useful for validating our simulations, and for characterizing the ringing behavior observed. The varying gap distances in our Oersted-antenna devices provide insight into the electromagnetic field power distribution as a function of distance from an ESR line.

S-parameter measurements of our PCB CPW wire-bonded to a silicon chip CPW are shown in Figure 8. Note that the lower transmitted power compared to the simulated result in Figure 2 is due to about 7.5 dB loss from our cabling setup, less than perfect conductance across the signal lines, and additional attenuation caused by variations in wire bonding. S12 and S22 parameters were similar to their counterparts due to symmetry in the design and have been omitted for simplicity.

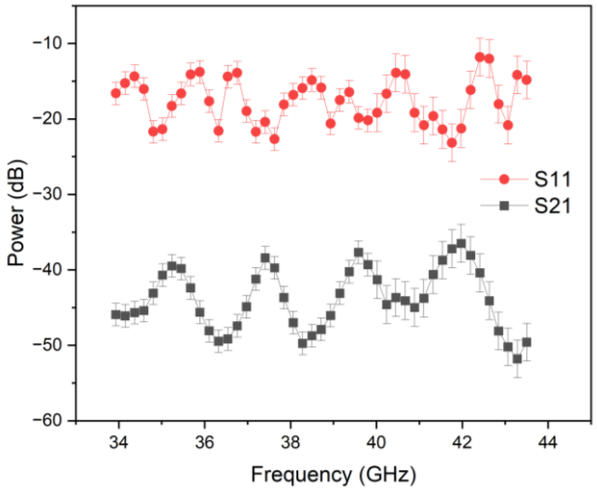

FIG. 8. Measured S-parameters for a PCB CPW wire-bonded to a silicon chip CPW. COMSOL simulation shown in Figure 2 qualitatively shows the expected ripple behavior and slightly greater transmittance at 42 GHz.

The simulation shown in Figure 2 successfully predicts the ripple behavior that was measured for the transmittance and the slightly greater power transmitted at around 42 GHz. From Figure 8, we find the ripple period in the S21 measurement is roughly 2 GHz. Calculating the cavity length, L, from the period, we find that $L = \frac{c}{2\Delta f\sqrt{\varepsilon_r}} \approx 4.3$ cm. This is exactly the distance from the SMP connector on the PCB to the wire bonded edge, which is consistent with the hypothesis that the wire bonded edge is contributing significant reflections along the PCB as shown in Figure 3. Additionally, reflections at the end of the Si chip CPW and slightly mismatched impedances can contribute further non-idealistic behavior.

To characterize the ringing behavior from the cavity, an S21 measurement of the PCB with long wire bonds bridging both CPW ends together was taken. The result is shown as the data labelled PCB in Figure 9(a). We then fabricated several Oersted-antenna devices with variable gap spacings ranging from 0.5 μm to 2 μm (designed as shown in Figures 4 and 5). As simulated in Figure 4(b), the magnetic field magnitude is inversely proportional to the distance. Normalizing the measurement results for the losses caused by the cabling and the PCB CPW (Figure 9(b)), as expected, we find that the transmitted power through the Oersted-antenna spacing shows higher coupling for smaller gap spacing.

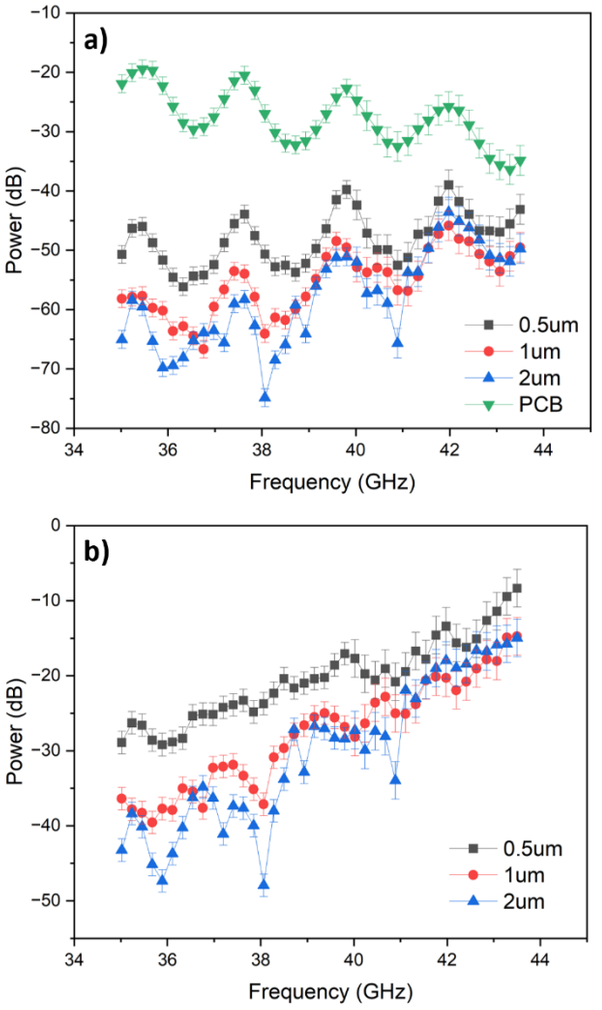

FIG. 9. (a) Measured S21 parameter for several fabricated Oersted-antenna devices with variable center gap spacings. Measurements were taken with the PCB and wire bonded Si chip test setup. The S21 measurement of the PCB with long wire bonds bridging both CPW ends together is included. (b) Results have been normalized to take into account cabling and PCB induced losses by subtracting the data labelled as PCB from the variable gap spacing measurements. Higher frequencies and smaller gap spacings increase transmittance.

Using longer wire bonds leads to greater attenuation as frequency increases in the 35-45 GHz range[8]. This is observed in the data labelled as PCB in Figure 9(a). When

normalizing the data to reduce the ripple effect induced by the PCB and cavity effect, the approximately 20 dB power gain over the 10 GHz range shown in Figure 9(b) is in part due to the increased attenuation of the longer wire bonds in the base measurement of the pass-through PCB CPWs. The remainder of the power gain can be attributed to an inverse proportionality between frequency and impedance of the gap spacing in this frequency range.

The measured power of -15 dB at around 42 GHz in the normalized dataset corresponds to a magnetic field on the order of several millitesla at our quantum dot device interface. This is consistent with our modelled magnetic field distribution displayed in Figure 4 showing roughly 10 mT to 30 mT at the antenna line. Although slightly higher than prior published work simulating high frequency nanoscale microwave ESR lines[8], our simulation does not account for any losses due to cabling. Hence, the input power of the device simulated in Figure 4 is greater than would be for a physical device.

V. SUMMARY AND CONCLUSIONS

We have presented a comprehensive study on designing, modelling, and fabricating on-chip coplanar waveguides and Oersted-antenna structures, which was motivated by high frequency electron spin manipulation experiments in silicon quantum dot devices.

We have introduced a novel design for coupling Oersted lines to a symmetrical antenna on the opposing side of a silicon chip device for the purpose of monitoring electromagnetic field strength while sending RF pulses down the line. Finite element modelling software can be utilized to model and qualitatively predict behavior of S-parameters and electromagnetic fields of our experimental test setup including a PCB,

silicon chip device, and wire bonds. This is extremely useful during the design process and confirming any non-idealistic behavior, such as ringing at high frequencies caused by cavity effects.

The Oersted-antenna coupled device allows us to understand the magnetic field distribution around the ESR line. We have shown the power distribution across the gap spacing is inversely proportional to distance and corresponds to a magnetic field on the order of several millitesla, which plays an important role in determining the placement of a quantum dot device relative to the ESR line. This lays the groundwork necessary for characterizing high frequency Oersted lines needed to drive Rabi oscillations for silicon donor dot devices. The preliminary investigation of a magnetic force measurement pertaining to the field strength induced by an ESR line within the silicon substrate at the device interface shows promising results and is under further investigation.

We anticipate that our novel design and test setup presented in this manuscript will prove useful towards optimizing high frequency microwave circuitry for spin manipulation in single dopant atomic scale quantum devices.

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AUTHOR DECLARATIONS

Conflicts of Interest

The authors have no conflicts to disclose.

Author Contributions

M. Gaunin and P. Namboodiri contributed equally to this work.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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