

Autonomous bootstrapping of quantum dot devices

Anton Zubchenko,^{1,2} Danielle Middlebrooks,³ Torbjørn Rasmussen,¹ Lara Lausen,¹
Ferdinand Kuemmeth,^{1,4,5} Anasua Chatterjee,^{1,2} and Justyna P. Zwolak^{3,6,7,*}

¹*Center for Quantum Devices, Niels Bohr Institute, University of Copenhagen, Copenhagen 2100, Denmark*

²*QuTech and Kavli Institute of Nanoscience, Delft University of Technology, Delft, The Netherlands*

³*National Institute of Standards and Technology, Gaithersburg, MD 20899, USA*

⁴*Institute of Experimental and Applied Physics, University of Regensburg, 93040 Regensburg, Germany*

⁵*QDevil, Quantum Machines, 2750 Ballerup, Denmark*

⁶*Joint Center for Quantum Information and Computer Science,
University of Maryland, College Park, MD 20742, USA*

⁷*Department of Physics, University of Maryland, College Park, MD 20742, USA*

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Semiconductor quantum dots (QDs) are a promising platform for multiple different qubit implementations, all of which are voltage controlled by programmable gate electrodes. However, as the QD arrays grow in size and complexity, tuning procedures that can fully autonomously handle the increasing number of control parameters are becoming essential for enabling scalability. We propose a bootstrapping algorithm for initializing a depletion-mode QD device in preparation for subsequent phases of tuning. During bootstrapping, the QD device functionality is validated, all gates are characterized, and the QD charge sensor is made operational. We demonstrate the bootstrapping protocol in conjunction with a coarse-tuning module, showing that the combined algorithm can efficiently and reliably take a cooled-down QD device to a desired global-state configuration in under 8 min with a success rate of 96 %. Finally, by following heuristic approaches to QD device initialization and combining the efficient ray-based measurement with the rapid radio-frequency reflectometry measurements, the proposed algorithm establishes a reference in terms of performance, reliability, and efficiency against which alternative algorithms can be benchmarked.

I. INTRODUCTION

Gate-defined quantum dots (QDs) in semiconductors present a promising avenue toward building high-fidelity and scalable quantum processors using existing industrial infrastructure [1–15]. However, due to the gate-defined and gate-controlled nature of spin qubits based on QDs, effective tuning within the large-dimensional gate-voltage landscape is becoming a key limitation to qubit array operation [16]. Previous work has made progress in areas such as topology and charge-state classification [17–19], navigation in higher-dimensional gate-voltage spaces using ray-based tuning [14, 20], and optimization of readout and qubit fidelity [21, 22]. However, most algorithms assume that previous tuning steps, such as the definition of the QD(s) channel(s), calibration of the charge sensor(s), or identifying regions of interest within the coarse-tuning regime, have been completed [18–20].

In this work, we focus on the task of fully autonomous bootstrapping of the QD device, where “bootstrapping” is defined as a pretuning process that brings the device to an operational regime in which the coarse-tuning stage can be initiated [16, 18]. The proposed bootstrapping algorithm is designed to be initiated on a pristine QD device post-cooldown in the two-dimensional electron gas (2DEG) limit. While previous work has proposed a machine-learning- (ML) based approach to QD device initialization [23], our algorithm instead takes advantage of physics-based heuristics whenever possible. The reason we choose to rely on domain knowledge rather than ML methods is that, at present, even the

best-performing ML models are limited in their interpretability, making it challenging to determine how the QD device should be adjusted in the case of failure. Moreover, low signal-to-noise ratio and other data imperfections can significantly affect the validity of ML predictions, causing unexpected failures of the tuning protocol. Finally, automating bootstrapping following heuristic approaches allows us to establish a reference in terms of performance, reliability, and efficiency against which alternative, possibly more ML-heavy, algorithms can be benchmarked. Thus, the procedural flow of the proposed bootstrapping algorithm closely follows the typical manual-tuning steps of a QD device. Moreover, to improve the tuning efficiency and reliability, our algorithm utilizes a proximal charge sensor [24], measured in radio-frequency (rf) reflectometry, instead of transport measurements used in previous work [25].

The bootstrapping process starts after cooling the device down to a few millikelvins and involves determining the operational ranges, determining charging energies for each quantum dot (QD), and making the local charge-sensing system operational. In Fig. 1(b), we depict the flow of the tuning protocol reported in this work. The procedural flow of the bootstrapping algorithm is shown in Fig. 1(c).

Preparation. The first, preparatory stage [teal box in Fig. 1(c)] consists of setting the backbone (BB) gate to localize the operational region, followed by testing and setting the Ohmic to a voltage that corresponds to the target current.

Diagnostics and characterization. With the bias on the Ohmic set, the protocol proceeds with diagnostics and characterization of the device finger gates [light blue box in Fig. 1(c)]. At this stage, the algorithm tests whether all relevant gates are functional and collects pinch-off and saturation

* jpzwolak@nist.gov

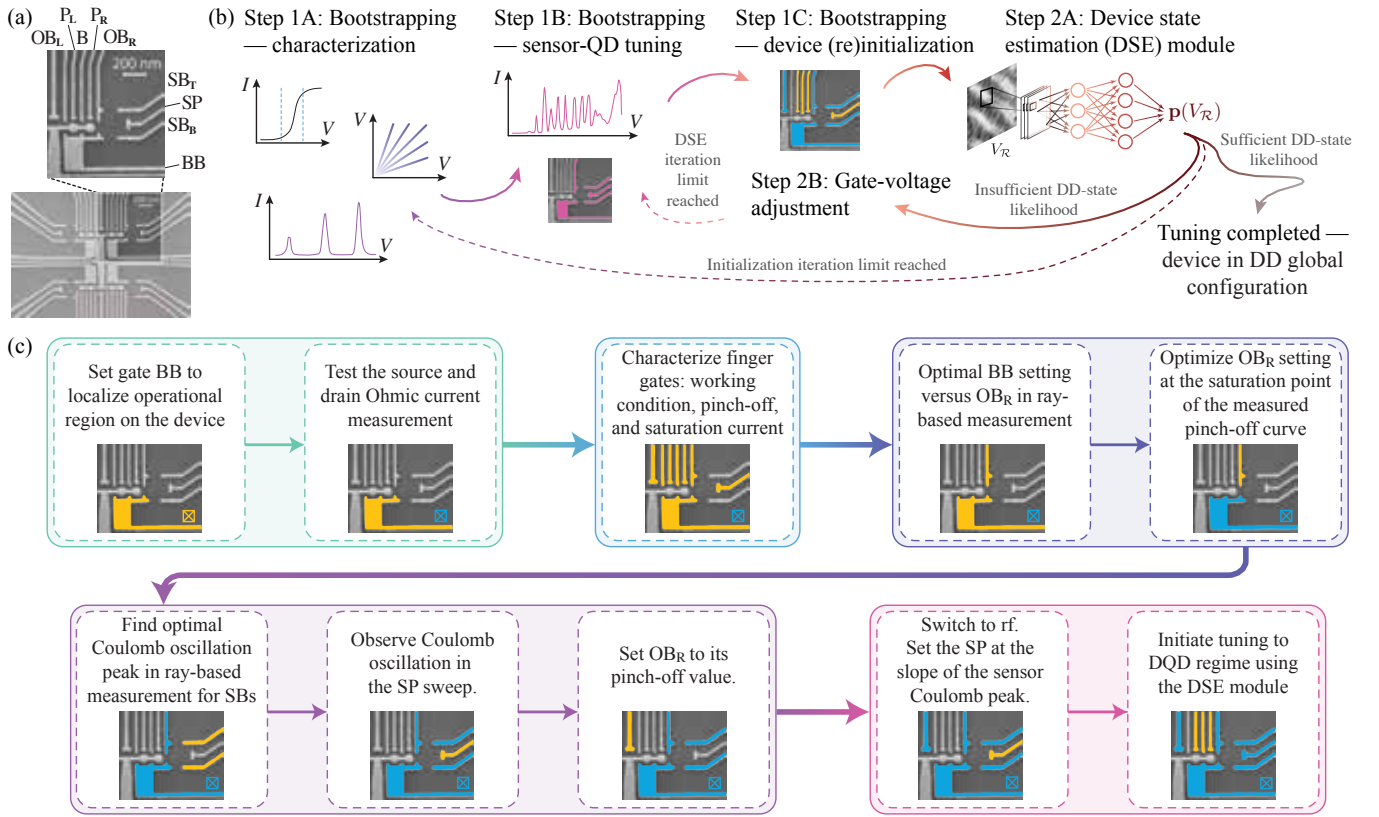


FIG. 1. (a) A scanning electron micrograph (SEM) of a gate-defined, depletion-mode GaAs/Al_{0.36}Ga_{0.64}As device used to demonstrate the bootstrapping protocol. The gates are labeled as follows: P_L, P_R, and SP for the left, right, and sensor plunger, respectively; OB_L, OB_R, B, SB_T, and SB_B for the outer left, outer right, middle, sensor top, and sensor bottom barrier, respectively; and BB for the backbone gate. (b) A conceptual overview of the tuning protocol. The bootstrapping process, depicted in steps 1A–1C, is followed by the device state estimation module (DSE; step 2A) [17, 18], and (optional) gate-voltage adjustment (step 2B). Steps 2 and 3 are interleaved with an optimization protocol and, if necessary, repeated characterization and reinitialization, to iteratively adjust voltages until the DSE module declares the device to be in a double-dot (DD) state. (c) The procedural flow of the bootstrapping algorithm. The algorithm begins with the preparatory stage and setting the BB gate (teal box), followed by the device diagnostics and characterization of the finger gates stage (light blue box), defining of the sensor-QD- and qubit-QD-channels stage (dark blue box), a configuration of the outer barrier gates (purple box), and the sensor-tuning stage (pink box).

voltages where applicable. Should any of the finger gates be flagged as non-functional, the bootstrapping process is terminated.

Defining QDs channels. Defining the sensor-QD and qubit-QD channel [dark blue box in Fig. 1(c)] begins from a pinched-off current using the BB and right outer barrier (OB_R). Then, the OB_R is fine tuned to the saturation point of the measured current.

Setting up charge sensor. The final stage of bootstrapping consists of two parts. With the BB and OB_R set, the algorithm first sets the sensor barrier gates (SB_T and SB_B) based on Coulomb oscillation in ray-based (rb) measurement and then the left outer barrier (OB_L) in the qubit-QD channel to its pinch-off [purple box in Fig. 1(c)]. Finally, the measurement system switches to rf reflectometry, and the sensor plunger (SP) is calibrated [pink box in Fig. 1(c)].

Once the bootstrapping process is completed, the tuning algorithm initiates the coarse tuning [16, 18]. The goal of coarse tuning is to find a range of gate voltages where the device is

in a particular global configuration, i.e., a single-dot (SD) or double-dot (DD) state.

We show that the proposed bootstrapping approach can be highly successful, with 86.5 % of test runs successfully preparing the device for coarse tuning. Given the rapid acquisition of data and its efficient analysis, our algorithm is capable of tuning the double-QD device within about 8 min. Moreover, using the parameters gathered during bootstrapping, we show a 96.6 % success rate for coarse tuning, preparing the QD device for further calibration toward qubit operation.

Finally, we demonstrate the cross-platform applicability of the ML model used in the coarse-tuning module, which, thus far, has only been deployed on Si/Si_xGe_{1-x} QD devices with an overlapping gate architecture [17–19, 26]. This work is, therefore, also a demonstration that an ML algorithm trained exclusively using synthetic data [27] can be successfully used to assess the state across various device designs.

The remainder of the paper is organized as follows: In Sec. II, we give an overview of the design of the bootstrapping

ping protocol. The specifics of the algorithm and its configuration for all tests in this work are described in Secs. II A–II D. The performance at the level of individual stages in bootstrapping is presented in Sec. III A. The overall performance of the tuning algorithm in reaching the target global configuration is discussed in Sec. III B. We conclude with a discussion of the potential modifications to further improve the proposed bootstrapping technique in Sec. IV.

II. METHODOLOGY: EXPERIMENTAL SETUP

Bootstrapping is initiated with a configuration file that defines the device architecture, identifies the quadrant that will be used in the experiment, defines the functionality of the gates (e.g., labeling gates as barriers or plungers), and specifies the safety ranges of the device. A scanning electron micrograph (SEM) of a gate-defined, depletion-mode GaAs/Al_{0.36}Ga_{0.64}As device used to demonstrate the bootstrapping protocol is shown in Fig. 1(a) [28]. The two-dimensional electron gas (2DEG) is formed 57 nm below the surface. The device, shown in Fig. 1(a), consists of four identical quadrants, each with tunable metallic electrodes for forming two QDs for hosting qubits and a larger sensor QD. Barrier gates [OB_L, B, OB_R, SB_T, and SB_B in Fig. 1(a) for the outer left, middle, outer right, sensor top, and sensor bottom barrier, respectively] confine each of the QDs, while plunger gates [P_L, P_R, and SP in Fig. 1(a) for the left, right, and sensor plunger, respectively] control their chemical potentials. The backbone gate and an appropriate separator gate [BB and OB_R in Fig. 1(a)] are used to isolate the quadrant of interest. The separator gate is also used as a barrier for one of the qubit QDs as the designated gate was dysfunctional. Each quadrant has two Ohmic contacts to the 2DEG which are also connected to an off-chip resonator. The Ohmics are used to measure the current through the 2DEG. The resonator and sensor QD form an RLC circuit for rf-reflectometry measurements.

The experiment is conducted in the dilution fridge at roughly 30 mK. The Quantum Machines QDAC-II is used to set the bias on the source Ohmic, as well as to perform voltage sweeps of the gates. The current measurements are acquired and converted into voltage readings using an Ithaco 1211 current preamplifier before being fed into a Keysight 34465A 6.5 digital multimeter. Finally, the rf-reflectometry measurements for the DSE-based tuning protocol are acquired using a Quantum Machines OPX tuned to 273.8 MHz, the resonant frequency of the selected quadrant.

A. Bootstrapping: Preparation

Once the device is cooled down, the preparatory stage begins [teal box in Fig. 1(c)]. The localization of the operational quadrant is achieved by setting the BB gate to the most negative safe voltage of the gate. Then, with all gates set to zero, the bias voltage is swept to test for Ohmic behavior. If the expected linear relationship between the voltage bias and the measured current is observed, the Ohmic is biased to the

voltage where a small positive current of about 10 nA can be observed. This amperage was determined during the manual prescreening to be both safe for the device, and sufficiently high for measurements using the experimental setup described in Sec. II.

B. Bootstrapping: Diagnostics and characterization

With the bias on the source Ohmic set, the algorithm proceeds to assess the functionality of the finger gates in the quadrant, as shown in the light blue box in Fig. 1(c). This is achieved by applying a voltage to each gate, one at a time, and measuring the current through the device. Ideally, the voltage versus current signal should have a sigmoidal shape. However, the device imperfections may lead to curves that more or less significantly violate this assumption, as can be seen in Fig. 2(b).

The analysis of the current versus voltage signal serves several purposes. First, it is a diagnostic tool that verifies whether gates are functional and the device is suitable for tuning. Finger gates are classified as working if they produce a current versus voltage signal with a sufficiently wide distribution, as quantified by the median absolute deviation (MAD). The MAD is compared to the threshold value that is expected to be higher than the experimental setup noise levels determined from the device prescreening to be less than 1 % of the target current.

Second, all the relevant gate characteristics, such as pinch-off, saturation, and parking values, are determined as part of the bootstrapping process. To determine the pinch-off and saturation values, we consider the first (dI/dV) and the second (d^2I/dV^2) derivative of the current versus voltage signal, respectively. Prior to analysis, the gradient of the signal is first smoothed with a Gaussian filter and then fitted with an inverse cosine hyperbolic function of the form

$$f(x) = \frac{a}{\cosh^2[b(x-x_o)]} + y_o, \quad (1)$$

where a , b , x_o , and y_o are fit parameters used for a *post-hoc* analysis [29]. The location of the minimum-voltage prominent peak in the dI/dV curve defines the pinch-off value. The saturation point value is defined at the location of the maximum-voltage negative prominent peak of the d^2I/dV^2 . The prominence assessment is used to identify stand-out features. For finding the pinch-off and saturation values, calculated prominence values are used to filter the peaks arising from the experimental setup noise. Additionally, prominence analysis is used for finding and narrowing down the candidate list of optimal Coulomb oscillation peaks during the sensor-QD tuning that uses a threshold value corresponding to 1 % of the target current (see Sec. II D).

C. Bootstrapping: Defining QDs channels

With all gates characterized, the bootstrapping algorithm proceeds to define the QDs channels [dark blue box in

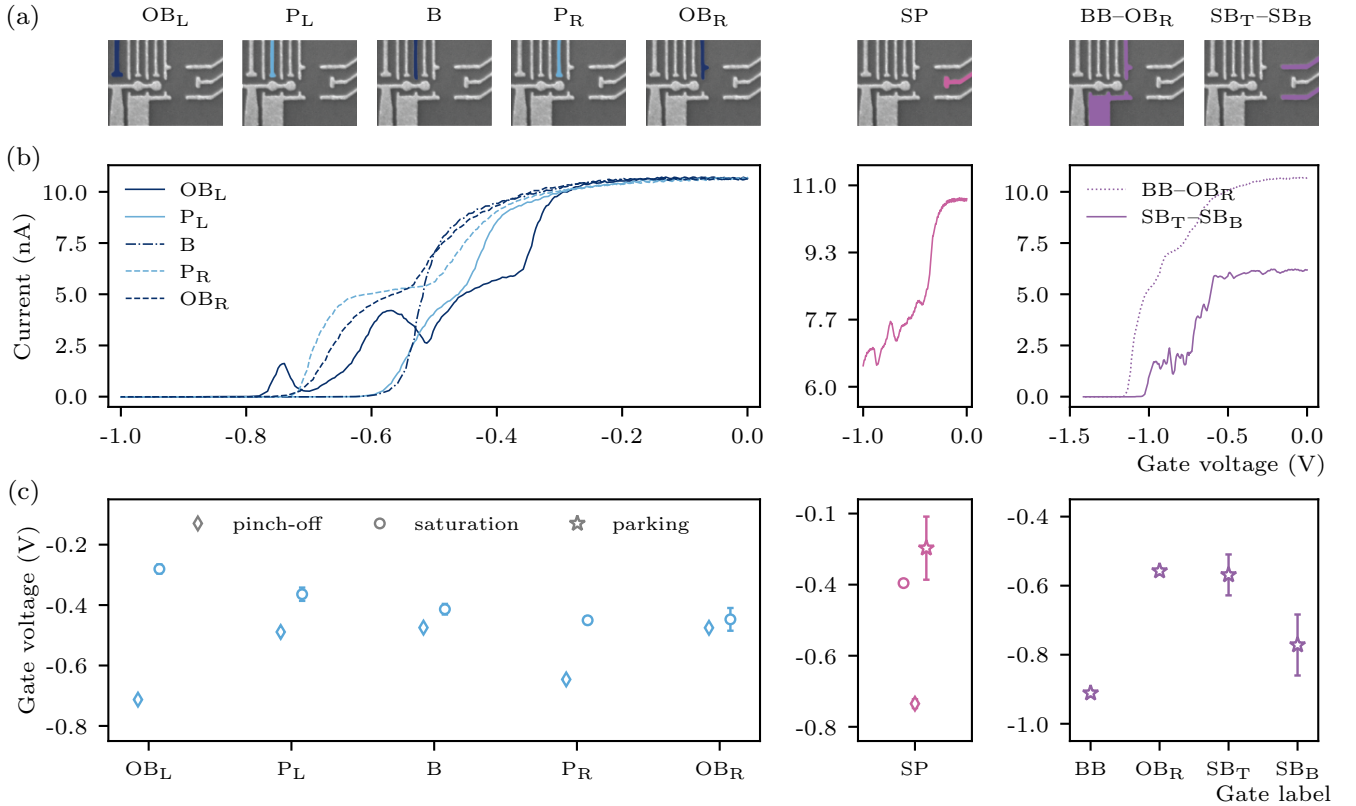


FIG. 2. (a) SEMs highlighting finger gates characterized during the bootstrapping process. (b) Sample voltage versus current plots for the finger gates depicted in panel (a). The OB_L gate measures Coulomb oscillations due to the formation of a QD between OB_L and OB_R . The BB , OB_R , SB_T , and SB_B gates are set as a result of ray-based (rb) measurement. SB_T versus SB_B measures Coulomb oscillations due to setting sensor-QD barriers. The BB versus OB_R rb measurement analyzes the current trace and finds the current saturation point: the gates are then parked at the voltage at which saturation is reached. The palette corresponds to the colors used to highlight gates in panel (a). (c) Consistency plots showing the mean values and standard deviations for the characteristics of interest, averaged over $N = 89$ test bootstrapping runs. For gates OB_L , P_L , B , P_R , OB_R , and SP , the pinch-offs and saturation values are collected. For SP , BB , OB_R , SB_T , and SB_B , the parking-value statistics are collected. For the SP , the parking value corresponds to the position on the most sensitive Coulomb peak position found with rf reflectometry. The final configuration for P_L , B , and P_R are established during the coarse-tuning stage. The error bars indicate one standard deviation. However, their respective pinch-offs and saturation points are used to determine the starting position for the initialization of the DSE module.

Fig. 1(c)]. The goal of this step is to adjust the BB and OB_R gates to split the QD device quadrant into the sensor-QD and qubit-QD channels.

To find the combined voltages for BB and OB_R that pinch off current, the algorithm utilizes the rb measurement instead of the conventional 2D scans. The rb approach involves measuring a collection of one-dimensional (1D) voltage sweeps initiated from a common starting point $(V_{BB}, V_{OB_R}) = (0, 0)$ at a tilt from the central measurement axis, defined as the straight line to $(V_{BB}, V_{OB_R}) = (-1, -1)$. The tilt angles, set at seven evenly spaced orientations in a range between 0.2π and 0.3π , are chosen to increase the likelihood of observing the current pinch-off. The algorithm picks the angle for which the pinch-off voltage is the lowest, decomposes the optimal pinch-off voltage into the BB and OB_R voltage components, and then sets the BB gate based on this decomposition.

With BB calibrated, a full trace of the OB_R gate is measured and OB_R is parked at the position of the peak in the dI/dV

with the highest current for sustaining transport through the QDs.

D. Bootstrapping: Setting up charge sensor

Once the current channels are established, the protocol proceeds with tuning the outer barrier gates for both the sensor and qubit QDs [purple blue box in Fig. 1(c)]. With the BB and OB_R gates calibrated and the SP gate parked at 0 V, rb measurement is conducted for SB_T versus SB_B in a similar fashion as for BB versus OB_R .

The goal of this stage is the detection of the Coulomb blockade induced by the formation of the sensor QD, manifested through oscillations in the current sweep measured on the SP gate. If oscillations are absent in all rays, the protocol is programmed to abort the run and restart. For all rays where the oscillations are detected, all peaks are analyzed to find one

that is most likely to lead to a high sensitivity of the sensor.

All detected peaks are first filtered to remove overlapping peaks from further analysis. Then, the remaining peaks are ordered according to a score function inspired by Ref. [30]:

$$S = h \frac{2}{1 + hw/hw_0}, \quad (2)$$

where h is the peak height, hw is the full width at half maximum of the peak, and $hw_0 = 10$ mV is an expected full width at half maximum for the device type used to test the bootstrapping algorithm [30]. The h and hw are determined based on the prominence analysis described in Sec. II B.

Once the most promising peak is determined, SP is put back into the open position, and the OB_L is swept to localize qubit QDs. Again, if oscillations are observed, the qubit QD has been successfully confined and, thus, it is possible to split it with the B gate to form DD. We then proceed to turn on the rf-reflectometry setup for charge sensing. To achieve the best sensitivity, the plunger needs to be parked at the largest slope of the signal reflected off the sensor QD. In this way, small shifts in the DD capacitances due to electron transitions can be observed.

E. Coarse tuning

Once the bootstrapping module is completed, the coarse-tuning stage begins [16, 18]. The finger-gate characteristics from bootstrapping are used to define the operational regime by limiting the range over which gates P_L , B, and P_R can be adjusted. The DSE-based tuning module is then initiated at voltages of the P_L , B, and P_R gates randomly selected from a uniform distribution between $V_{\text{saturation}} + \gamma$ and $V_{\text{saturation}} - \gamma$ for each respective gate, where $\gamma = V_{\text{saturation}} - V_{\text{pinch-off}}$. Proper scaling of the measurement scans is crucial for meaningful network analysis: scans that are too small may not contain enough features necessary for state classification, while scans that are too large may result in probability vectors that are not useful in the navigation phase. The size of the scans is determined based on the charging energies extracted during the diagnostics and characterization phase. The scan size is set to match roughly 1.5 times the initial charging energies of individual QDs in the qubit-QDs region of the device, as suggested in Ref. [26].

The navigation algorithm within the DSE-based module is driven by the distance between the state vector describing the target state $\mathbf{p}_{\text{target}}$ and the state vector $\mathbf{p}(V_{\mathcal{R}})$ predicted for current measurement. The state vector quantifying the current state of the device is defined as

$$\mathbf{p}(V_{\mathcal{R}}) = [p_{\text{ND}}, p_{\text{SD}_R}, p_{\text{SD}_C}, p_{\text{SD}_L}, p_{\text{DD}}], \quad (3)$$

with ND indicating no QDs formed, SD_R , SD_C , and SD_L denoting the right, central, and left single QD, respectively, and DD denoting the double-QD state.

The distance between the two state vectors is defined as:

$$\delta[\mathbf{p}_{\text{target}}, \mathbf{p}(V_{\mathcal{R}})] = \|\mathbf{p}_{\text{target}} - \mathbf{p}(V_{\mathcal{R}})\|_2 + \varepsilon(V_{\mathcal{R}}), \quad (4)$$

where $\|\cdot\|_2$ is the Euclidean norm and $\varepsilon(\cdot)$ is a penalty function for tuning to larger plunger voltages [18, 20]. The penalty is determined dynamically as a function of the distance to the middle of the operational regime defined by the bootstrapping.

Depending on the outcome of the DSE module, the algorithm can take one of three actions. If the distance between $\mathbf{p}_{\text{target}}$ and $\mathbf{p}(V_{\mathcal{R}})$ falls below a predefined threshold δ_{tr} , the tuning process is terminated and the device is declared to be in a DD global configuration. The choice of δ_{tr} translates directly to how close in the state space the final point is to the DD region. By default, $\delta_{\text{tr}} = 0.3$, which means that the estimated likelihood of the DD regime within the measurement is at least 85 % DD state.

If the distance between $\mathbf{p}_{\text{target}}$ and $\mathbf{p}(V_{\mathcal{R}})$ surpasses the predefined threshold, i.e., $\delta[\mathbf{p}_{\text{target}}, \mathbf{p}(V_{\mathcal{R}})] > \delta_{\text{tr}}$, and the DSE module iteration limit has not been reached, the gate voltages for the plunger gates are adjusted [step 2B in Fig. 1(b)]. The navigation is driven by the action-based algorithm proposed in Ref. [19].

This process is repeated until either the DD state is declared or the DSE module iteration limit is reached. Reaching the DSE module iteration limit triggers recalibration of the sensor QD, which is followed by reinitialization of the DSE module. By default, the iteration limit is set to 10. The reinitialization involves finding new starting values for P_L , B, and P_R . This is done by resampling the uniform distributions around saturation points for all three gates.

Finally, if $\delta[\mathbf{p}_{\text{target}}, \mathbf{p}(V_{\mathcal{R}})] > \delta_{\text{tr}}$, the DSE module iteration limit has been reached, and the reinitialization iteration limit has been reached, the bootstrapping is restarted. The autotuning is considered successful if the optimizer converges to a voltage range that gives the expected DD configuration when evaluated by human experts.

III. RESULTS

The evaluation of the tuning algorithm is carried out in two phases. In the first phase, we test the performance of the individual steps of the bootstrapping algorithm. In the second phase, we perform a series of trial runs of the full autotuning

TABLE I. The summary statistics for pinch-off, saturation, and parking voltages for all finger gates assessed during the bootstrapping tests, averaged over $N_{\text{boot}} = 89$.

Gate	Pinch-off (mV)	Saturation (mV)	Parking (mV)
OB_L	-762.9(2.1)	-330.6(15.3)	...
P_L	-539.0(1.3)	-414.0(22.0)	...
B	-524.6(1.1)	-500.4(12.4)	...
P_R	-696.0(1.4)	-463.7(17.6)	...
OB_R	-525.2(0.9)	-497.3(37.6)	-507.5(1.4)
SP	-768.6(15.4)	-344.6(8.1)	-221.7(111)
BB	-861.1(5.3)
SB_T	-518.9(59.2)
SB_B	-721.9(88.3)

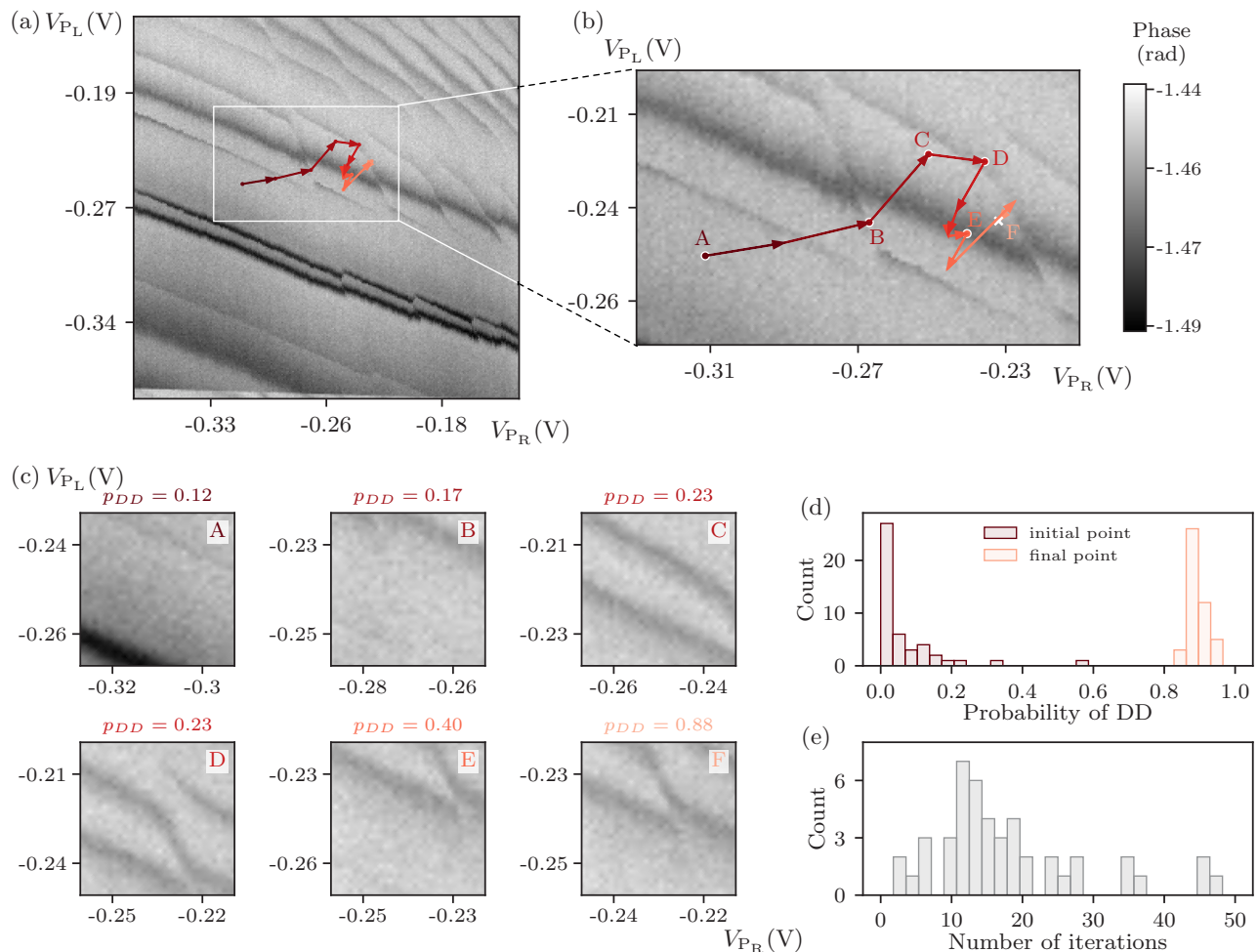


FIG. 3. (a) An overview of the sample run of the autotuning protocol implemented with active feedback in the larger space of plunger gates (V_{P_R}, V_{P_L}). (b) A close-up of a charge stability diagram showing a sample 12-step path of the coarse-tuning module with active feedback in the space of plunger gates (V_{P_R}, V_{P_L}). The arrows and the intensity of the color indicate the progress of the autotuner (dark to light). (c) The measured raw scans in the space of plunger gates (V_{P_R}, V_{P_L}) showing data available to the DSE module for six selected steps along the path shown in panel (a). The p_{DD} corresponds to the evaluated likelihood of the DD regime. (d) The DD likelihood of initial and final points. (e) The distribution of path lengths across the 46 test runs.

algorithm in the (V_{P_R}, V_B, V_{P_L}) space, with the B gate adjusted as described in Sec. II C.

A. Bootstrapping: Performance analysis

We initialize $N_{boot} = 89$ bootstrapping runs to test the performance of the autonomous bootstrapping algorithm presented in Fig. 1(b). In each test run, we extract the results of 1D gate characterization as well as the final sensor-QD gate voltages obtained using rb measurements.

The finger-gate characterization identifies working gates, and extracts pinch-off and saturation voltages. The five panels in the leftmost column in Fig. 2(a) identify on the device SEM the finger gates used to form and control qubit QDs: $OB_L, P_L, B, P_R,$ and OB_R . The corresponding 1D gate traces are shown in Fig. 2(b) and the extracted pinch-off and saturation voltages averaged over the $N_{boot} = 89$ tests are shown in Fig. 2(c).

The error bars in Fig. 2(c) represent one standard deviation within the collected sample and provide a metric of algorithm and device stability. High device and algorithm stability manifest through the low standard deviations of the extracted features: for the pinch-off, values range from $-762(2)$ mV [31] for OB_L to $-525(1)$ mV for B; saturation values range from $-500(12)$ mV for B to $331(15)$ mV for OB_L . A summary of statistics for all finger gates is presented in Table I.

The middle column in Fig. 2(a) highlights the SP gate on the SEM. An example of a 1D trace used to extract pinch-off and saturation voltages is shown in Fig. 2(b). The average pinch-off and saturation values collected at the characterization stage, as well as the parking positions obtained by detecting the most sensitive position on the highest-scoring [according to the Eq. (2)] Coulomb peak in rf reflectometry after the formation of the sensor QD and the localization of the DD region is concluded, are depicted in Fig. 2(c). The standard deviations for pinch-off and saturation values of the

SP gate extracted from current measurements are found to be 15 mV and 8 mV, respectively (for details, see Table I). The standard deviation for the SP position selected on the highest-scoring Coulomb oscillation peak and parking at its steepest slope was at 111 mV. Since pinch-off values are more well-defined physically, with the slope being steeper than at saturation, we expected the standard deviation of saturation values to be higher than those of pinch-offs.

The two panels in the rightmost column in Fig. 2(a) show the pairs of gates used to form a sensor QD. In Fig. 2(b), we show the analyzed rb measurements and in Fig. 2(c), we show the statistics for the parking voltages in (c). The parking voltages for the BB, SB_T, and SB_B gates have been obtained using rb measurements, with the corresponding 1D traces shown in the rightmost panel in Fig. 2(b). The parking voltage for the BB gate is the result of detecting a pinch-off in rb measurement taken in combination with OB_R [for performance statistics, see Fig. 2(c)]. The OB_R is the result of the succeeding fine tuning, as described in Sec. II C. Finally, the parking positions of the sensor barriers correspond to the location of the most sensitive Coulomb oscillation peak [see Fig. 2(c)]. In this case, the dependence on the oscillatory behavior has resulted in a larger standard deviation of the parking voltages for the SB_T and SB_B gates, at 59 mV and 88 mV, respectively, than for BB and OB_R, which rely on the well-behaving pinch-off values.

To test the bootstrapping performance, we measure a large charge stability diagram in the (V_{P_R}, V_{P_L}) plunger space, with $V_B = -500$ mV to qualitatively confirm that the qubit QDs can be sensed with the sensor QD. The choice of V_B comes from prior work [32]. Out of 89 bootstrapping test runs, 12 were unsuccessful at charge sensing the qubit QDs. Among these 12 failed tuning attempts, 10 had an uncharacteristically high parking voltage for the OB_L that provided an insufficient current pinch-off to form the left QD, and two remaining runs failed to detect the Coulomb oscillations in the rb measurements for SB_T versus SB_B measurements, and thus no sensor QD could be formed. The discovered failure modes have provided an experimental heuristic for invoking the sensor-QD re-tuning from the initial device state that was implemented for the full tuning protocol discussed in Sec. III B.

B. Full tuning: performance analysis

Once the bootstrapping algorithm had been validated, the algorithm was expanded to include an active coarse-tuning feedback routine for calibrating the V_{P_L} , B, and V_{P_R} gates to bring the QD device to a DD state [see Fig. 1(b)]. The full tuning testing involves running the bootstrapping algorithm followed by the DSE-based coarse-tuning module as a single protocol, with the DSE module relying exclusively on rf reflectometry.

The performance assessment for full tuning focuses on successful tuning to the DD state based on the outcome of the successful bootstrapping phase. Given the random initialization of the coarse tuning, configurations of the individual gates after bootstrapping are re-used to perform multiple attempts at

qubit DD tuning with randomized initial V_{P_L} , V_{P_R} , and B gate voltages. In cases when the DSE-based module reaches the initialization iteration limit, the algorithm restarts bootstrapping. A total of $N_{\text{full}} = 46$ complete runs are collected for further analysis.

In Fig. 3(a), we show an overview of a sample coarse-tuning run with active feedback in the (V_{P_R}, V_{P_L}) plunger gate space. A close-up of the tuning path is shown in Fig. 3(b). In this example, the QD device is initialized in a configuration corresponding to the SD_L state, with $\mathbf{p}(V_{\mathcal{R}}) = [0.2, 0.0, 0.0, 0.7, 0.1]$. Then, through an iterative application of the DSE module along with the navigation routine, the configuration of the plunger gates is adjusted to bring the QD devices to the target DD state. In Fig. 3(c), we depict six (38×38)—mV scans with (30×30)—pixels resolution taken along the tuning path, indicating an increased likelihood of the DD state as the algorithm navigates toward the DD state.

Out of $N_{\text{full}} = 46$ full tuning algorithm runs terminated at a gate configuration with the DD likelihood of the $\mathbf{p}(V_{\mathcal{R}})$ state vector surpassing the predefined threshold of 85 %, two were qualitatively assessed as false positives. All remaining test runs were successful. While human experts might have been able to recover a DD state from these failed positives, in the time spent recovering, the algorithm could possibly have tuned from scratch again. The probability distributions of the DD likelihood for the initial and the final state vectors are shown in Fig. 3(d). The histogram in Fig. 3(e) shows the number of iterations it took for this algorithm to find the target state. We find a slight correlation between the probability of DD in the initial scan and the number of iterations. In particular, while for test runs with $p_{\text{DD}}^{(\text{init})} < 0.11$ the number of iterations goes up to $N_{\text{iter}} = 47$, for $p_{\text{DD}}^{(\text{init})} > 0.11$, $N_{\text{iter}} < 21$. The average time spent by the algorithm from starting bootstrapping until termination by successful tuning to the DD state was 7.7 min, with 5.7 min spent on bootstrapping and about 2 min on tuning. This compares very well with human expert tuning which, typically requires hours to reach charge sensing of double QDs [23].

IV. SUMMARY AND OUTLOOK

We propose and experimentally demonstrate a modular autonomous bootstrapping algorithm for bringing a GaAs spin-qubit QD device from a completely untuned state to the DD global-state configuration. The algorithm performs gate characterization and device diagnostics, ensures the formation of a qubit-QD channel, and prepares the charge sensing QD for rf reflectometry. The low initialization failure rate and high consistency of the saturation and pinch-off voltages confirm the stability of the algorithm. The bootstrapping protocol efficiently deploys a combination of measurement techniques such as regular 1D voltage sweeps and rb measurements for the current sweeps and small and fast 2D sweeps using rf reflectometry, improving over previous demonstrations in the field that have used transport measurements. Moreover, the high success rate for tuning to the DD global-state configura-

tion confirms the utility of the ML-based DSE module, trained exclusively using simulated data, for deployment across varying device architectures and materials.

The ability to perform autonomous tuning in charge sensing is especially important for dense arrays without access to individual transport measurements for each QD. The results presented in this work serve as a baseline for the development of a fully autonomous QD device initialization, calibration, and control system for large 1D and 2D QD arrays. The next steps include incorporating data quality control modules to improve the reliability of the ML-based methods and integrating the charge-tuning and fine-tuning modules necessary for a full tune-up to the qubit stage. An important development will be the seamless integration of the QD device virtualization module to enable target control of qubit QDs. Future work will also focus on extending first the bootstrapping and then the full algorithm to multiple QD arrays.

In the present work, the rf-reflectometry circuit (frequency, phase, position in the I-Q plane, demodulation parameters) has been set to known values optimized manually; in the future, the rf-reflectometry optimization could be automated using simple feedback based on measurements that are similar to those presented here. Additionally, recent developments in high-speed and high-sensitivity real-time “video mode” data acquisition could be complemented by this protocol, allowing for more rapid sensor-QD tuning for charge sensing of the QD arrays, eliminating the need for human intervention. A broad application of our modules to different materials systems (e.g., nanowires, germanium quantum wells) might help us to understand differences between materials, disorders, and future platform-specific improvements.

Finally, this work focuses on GaAs devices, where a single

layer of gates is sufficient to confine the QDs. This simplifies tuning compared to QDs defined by overlapping gate electrodes, which may add complexities due to cross-capacitance as well as a higher number of parameters that need to be adjusted. While preliminary testing of some of the bootstrapping algorithm components shows good performance when tested on an accumulation-mode Si sample, full cross-platform compatibility will require the development of specialized data-analysis tools.

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