Dual-Frequency-Bias Programmable Josephson Voltage Standard Circuit Design

A. Rüfenacht, A. E. Fox, P. D. Dresselhaus, and S. P. Benz

National Institute of Standards and Technology, Boulder, CO 80305
alain.rufenacht@nist.gov

2024 Conference on Precision Electromagnetic Measurements (CPEM) | USGov | DOI: 10.1109/CPEM61406.2024.10646095

***Abstract* — This paper presents a new 2 V programmable Josephson voltage standard circuit with dual microwave frequency input. This design provides three main features: (1) output voltages with nanovolt resolution, (2) the ability to perform a microwave frequency self-check based on a null voltage measurement, and (3) additional voltage output taps providing simultaneous 10:1 (or 5:1) divided voltage reference for resistive divider calibration.**

***Index Terms* — Josephson arrays, Measurement techniques, Precision measurements, Standards, Superconducting integrated circuits, Voltage measurement.**

I. Introduction

Following the 2019 redefinition of the International System of Units (SI), programmable Josephson voltage standards (PJVS) became the primary instrument to realize the volt. With full automation, cryogen-free operation, and robustness to external perturbation, PJVS systems perform a variety of dc electrical metrology calibrations [1,2]. In their typical configuration, our present NIST PJVS circuit designs had two limitations we desired to improve. The frequency reference to the microwave synthesizer (typically 10 MHz) and the microwave frequency must be SI traceable. (1) While the 10 MHz frequency reference can be verified with standard frequency metrology methods to better than 1 part in 10^{10} with a GPS-disciplined oscillator, the task of verifying the frequency at the output of the microwave synthesizer is not trivial and typically requires periodic intercomparison with another frequency reference or intercomparison of the PJVS output voltage with that of another PJVS system. (2) The programmable voltage resolution is restricted by the number of Josephson Junctions (JJs) in the least significant bit (LSB subarray) and the applied bias frequency. For example, with the present NIST 10 V PJVS circuit design (LSB=6 JJs @ 18.3 GHz), the voltage resolution is typically ~227 µV.

Our dual-frequency-bias 2 V PJVS circuit design presented here is intended for implementation on a compact cryocooler system for easy transport and setup. It is designed to overcome the two limitations mentioned above, with additional features supporting voltage divider measurements.

II. Circuit Design

The new circuit design consists of eight arrays of 8,160 JJs, each embedded in a coplanar waveguide (CPW), such that the series-connected arrays generate a maximum voltage of 2 V at a drive frequency f_1=f_2=14.816 110 552 GHz. The schematic in Fig. 1 shows the dual-frequency input and the JJs subarray ("Sba") distribution, as well as the current bias (DAC#) and voltage taps. The JJs in the last CPW are subdivided into ternary segments to provide the coarse voltage adjustment (LSB=24 JJs @ 14.8 GHz ≅ 735µV). The top and bottom halves of the JJ array have two independent microwave inputs (f_1 and f_2), each biasing four CPW arrays through two layers of on-chip Wilkinson dividers (Figure 2). The fine voltage tuning is accomplished by adjusting the difference frequency between the two microwave synthesizers. The voltage resolution is only limited by the frequency resolution of the two independent synthesizers. This dual-frequency bias design is especially advantageous because of the availability of low-cost commercial microwave synthesizers and amplifiers in the (14 – 18) GHz frequency range.

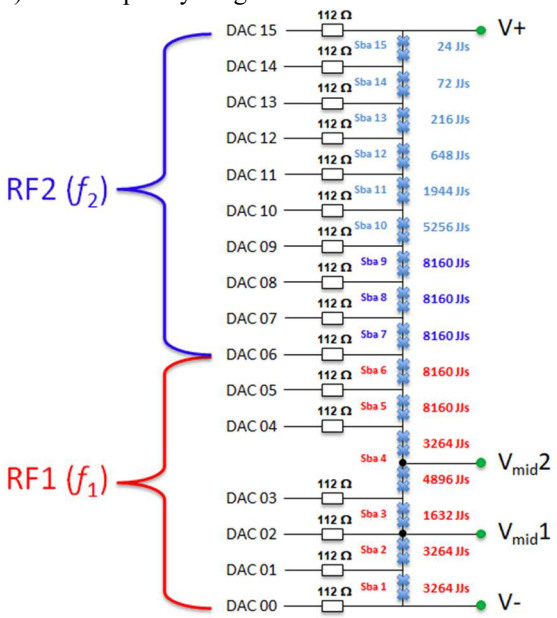

Fig. 1. Circuit layout of the dual-frequency-bias 2 V PJVS. The 16 current bias input taps (DAC0 to DAC15) are shown on the left side, and the four voltage output taps on the right side. The least significant bit subarrays at the top are labeled Sba 10 to Sba 15. There are multiple most significant bit (MSB) subarrays that each have 8,160 JJs.

III. Frequency Self-Verification

The dual-frequency-bias circuit is advantageous to performing regular in-situ frequency tests. Such tests can be achieved by biasing the two halves of the circuit at the same

979-8-3503-6104-9/24/$31.00 ©2024 IEEE

frequency such that each half produces the opposite voltage and a null output across the entire circuit (+1 V−1 V = 0 V) and measuring the output voltage at room temperature on a digital nanovoltmeter. The measurement is repeated with a reversed bias current to remove the thermal electromagnetic force (EMF) on the voltage output leads (also reversing the subarray voltage polarities to −1 V+1 V = 0 V). Subtracting the two voltage measurements eliminates the emf voltage, but not the contribution of a possible frequency error on the output voltage. Such measurements verify that the frequencies f_1 and f_2 are equal, with a limit based on the voltage and uncertainty measured. However, if both microwave synthesizers implemented are identical, a systematic frequency error due to the synthesizer's internal design cannot be excluded. Another frequency verification at $f_1 \neq f_2$ can be performed by biasing all the JJs on the bottom half (−1 V on RF1) and all JJs minus the 24 JJs subarray on the top half (RF2). The frequency on RF2 is slightly increased by δf=10.902 215 MHz ($f_2=f_1+\delta f$) to generate exactly +1 V.

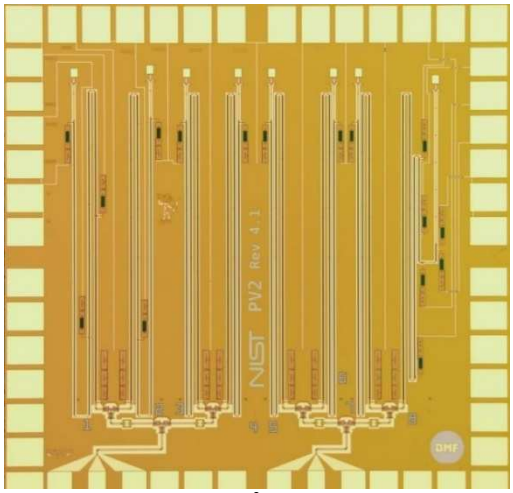

Fig. 2. Photograph of the 1 cm^2 circuit fabricated at NIST Boulder Microfabrication Facility. The two CPW microwave inputs are located on the bottom of the chip. The JJs are made of a triple stack of $Nb/Nb_{1-x}Si_x/Nb$, similar to the NIST 10 V PJVS circuit [1].

IV. Enhanced Voltage Resolution

The implementation of two bias frequency inputs to increase the voltage resolution has been previously demonstrated [3,4]. The circuit in Fig. 1 has the advantage of generating nanovolt resolution over the entire −2 V to +2 V range with a single circuit while keeping the bias microwave frequencies f_1 and f_2 always within 10 MHz of the base bias frequency f=14.816 GHz. The software algorithm selects the closest combination of LSB and MSB subarrays to generate the target voltage. Then, it calculates the difference frequency δf ($f_1=f+\delta f$ and $f_2=f-\delta f$) needed to reach the exact output voltage. If $|\delta f|>10$ MHz, the algorithm adds two unbiased MSB subarrays in opposition (i.e., +8160 JJs on RF1 and −8160 JJs on RF2), then recalculates δf. The MSB opposition "padding" JJs procedure is repeated until the criteria $|\delta f|<10$ MHz is reached.

V. Voltage Ratio Taps

The circuit has two additional voltage output taps to generate either a simultaneous 10:1 voltage ratio ($V_{mid}1$) [5] or a 5:1 voltage ratio ($V_{mid}2$) for the calibration of an external resistive voltage divider. The number of JJs biased in Sba1 to Sba3 is arranged so that $V_{mid}1$ can generate ±0.1 V or ±0.2 V (@ respectively ±1 V or ±2 V across the entire array). Similarly, for $V_{mid}2$, the output voltage can be programmed to be ±0.2 V or ±0.4 V (@ ±1 V or ±2 V across the entire array). If the ratio function is unused, then Sba (1-3) can be biased together to resemble an MSB with 8,160 JJs, reducing the number of subarrays used to characterize the circuit bias.

VI. Conclusion

This circuit design is intended to be implemented on a traveling cryocooled system to perform direct PJVS to PJVS comparisons at 2 V at the location of disseminated 10 V PJVS systems. The traveling PJVS system is being designed to complete all the measurements required for the direct comparison uncertainty analysis, including frequency self-check, quantum locking range (QLR) to test the quantization of the PJVS array, and automated leakage current measurements [1]. Since the 2 V PJVS cryopackage dissipates much less power than the 10 V PJVS cryopackage, it may be operated on a cryocooler with lower cooling power that is more transportable.

The 2 V chip has been fabricated and is under evaluation. The full implementation and QLR performance will be presented at the conference.

References

[1] A. Rüfenacht, N. E. Flowers-Jacobs, and S. P. Benz, "Impact of the latest generation of Josephson voltage standards in ac and dc electric metrology," *Metrologia*, vol. 55, no. 5, pp. S152–S173, Oct 2018.

[2] S. Bauer, R. Behr, J. Herick, O. Kieler, M. Kraus, H Tian, Y. Pimsut and L. Palafox, "Josephson voltage standards as for precision metrological applications at PTB," *Meas. Sci. Technol.* 34, 032001 (22pp), 2023.

[3] D. Georgakopoulos, I. Budovsky1, T. Hagen, H. Sasaki, and H. Yamamori, "Dual radiofrequency drive quantum voltage standard with nanovolt resolution based on a closed-loop refrigeration cycle," *Meas. Sci. Technol* 23, 124003 (6pp), Nov. 2012.

[4] H. Li, Z. Wang, W. Cao, J.Li, Q. He, Z. Li, "A Practical Microvolt Josephson Voltage Standard for Nanovoltmeter Measurement Based on Dual-Channel Josephson Junction Array," *CPEM 2020 conference digest*, DOI: 10.1109/CPEM49742.2020.9191899, 2020.

[5] A. Rufenacht, N. E. Flowers-Jacobs, A. E. Fox, P. D. Dresselhaus, and S. P. Benz, "Josephson Voltage Standard," U.S. Patent 11,557,708 B1, Jan 17, 2023