# Relationship between Trapping Centers, Charge Pumping, and Leakage Currents in Hot-Carrier-Stressed Si/SiO<sub>2</sub>/HfO<sub>2</sub> Transistors

S. J. Moxim Alternative Computing Group National Institute of Standards and Technology 100 Bureau Drive Gaithersburg, MD 20899 USA <u>stephen.moxim@nist.gov</u>

N. W. Lawson\*\*\* Alternative Computing Group National Institute of Standards and Technology 100 Bureau Drive Gaithersburg, MD 20899 USA <u>nlawson3@illinois.edu</u> J. P. Ashton\* Alternative Computing Group National Institute of Standards and Technology 100 Bureau Drive Gaithersburg, MD 20899 USA james.ashton@keysight.com

J. T. Ryan Alternative Computing Group National Institute of Standards and Technology 100 Bureau Drive Gaithersburg, MD 20899 USA jason.ryan@nist.gov M. A. Anders\*\* Alternative Computing Group National Institute of Standards and Technology 100 Bureau Drive Gaithersburg, MD 20899 USA mark.anders@broadcom.com

Current Affiliations: \*Keysight, Santa Rosa, CA USA. \*\*Broadcom, Breiningsville, PA USA \*\*\*U. of Illinois, Urbana, IL USA.

Abstract-We identify two distinct atomic-scale defect responses following hot carrier stressing of HfO2 based metaloxide-semiconductor field-effect transistors (MOSFETs). Revealed through various electron spin based magnetic resonance techniques, including spin dependent charge pumping (SDCP) and spin dependent tunneling (SDT), we describe in detail the physical and chemical nature of the two defect responses. Depending on the specific MOSFET biasing configuration and the response magnitude of each defect type. we detect magnetic resonance spectra originating from recombination at defect centers located precisely at the silicon/oxide interface, trap assisted tunneling current through defects located in the oxide bulk, or some combination of both. The results are correlated to and quantified by purely electrical based (non-resonant) measurements of MOSFET charge pumping (CP) and gate leakage behavior. Finally, the nonresonant electrical measurements include deconvolution of the two competing (CP and leakage) mechanisms via frequency modulated CP techniques.

Keywords—charge pumping, leakage current, defects, electrically detected magnetic resonance, hot carrier stress

### I. INTRODUCTION

Metal-oxide-semiconductor field-effect-transistors (MOSFETs) based on Si/SiO<sub>2</sub>/HfO<sub>2</sub> materials have dominated state-of-the-art integrated circuits for well over a decade [1]. Despite being mainstream, many unanswered questions remain regarding the identity of, and role that atomic-scale trapping centers play in various reliability mechanisms, including hot carrier degradation [2]. Purely electrical-based measurements of charge pumping (CP) current [3] and gate leakage current [2] have proven useful for shedding light on the evolution of reliability issues by providing qualitative and/or quantitative information about the specific atomic scale trapping centers responsible for the degradation. These electrical based metrology techniques are also noteworthy since they both can be extended to include analytical electron spin resonance (ESR) responses via electrically detected magnetic resonance (EDMR). When configured as such, spindependent charge pumping (SDCP) [4] and spin-dependent tunneling (SDT) [5] provide all the normal information available with the purely electrical versions, with the added analytical ability to provide detailed chemical and physical identification of the specific atomic scale defect centers responsible for observed reliability degradation, even at the scale of a single transistor. This vastly increases the power and usefulness by providing a direct and often quantitative link between device parametric degradation and specific atomicscale defect entities.

Briefly, both EDMR techniques rely on the Pauli exclusion principle to enhance or impede some current producing mechanism that involves the interaction of two spin species. For the case of SDCP, the EDMR response is read out via the CP current itself; here, the MOSFET is biased to produce a CP current in the normal fashion [3] which involves electron-hole recombination through interface defects at the semiconductor/oxide juncture. The device is then placed within a microwave resonance cavity, tuned to a constant frequency, that resides between the poles of an electromagnet. The magnetic field is swept while the CP current is monitored. When the ESR resonance condition for the interface traps is satisfied, a change in CP current is observed due to previously forbidden spin transitions becoming allowed.

The experimental setup is nearly identical for SDT. In this configuration, the EDMR response is read out via a gate leakage current that involves some intermediary spin species (so called trap assisted tunneling current) located within the gate oxide bulk region. Here, the MOSFET (or simpler capacitor structures) is biased to produce a gate leakage current which is monitored as a function of magnetic field. When the ESR resonance condition is satisfied, a change in leakage current is observed again due to previously forbidden spin transitions becoming allowed. A much more thorough and detailed description of SDCP and SDT processes is described elsewhere [4-5].

Both SDCP and SDT results are interpreted in terms of the underlying ESR response. Information about the physical defect wavefunction is gained from the effects of spin-orbit coupling at the defect site. This is related to the specific combination of magnetic field strength (Zeeman energy splitting) and microwave frequency (photon energy) that resonance occurs at. This is expressed as the "g-value" for a particular experiment and contains all the detailed chemical and physical spectroscopic information. In addition, the results can also reveal spin-spin interactions between the defect electron(s) and nearby magnetic species, typically magnetic nuclei, or other unpaired electrons. These can manifest themselves as a splitting of the resonance if the magnetic species are closely tied to the structure of the defect center, or as a broadening of the resonance spectrum if they are not. Again, more detailed explanations are available elsewhere [4-5].

In this paper, we present SDCP and SDT results from a single hot carrier stressed p-type Si/SiO<sub>2</sub> (2 nm)/HfO<sub>2</sub> (3 nm) planar MOSFET and, building upon previous work [6], we directly link the analytical magnetic resonance defect responses to purely electrical data. Thus, providing a convenient and powerful link between specific defect entities and device parametric degradation. The gate width of the transistors was 100  $\mu$ m and the channel length was 1  $\mu$ m. The large area devices were selected to ensure reasonable detection times for SDCP and SDT measurements. Strong pitch was used as a standard reference material to calibrate the magnetic field for accurate g component measurements. The uncertainty in g is  $\pm 0.0003$  and the typical detection limit for the EDMR current change was 4 pA. All measurements and device stressing were conducted at room temperature.

#### II. RESULTS AND DISCUSSION

Fig. 1 illustrates the results of purely electrical (no resonance) CP measurements before (blue) and after (red) hot carrier stressing the device at  $V_g = 1.3$  V and  $V_d = 3.5$  V for 2000 s. The constant amplitude ( $\Delta V_{CP} = 0.5$  V) swept base voltage ( $V_{mid,CP}$ ) CP measurements, performed at a CP frequency of  $f_{CP} = 500$  kHz, display a characteristic peak which is directly proportional to the number of interface defects participating in the mechanism [3]. The peak increases in amplitude following stress clearly indicating the creation of interface defects due to the stress conditions.

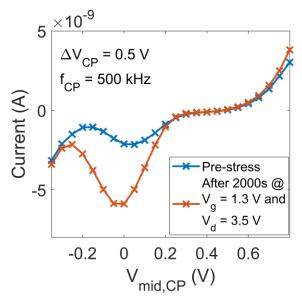


Fig. 1: Purely electrical (non-resonant) constant amplitude swept base voltage CP measurements before (blue) and after (red) hot-carrier stressing. The characteristic "peaks" in these curves are due to recombination at interface defects. The peak amplitude clearly increases following stress which is indicative of stress induced interface defect generation. Also note that because the CP current is measured through the MOSFET substrate contact, it also includes contributions from gate leakage currents. These gate leakage contributions also increase post stress, most noticeably at the far left and far right of the curves.

A shift in threshold voltage of approximately 70 mV, measured via standard drain current versus gate voltage measurements (not shown) was also induced by the stress conditions. Since the CP current is measured through the device substrate contact, while the source (S) and drain (D) are grounded and a voltage pulse train is applied to the gate, the current measurement by default also includes any gate leakage current components [7]. This is especially noticeable when the device is biased outside voltage regions which do not support CP recombination. In other words, the voltage ranges which do not allow for sufficient populations of *both* electrons and holes that are required for recombination. In these regions (the far-left negative gate voltages and far-right positive gate voltages of fig. 1) there is a small but noticeable increase in leakage current following stress.

Fig. 2a illustrates the post stress EDMR results at three different gate voltage pulse values ( $V_{high,CP}$  and  $V_{low,CP}$ ) which correspond to three distinct regions of biasing, as highlighted within the figure. Note that no EDMR responses could be resolved with reasonable signal averaging in pre-stress devices, owing to their apparent as processed low defect density. Additionally, Fig. 3 shows a purely DC SDT response; that is, a measurement utilizing a constant gate voltage rather than the square waves utilized in fig. 2. Here, a much larger gate area (gate length and width are 100  $\mu$ m) device was used to enhance the signal to noise ratio.

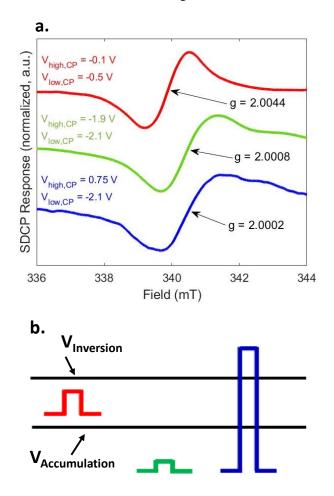


Fig. 2: (a) Post-stress EDMR results reveal different defect responses depending on the specifc gate voltage waveform utilized. As illustrated in fig. 2b. the voltages used either fully support SDCP (red), fully support SDT (green), or support some intermediary simultaneious combination of SDCP and SDT (blue).

As noted, the three measurements of fig. 2a were taken at three distinct regions of gate voltage biasing. The voltages used in the top trace (red,  $V_{high,CP} = -0.1$  V and  $V_{low,CP} = -0.5$ V) fully supports CP based recombination (by having participation from both electrons and holes) through interface states while also minimizing any additional gate leakage current (by keep the voltages relatively low, gate leakage is Thus, this g = 2.0044 response is almost minimized). completely due to SDCP at defects located at the Si/SiO2 interface. Also known as the Pb center family of defects, these "dangling bond" defects consist of a central silicon atom back bonded to three other silicon atoms and are dominating defects in most Si/SiO<sub>2</sub> systems, as discussed in detail elsewhere [8-11]. Its worth noting that the spectra observed here is significantly broadened compared to the spectra observed for pure Si/SiO<sub>2</sub> systems. This is likely due to large spin-orbit coupling effects between the dangling bond electron and nearby hafnium atoms, as previously observed [12-13].

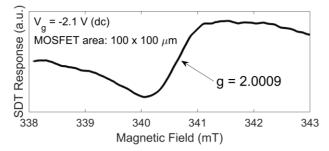


Fig. 3: Pure SDT spectrum obtained by making the measurement with a DC gate bias (source and drain floating) rather than a square wave. While made on a much larger area device to enhance the signal to noise ratio, the spectrum is consistent with E' centers located within the SiO<sub>2</sub> interfacial layer. The significant broadening indicates large spin orbit coupling with nearby hafnium atoms.

On the other hand, the middle trace (green,  $V_{high,CP} = -1.9$ V and  $V_{low,CP} = -2.1$  V) does not support any CP recombination (the waveform is always entirely in accumulation thus only one type of charge carrier is ever present) and the observed response is likely entirely due to an SDT effect. Consistent with the measured g-values, this almost pure SDT response is likely due to oxygen vacancy defects in the 2 nm SiO<sub>2</sub> layer (known as the E' center family of defects) serving as intermediary hopping sites in a trap assisted tunneling process through the gate state. Note that this spectrum is significantly broadened, likely due to spin-orbit interactions with nearby hafnium atoms in the interfacial layer [13-14]. This is additionally validated in Fig 3 which illustrates a pure DC SDT measurement, in which the applied gate voltage ( $V_G = -2.1 \text{ V}$ , S/D floating) is constant throughout the measurement, as opposed to the square wave voltage pulse trains used elsewhere.

Lastly, the bottom trace (blue,  $V_{high,CP} = 0.75$  V and  $V_{low,CP} = -2.1$  V) supports a convoluted combination of CP recombination as well as a fairly large contribution from gate leakage. Thus, one would expect a combined SDCP and SDT response, in effect, a combination of the previous two responses (red and green spectra from fig. 2). However, the response observed is clearly not consistent with this assessment. Here, only the spectrum consistent with that of the SDT response is observed (the green curve of fig. 2a and fig. 3).

While seemingly inconsistent, the reason becomes apparent when purely electrical (non-resonant) CP curves are taken with increasing  $\Delta V_{CP}$ , as shown in fig. 4. Here, at

smaller values of  $\Delta V_{CP}$ , similar to fig. 1, the characteristic peak associated with CP through interface defects is clearly observed (the red vertical line is provided as a guide to the eye). At larger  $V_{mid}$  voltages (either positive or negative) the current rapidly increases due to gate leakage. However, when the  $\Delta V_{CP}$  is increased, the additional gate leakage current quickly increases and overwhelms the CP response, occurring as early as  $\Delta V_{CP} = 0.8$  V. Thus, the reason the EDMR spectra that *should* support both SDCP and SDT only produces the SDT response (blue spectrum of fig. 2a), is simply that the leakage current is much larger and simply overwhelms the SDCP response. In other words, both responses are present, but is simply dominated by the larger SDT response.

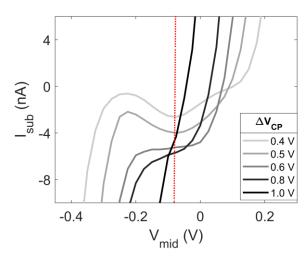


Fig. 4: Non resonant charge pumping and leakage characteristics as a function of  $\Delta V_{CP}$ . At small voltages, the characteristic peak due to interrface trap recombination is clearly present. Increased voltage results in increased leakage current which rapidly overhwhelms and obscures the CP peak response. The red, dotted line draws the eye to the disappearing peak in CP current.

To confirm this ascertain and attempt to deconvolute the contributions from both competing mechanisms, frequency modulated CP (FMCP) was implemented [7, 15]. Schematically described in fig. 5, FMCP takes advantage of the fact that CP current is frequency-dependent, while leakage current is not, when a constant waveform shape factor is used. In this configuration, the CP gate waveform is modulated (alternated) between two different frequencies, Fhigh and Flow (modulation depth) at some rate, known as the modulation frequency, using an arbitrary waveform generator (AWG). The subsequent two-level CP signal is fed into a current preamplifier and subsequent lock in amplifier (LIA) phase locked to the modulation frequency. Thus, the lock-in output is proportional to the *difference* between the two CP signal levels,  $\Delta I_{FMCP} = I_{CP}(F_{high}) - I_{CP}(F_{low})$  corresponding to CP at a frequency equal to the modulation depth, I<sub>CP</sub> (F<sub>high</sub>-Flow).Further details and discussion about the FMCP measurement can be found elsewhere [7, 15].

The FMCP results are shown in fig. 6. and were obtained by utilizing a modulated gate waveform with  $\Delta V_{CP} = 1.0$  V, the most extreme (highest leakage) voltages used in fig. 4 and do not display any CP response. With FMCP detection however, for the same case of extreme leakage components, we can clearly resolve the characteristic peak associated with CP through interface states, despite the very large leakage component background. Thus, this data serves as confirmation that for the convoluted EDMR measurements, there is still a small SDCP contribution that is simply overwhelmed by the large leakage response.

While not shown, implementing an FMCP concept into the measurements of fig. 2 would be a very worthwhile future pursuit in order deconvolute SDCP versus SDT and allow for identification of interface defects in biasing schemes overwhelmed by gate leakage.

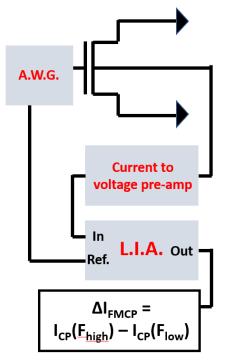


Fig. 5. FMCP block diagram in which the frequency modulated gate voltage waveform is provide by an arbitrary waveform generator and the subsequent substrate current is measured via lock-in detection. This provides a leakage free measure of CP.

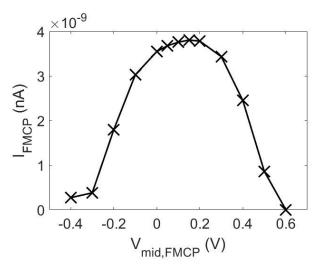


Fig. 6: Even at the most extreme leakage conditions of fig. 4,  $\Delta V_{CP} = 1$  V, FMCP clearly shows the characteristic CP peak.

## III. CONCLUSIONS

We utilize SDT and SDCP to identify two distinct hotcarrier-induced defect responses in HfO<sub>2</sub> based MOSFETs. Consistent with interface defect recombination and/or trap assisted tunneling through oxide defects, the observed spin dependent responses depend on the biasing specifics, sometimes producing a convoluted combination of both. We provide detailed magnetic resonance identification of both defect entities and support our analysis by connecting the magnetic resonance results to traditional leakage current, charge pumping, and frequency-modulated charge pumping measurements. We also propose a more efficient deconvolution method, in the form of frequency-modulated, spin-dependent charge pumping, which should be explored in the future.

#### **IV. REFERENCES**

- J. Robertson and R.M. Wallace, "High-k Materials and Metal Gates for CMOS Applications", *Materials Science and Engineering: R: Reports*, Vol. 88, pp. 1-41, 2015.
- [2] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasaranthy, E. Vincent, and G. Chibaudo, "Review on High-k Dielectrics Reliability Issues", *IEEE Transactions on Device and Materials Reliability*, Vol. 5 (1), pp. 5-19, 2005.
  [3] J.S. Brugler and P.G.A. Jespers, "Charge Pumping in MOS Devices",
- [3] J.S. Brugler and P.G.A. Jespers, "Charge Pumping in MOS Devices", *IEEE Transactions on Electron Devices*, Vol. 16 (3), pp. 297-302, 1969.
- [4] M.A. Anders, P.M. Lenahan, and A.J. Lelis, "Multi-Resonance Frequency Spin Dependent Charge Pumping and Spin Dependent Recombination Applied to the 4H SiC/SiO<sub>2</sub> Interface", *Journal of Applied Physics*, Vol. 122 (23), 234503, 2017.
- [5] M.A. Anders, P.M. Lenahan, C.J. Cochrane, and J. van Tol, "Physical Nature of Electrically Detected Magnetic Resonance through Spin Dependent Trap Assisted Tunneling in Insulators", *Journal of Applied Physics*, Vol. 124 (21), 215105, 2018.
- [6] S.J. Moxim, J.P. Ashton, M.A. Anders, and J.T. Ryan, "Combining Electrically Detected Magnetic Resonance Techniques to Study Atomic-Scale Defects Generated by Hot Carrier Stressing in HfO<sub>2</sub>/SiO<sub>2</sub>/Si Transistors", *Journal of Applied Physics*, Vol. 133 (14), 145702, 2023.
- [7] J.T. Ryan, J. Zou, R.G. Southwick, J.P. Campbell, K.P. Cheung, A.S. Oates, and R. Huang, "Frequency Modulated Charge Pumping with Extremely High Gate Leakage", *IEEE Transactions on Electron Devices*, Vol. 62 (3), pp. 769-775, 2015.
- [8] Y.Y. Kim and P.M. Lenahan, "Electron Spin Resonance Study of Radiation Induced Paramagnetic Defects in Oxides Grown on (100) Silicon Substrates", *Journal of Applied Physics*, Vol. 64 (7), pp. 3551-3557, 1988.
- [9] E.H. Poindexter, P.J. Caplan, B.E. Deal, and R.R. Razouk, "Interface States and Electron Spin Resonance Centers in Thermally Oxidized (111) and (100) Silicon Wafers", *Journal of Applied Physics*, Vol. 52 (2), pp. 879-884, 1981.
- [10] S.J. Moxim, F.V. Sharov, D.R. Hughart, G.S. Haase, C.G. McKay, and P.M. Lenahan, "Atomic Scale Defects Generated in the Early/Intermediate Stages of Dielectric Breakdown in Si/SiO<sub>2</sub> Transistors", *Applied Physics Letters*, Vol. 120 (6), 063502, 2022.
- [11] P.M. Lenahan and J.F. Conley, "What Can Electron Paramagnetic Resonance Tell Us About the Si/SiO<sub>2</sub> System?", *Journal of Vacuum Science and Technology*, B, Vol. 16, pp. 2134-2153, 1998.
- [12] T.G. Pribicko, J.P. Campbell, P.M. Lenahan, W. Tsai, and A. Kerber, "Interface Defects in Si/HfO<sub>2</sub> based Metal Oxide Semiconductor Field Effect Transistors", Applied Physics Letters, Vol. 86 (17), 173511, 2005.
- [13] P.M. Lenahan and J.F. Conley, "Magnetic Resonance Studies of Trapping Centers in High-K Dielectric Films on Silicon", *IEEE Transactions on Device and Material Reliability*, Vol. 5 (1), pp. 90-102, 2005.
- [14] J.T. Ryan and P.M. Lenahan, "Direct Observation of Electrically Active Interfacial Layer Defects Which May Cause Threshold Voltage Instabilities in HfO<sub>2</sub> Based MOSFETs', *IEEE International Integrated Reliability Workshop Final Report*, pp. 107-110, 2007.
- [15] J.T. Ryan, R.G. Southwick, J.P. Campbell, K.P. Cheung, A.S. Oates, and J.S. Suehle, "Frequency Modulated Charge Pumping: Defect Measurements with High Gate Leakage", *IEEE Electron Device Letters*, DOI: 10.1109/LED.2013.2251315, 2013.