Josephson Sampler Response using a Binary Search Algorithm

Bart J. Van Zeghbroeck, Logan A. Howe, and Peter F. Hopkins

***Abstract*—This paper presents the use of a binary search algorithm to obtain the simulated response of a superconducting Josephson junction-based sampler. In the absence of noise, this simple approach is superior to mimicking the experimental approach of using an analog feedback circuit. This binary search method is first used to obtain the response of an idealized sampler, analyzing the sampler risetime to a step input and its dependence on damping. Next, it is applied to a full sampler circuit. Finally, we present the first experimental implementation of this method. A 10%-to-90% step-input response of 5.1 ps was obtained using 8 binary search iterations which yielded a current sensitivity of 1 μA.**

***Index Terms*—Algorithm, Binary, Josephson, Resolution, Response, Sampler, Simulation, Superconductor.**

I. INTRODUCTION

There is a renewed interest in Josephson samplers for the characterization and calibration of high-speed systems at cryogenic temperatures such as high-density superconducting computer chips [1], quantum computers [2] and scanning magnetometers [3]. Most initial work [4-10] dates back to the 70's and 80's when there was a need to characterize latching superconducting logic and memory circuits [11,12]. Noteworthy progress included the demonstration of a two-junction pulse generator [5], an on-chip adjustable delay circuit [7], a sampler with a step-input response 10%-90% risetime of 2.1 ps [8] and the development of a commercial ultra-fast sampling oscilloscope and a time domain reflectometer [9]. A second generation of sampler designs are based on non-hysteretic junctions, compatible with Single Flux Quantum logic and memory circuits [13]; low temperature [14] and high temperature [15,16] superconductor versions of these sampler designs have been implemented.

Operation of such samplers requires the repeated operation of the device under test (DUT), sampling its signal at different times and adjusting the bias to extract the sampler response. This involves an analog feedback circuit, as for instance detailed in [17].

Simulation of the sampler response presents its own challenge. Conceptually one can simulate the sampler circuit, including the analog feedback circuit, with sub-picosecond resolution. However, a single sampler response trace can take 20 ms [8] so that such a long simulation would have been prohibitive at the time, and today would still be a time-consuming task. In addition, any sampler optimization would require several of those simulations when exploring the effect of circuit parameters and/or bias currents.

This limitation is documented by the sparse number of simulated data points published, providing only an approximate fit to the measured data [6,9]. Instead, an analytical model was proposed [18] for comparison with experimental data [8].

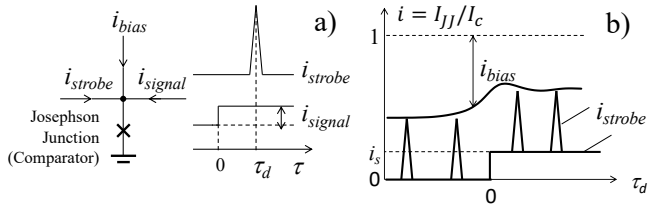

Fig. 1. Sampler operation principle indicating the: a) applied currents and b) sampler response obtained for different delays, τ_d, between strobe and signal.

With the current availability of computing power as well as digital experiment control and data acquisition, the question arises how such simulations can be accelerated and whether the same method can be used to extract the measured sampler response.

In this paper, we present a binary search algorithm as a novel approach to extract the sampler response using a latching junction as a comparator. First, we implement the algorithm to identify the limiting resolution of an idealized Josephson sampler to a step-input signal. Next, we implement the algorithm to simulate the response of an actual sampler circuit and present the measured response of a fabricated sampler circuit.

II. IDEALIZED SAMPLER SIMULATIONS

A. Principle of Operation

The principle of operation of samplers that use hysteretic Josephson junctions - as only considered in this paper - is based on using the junction as a threshold detector, also referred to as the comparator. Fig. 1a illustrates the operation principle, where a short sampling strobe pulse, I_{strobe}, as well

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as the signal of interest, I_{signal}, are applied to the junction together with a dc bias, I_{bias}. The delay (τ_d) between the pulse and signal is then varied and for each delay the dc bias current is adjusted until the junction reaches its critical current as shown in Fig. 1b.

As can be taken from Fig. 1b, the required bias current then varies with the signal, be it with reversed sign and a dc offset. This does not fully reconstruct the actual signal because of the dynamics of the comparator junction. Instead, the response has, as shown in the Fig. 1b., a finite risetime in response to an abrupt step-input signal. There is also some ringing due to the plasma oscillation of the comparator junction.

B. Binary Search Algorithm and Simulation

Binary search algorithms have the benefit of significantly reducing the number of iterations required in root-finding or, in our case, threshold detection. In scenarios with negligible noise, using a current range $\Delta I = I_{\max} - I_{\min}$ and requiring current a resolution $\Delta I/N$, a linear search requires on average $N/2$ sampling iterations. For a binary search, the same resolution may be obtained in $\log_2(N)$ iterations. In the context of a typical Josephson sampler where the signals of interest are within a current range of 256 μA and for a desired resolution of 1 μA, the binary search results in a speedup of 16x (8 vs 128 iterations). If noise is nonnegligible then multiple sampling events must be gathered for each search iteration and decisions are then made using a probability threshold as well. This is true of both binary and linear searches. Also, when performing a binary search in the presence of excessive noise, the applied current bias does not change monotonically for subsequent iterations, indicating the need for additional averaging.

The binary search algorithm used here is described in more detail with the aid of Fig. 2. The process starts with the selection of a minimum and maximum bias current that will be applied to the junction. These are to be chosen such that the signal of interest is smaller than the difference between those two currents and with an appropriate offset to avoid clipping of the response. Furthermore, these max (min) biases must be selected such that the comparator always (never) latches for all delays – i.e., for all delays, τ_d, which offset the strobe pulse to any portion of the signal.

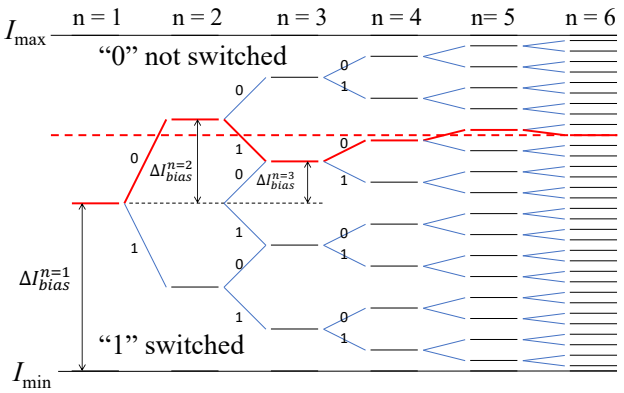

Fig. 2. Illustration of the binary search algorithm. See text for detail.

First, two initial simulations are run with $I_{bias} = I_{max}$ and $I_{bias} = I_{min}$ to guarantee the maximum and minimum biases are appropriately chosen. We then define:

$$I_{high}^{n=0} = I_{max} \tag{1}$$

$$I_{low}^{n=0} = I_{min}, \tag{2}$$

$$\Delta I_{bias}^{n+1} = \frac{I_{high}^{n} - I_{low}^{n}}{2}, \tag{3}$$

set the bias for the first binary search step to

$$I_{bias}^{n=1} = I_{low}^{n=0} + \Delta I_{bias}^{n=1} = I_{min} + \frac{I_{max} - I_{min}}{2}, \tag{4}$$

and determine whether the junction latches under this dc bias (a "1") or not (a "0"). If the result of simulation n was a 1, we select the lower bias range by setting:

$$I_{high}^{n+1} = I_{bias}^{n} \tag{5}$$

$$I_{low}^{n+1} = I_{low}^{n}, \tag{6}$$

and conversely for simulation n yielding the "0" result, we select the upper range:

$$I_{high}^{n+1} = I_{high}^{n} \tag{7}$$

$$I_{low}^{n+1} = I_{bias}^{n}, \tag{8}$$

Thus, the bias at simulation step $n \geq 1$ is:

$$I_{bias}^{n+1} = I_{low}^{n+1} + \Delta I_{bias}^{n+1} = I_{low}^{n} + \frac{I_{high}^{n} - I_{low}^{n}}{2} \tag{9}$$

This process is then continued up to the desired number of iterations, n, with a resulting bias current that represents the sampler response at the chosen delay, τ_d. The search algorithm is repeated for each of the strobe-to-signal delays, thereby constructing the sampler response.

C. Idealized Sampler Response

We further illustrate this method by simulating the response of an idealized sampler. It consists of a single junction with an abrupt step-input signal and a very short, 0.1 τ_0, and 0.2 I_c high strobe pulse, where:

$$\tau_0 = \frac{1}{\omega_0} = \sqrt{\frac{\hbar}{2e\, I_c} C} \tag{10}$$

and ω_0 is the plasma frequency of the junction.

This sampler response was obtained by numerically solving the normalized RCSJ model equations [19,20] which only depend on the McCumber parameter β_c [20], namely:

$$\beta_c = \frac{2e}{\hbar} I_c R^2 C, \tag{11}$$

where R is the shunt resistance and C is the capacitance of the comparator junction. The sampler response risetimes listed below are provided in units of τ_0. The step-input response of a comparator junction with β_c = 1.5 and 6 is shown in Fig. 3, for

a pulse delay varied from -15 τ_0 to 25 τ_0. Twelve binary search iterations were used to obtain the bias current, which was inverted and offset such that the sampler response is zero if there is no signal.

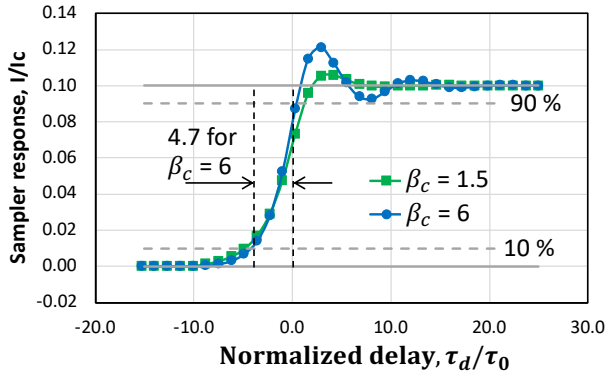

Fig. 3. Idealized sampler response for a comparator junction with β_c = 6 and 1.5.

As expected, the higher the damping, the longer the risetime and the smaller the overshoot of the response. Also, a further reduction of the damping, i.e., $\beta_c > 6$, results in a slightly faster risetime but would cause a distortion of the response which in the extreme case for $\beta_c > 22$ is known to result in an unwanted pre-pulse in the sampler response [10,18]. The dependence of the risetime and overshoot as a function of the McCumber parameter, β_c, is shown in Fig. 4.

For β_c ranging from 1.5 to 6, the overshoot increases from 5.8 % to 21% as the risetime decreases from 6.1 τ_0 to 4.7 τ_0. For $\beta_c > 6$, the sampler response dips below 90% after the initial overshoot causing a jump in risetime based on the last crossing of the 90% value. Because of this, values larger than 6 are not considered. For $\beta_c < 1.5$, the junction return current is larger than 0.87 I_c [21] which exceeds a typical bias current even when no signal is applied. As a result, the comparator junction no longer latches when exceeding its threshold. The desired window of operation is therefore $1.5 < \beta_c < 6$.

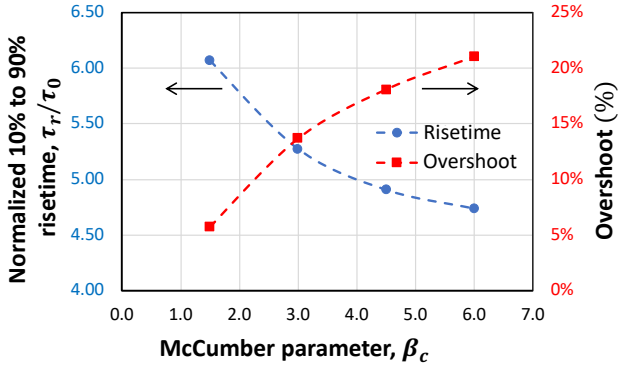

Fig. 4. Normalized sampler risetime and overshoot versus the McCumber parameter, β_c.

This result provides two key design considerations: 1) the McCumber parameter, β_c, as calculated by considering the total equivalent resistance shunting the comparator junction should be 6 or less and 2) the fastest expected 10% - 90% risetime in response to a step-input signal is 4.7 τ_0. Since τ_0 only depends on the ratio of the capacitance, C, to the critical current, I_c, one finds the limiting risetime of a sampler implemented with a 0.2 mA/μm² junction technology with 80 fF/μm² capacitance per unit area to be 1.7 ps.

III. Sampler Circuit Simulations

A. Sampler Circuit Description

The sampler circuit as fabricated is shown in Fig.5.

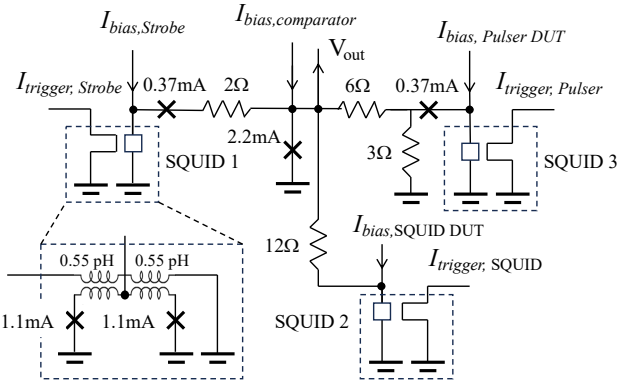

Fig. 5. Sampler circuit consisting of a comparator junction, a pulser as a strobe, the SQUID DUT providing a step-input signal and a second pulser with a reduced amplitude as an alternate DUT. The inset shows the detail of SQUIDs 1 through 3 in the circuit.

It consists of a 2.2 mA comparator junction connected with a 2 Ω resistor to the strobe circuit which consists of SQUID 1 and a small 0.37 mA junction. This strobe circuit provides the sampling pulse. Two devices under test (DUT) are connected to the comparator: 1) SQUID 2 which provides a step-input signal and 2) a circuit identical to the strobe circuit whose output is attenuated with a current divider. The inset shows the circuit detail of each of the identical SQUIDs. The capacitance-to-current ratio of all the junctions is 0.4 pF/mA.

B. Sampler Circuit Simulation

The sampler was simulated using LTSpice [22]. The model used for the Josephson junction is presented in the Appendix. Fig. 6. shows key current and voltage transients of a single sampling event. The SQUID DUT trigger precedes the sampling trigger by 10 ps and the comparator bias current is set just below the value needed for switching (Fig. 6a) and just above (Fig. 6b)

Shown on each graph are from top to bottom, the SQUID DUT current through the 12 Ω resistor, the Strobe pulse current through the 2 Ω resistor, the voltage across the comparator junction, V_{out}, and the supercurrent through the comparator junction.

For a SQUID DUT bias current of 2.0 mA, the signal current amplitude is 0.24 mA with a risetime of 1.7 ps. A first estimate of the sampler response is given by the supercurrent of the comparator junction [18], which has the same amplitude with a similar risetime of 1.6 ps mA.

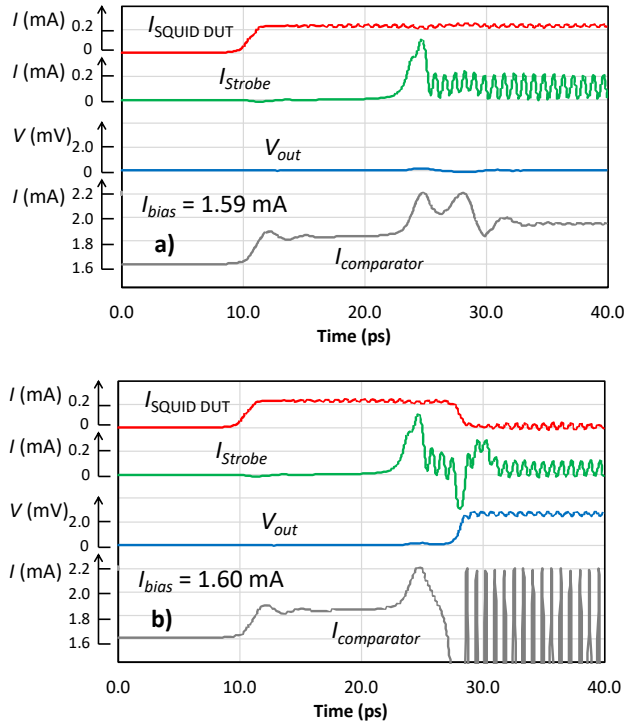

Fig. 6. The simulated SQUID DUT current, the strobe current as applied to the comparator, the voltage across the comparator junction, and the Josephson current through the comparator. These were simulated with a comparator bias of a) 1.59 and b) 1.60 mA.

For a bias current of 1.59 mA (Fig. 6a), the junction does not switch and the comparator current returns to a constant value after some oscillations. For a bias current of 1.60 mA (Fig. 6b), the comparator junction switches, causing a rise of V_{out} and an oscillating supercurrent through the junction.

C. Sampler Response Simulation

The sampler response was then obtained using the method described in II.B, using 60 equidistant delay values spaced by 0.25 ps and 12 binary search iterations, requiring therefore 720 sampler operations per trace. The resulting response is shown in Fig. 7.

The simulated 10%-90% risetime of the sampler circuit shown in Fig. 5 is 2.5 ps, while the overshoot and ringing are similar to that of the idealized sampler in Fig. 3 with $\beta_c = 6$. The difference with the 1.7 ps calculated risetime of the idealized sampler described in section II.C is attributed to the finite width of the strobe pulse and the non-abrupt (1.7 ps) risetime of the step-input signal of the SQUID DUT.

IV. Experimental Implementation

A. Circuit fabrication

The sampler circuit in Fig. 5 was fabricated using Nb/a-Si/Nb tri-layer junctions with an amorphous silicon barrier and a current density of 0.2 mA/μm² [23, 24]. The junctions have a capacitance-to-critical current ratio of 0.4 pF/mA. A micrograph of the circuit is shown in Fig. 8.

All three trigger lines connect to bond pads at the chip edge with a grounded coplanar waveguide geometry. As these lines reach the region shown in Fig. 8, they are transitioned to a microstrip (not shown) for coupling to the SQUID loops. The chip is wire bonded to a printed circuit board. The trigger lines are connected to a set of SMA connectors and semi-rigid coax lines, while the bias lines are all combined in a multi-wire cable.

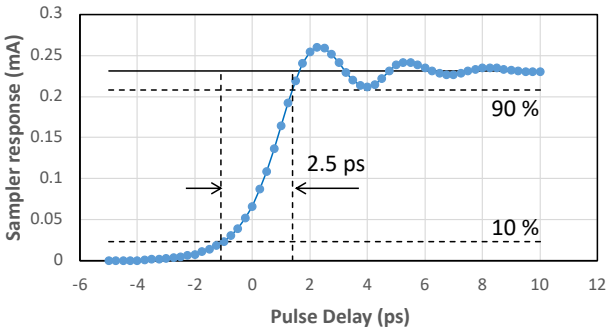

Fig. 7. Simulated sampler response of the step-input signal generated by the SQUID DUT shown in Fig. 5.

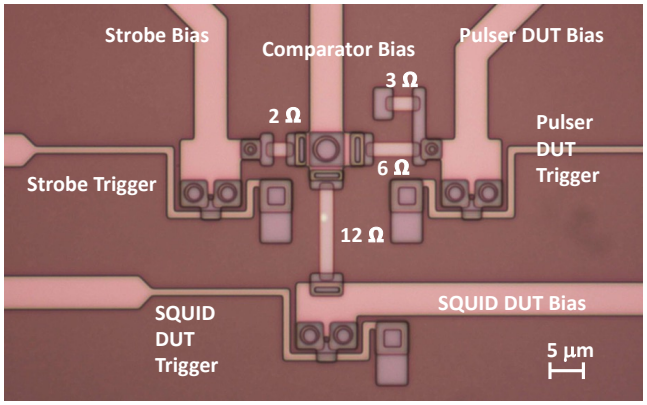

Fig. 8. Micrograph of the fabricated sampler circuit including two devices under test (DUT), namely a latching SQUID DUT creating a step-input and a Pulser DUT creating a pulse.

B. Sampler Characterization

The critical current, I_c, of each of the SQUIDs junctions was measured to be 1.1 mA and that of the comparator junction was measured to be 2.2 mA. The minimum critical current of the SQUID when changing the flux in the loop, is 1.25 mA. Using the empirical equation

$$\frac{I_{min}}{2I_c} = \frac{\frac{\beta}{2}+\beta^2}{2+\pi\beta+\beta^2} \text{ with } \beta = \beta_L\pi = 2\pi\frac{LI_c}{\Phi_0}, \quad (12)$$

obtained by combining the equations from [25], this yields a measured loop inductance, L, of 1.1 pH. The resistor values are expected to be within 10% of the nominal values listed.

C. Sampler Testing

The sampler was operated at 3.6 K, with all applied signals generated by a set of computer-controlled AWGs. The delay between the strobe and DUT was obtained with a setup similar to [8], including a manual delay line for calibration. Due to the

fact that all junctions are underdamped (latching), the bias must be reset at the end of each sampling period and the reset-to-reset period of the sampler was 66.7 ms or a repetition frequency of 15 kHz. The sampler output for a given bias, I_{bias}, and delay was averaged over 1000 sampler operations to reduce the influence of noise and crosstalk. This output provided the switching information for a binary search of the required bias at threshold with 8 iterations. This process was then repeated for 240 equidistant delay values spaced by 0.135 ps. The resulting sampler response for the SQUID DUT and pulser DUT are presented in Fig. 9.

The measured sampler response of the SQUID DUT resulted in a risetime of 5.13 ps. In addition, the pulser was measured to have a FWHM of 5.10 ps. A close look at the pulser response, as shown in the inset, reveals the sampler resolution of 1 μA as obtained with 8 iterations. The response to the step-input does not have the same overshoot as the simulated response of Fig. 7 and also has a slower risetime. Both are indicative of higher damping, possibly due to a lower-than-expected sub-gap resistance or parasitic elements that are not included in the simulations.

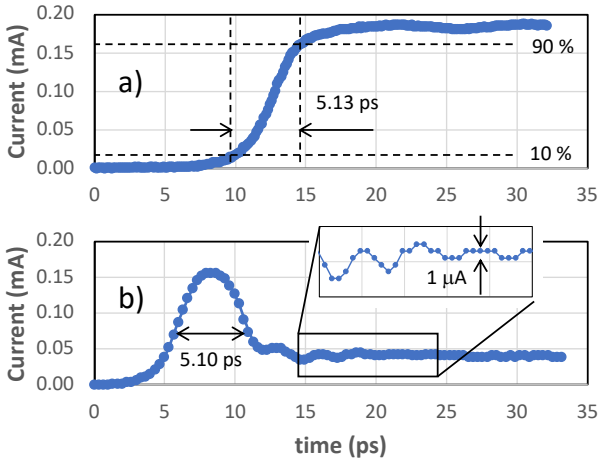

Fig. 9. Sampler response measured at 3.6 K of waveforms from a) the latching SQUID DUT and b) the pulser DUT. The inset shows the discretized output with a minimum current step of 1 μA.

V. Conclusion

In conclusion, a binary search method, used to obtain the response of a Josephson sampler, has been shown to speed up the simulation of the response of a Josephson sampler and has also been implemented experimentally.

Through simulation we obtained a 10% - 90% risetime of 4.7 τ_0 for an idealized sampler. This result is obtained for a comparator junction with a McCumber value, β_c, of 6 to avoid excessive overshoot to a step-input signal. The sampler response simulation predicted a 2.5 ps risetime for an actual sampler circuit, compared to a measured 5.1 ps rise time of a fabricated sampler with the same nominal circuit parameters.

The experimental demonstration required additional averaging because of external noise and crosstalk between the dc bias lines, both of which can be further reduced. As for a digital acquisition method, the binary search approach is preferred over collecting the probability of switching over all bias currents as in [3], since it speeds up the data acquisition significantly using only n sampling events, one for each iteration, instead of 2^{n-1}. Further improvements would entail a higher sampler frequency and a more advanced algorithm. One approach would be selecting a reduced bias range based on any known sampler response and its time derivative. Another possibility is using a variable delay step, optimized based on the derivative of the signal.

Appendix

A. Spice model of a Josephson junction

Use of a SPICE-compatible model of a Josephson junction has previously been reported [26, 27]. The simple SPICE model used here is shown in Fig. 10. It consists of the RCSJ model [20] of a Josephson junction with a non-linear resistance, representing the quasi-particle current shown in Fig. 10c. The subgap resistance was chosen to be 10 times the normal state resistance, R_N. The supercurrent of the junction is modeled with a current source which depends on a voltage representing the junction phase, V_{phase}. This voltage is created by a second current source which depends on the voltage across the junction, V_{JJ}, in parallel to a 1 Farad capacitor, which acts as an integrator.

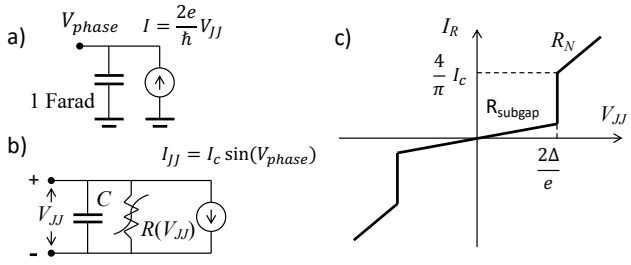

Fig. 10. Simplified SPICE model of a Josephson junction consisting of a) an integrator circuit creating a voltage representing the phase of the junction, b) the RCSJ model with a non-linear parallel resistor. c) Piecewise linear current-voltage characteristic of the resistor.

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Data Availability

The data presented in Fig. 9 will be openly available at https://scholar.colorado.edu/concern/datasets/9306t0730 from the date of publication to allow for commercialization of research findings.

References

[1] S. K. Tolpygo et al., "Advanced Fabrication Processes for Superconducting Very Large-Scale Integrated Circuits," in *IEEE Trans. Appl. Supercond.*, vol. 26, no. 3, pp. 1-10, April 2016, doi: 10.1109/TASC.2016.2519388.

[2] S. Bravyi, O. Dial, J. M. Gambetta, D. Gil, Z. Nazario, "The future of quantum computing with superconducting qubits," *J. Appl. Phys*., vol. 132, October 2022, Art. no. 160902, doi: 10.1063/5.0082975Z.

[3] Z. Cui, J. R. Kirtley, Y. Wang, et al., "Scanning SQUID sampler with 40-ps time resolution," *Rev. Sci. Instrum*. vol. 88, Art. no. 083703, August 2017, doi: 10.1063/1.4986525.

[4] C. A. Hamilton, F. L. Lloyd, R. L. Peterson, et al., "A superconducting sampler for Josephson logic circuits," *Appl. Phys. Lett.,* Vol. 35, pp 718, 1979.

[5] S. M. Faris, "Generation and measurement of ultrashort current pulses with Josephson devices," *Appl. Phys. Lett.*, vol. 36, pp 1005, 1980.

[6] D. B. Tuckerman, "A Josephson ultrahigh-resolution sampling system," *Appl. Phys. Lett*., vol. 36, pp 1008–1010, 1980, doi:10.1063/1.91665.

[7] R. E. Harris, P. Wolf, D. Moore, "Electronically Adjustable Delay for Josephson Technology," *IEEE Electr. Dev. Lett.*, vol. 9, pp 261, 1982.

[8] P. Wolf, B. J. Van Zeghbroeck, and U. Deutsch, "A Josephson sampler with 2.1 ps resolution," *IEEE Trans. Magn*., vol. 21, pp 226 , 1985.

[9] S. Whiteley, E. Hanson, G. Hohenwarter, F. Kuo, and S. Faris, "Technologies for a superconducting sampling oscilloscope/time domain reflectometer," *Interconnection of High Speed and High Frequency Devices and Systems*, Vol. 947 (SPIE, 1988) pp. 138–145.

[10] H. Akoh, S. Sakai, A. Yagi, and H. Hayakawa, "A Direct Coupled Josephson Sampler," *Jpn. J. Appl. Phys*., vol. 22, pp L435-L437, 1983.

[11] T. R. Gheewala, "Josephson-logic devices and circuits," *IEEE Trans. Electr. Dev.*, vol. 27, no. 10, pp. 1857-1869, Oct. 1980, doi: 10.1109/T-ED.1980.20123.

[12] M. B. Ketchen; D. J. Herrell; C. J. Anderson, "Josephson cross-sectional model experiment," *J. Appl. Phys.*, vol. 57, pp 2550–2574, 1985, https://doi.org/10.1063/1.335444.

[13] Y. Zhou, G. -M. Tang, J. -H. Yang, P. -S. Yu and C. Peng, "Logic Design and Simulation of a 128-b AES Encryption Accelerator Based on Rapid Single-Flux-Quantum Circuits," *IEEE Trans. Appl. Supercond.*, vol. 31, no. 6, Sept. 2021, Art no. 1302911, doi: 10.1109/TASC.2021.3075604.

[14] Kaplunenko, V. K., M. I. Khabipov, and E. B. Goldobin. "Experimental investigation of a high frequency sampling system based on shunted Josephson junctions." *Superconductor Science and Technology,* 4, 674 (1991), doi:10.1088/0953-2048/4/11/033.

[15] M. Maruyama, H. Suzuki, T. Hato, H. Wakana, K. Nakayama, Y. Ishimaru, O. Horibe, S. Adachi, A. Kamitani, K. Suzuki, Y. Oshikubo, Y. Tarutani, and K. Tanabe, "Observation of 45 GHz current waveforms using HTS sampler," *Physica C*, vol. 426–431, pp 1661–1667, 2005.

[16] M. Hidaka, T. Satoh, M. Koike, and S. Tahara, "High-resolution measurement by a high-T_c superconductor sampler," in *IEEE Trans. Appl. Supercond.*, vol. 9, no. 2, pp. 4081-4086, June 1999, doi: 10.1109/77.783923

[17] P. Wolf, "Picosecond Sampling with Josephson Junctions," Topical Meeting on Picosecond Electronics and Optoelectronics, Incline Village, NV USA, 1985, paper ThB2 doi: 10.1364/PEO.1985.ThB2

[18] B. J. Van Zeghbroeck, "Model for a Josephson sampling gate." J. Appl, Phys., vol. 57, no. 7, pp 2593-2596, 1985.

[19] W. C. Stewart, "Current-voltage characteristics of Josephson junctions," *Appl. Phys. Lett.,* vol. 12, pp. 277-280, Apr. 1968.

[20] D. E. McCumber, "Effect of ac impedance on dc voltage current characteristics of superconducting weak-link junctions," *J. Appl. Phys.*, vol. 39, pp. 3113-3118, June 1968.

[21] H. H. Zappe, "Minimum current and related topics in Josephson tunnel junction devices," *J. Appl. Phys*., vol. 44, pp 1371, 1973, doi: 10.1063/1.1662354.

[22] https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

[23] D. I. Olaya, J. Biesecker, M. A. Castellanos-Beltran, A. J. Sirois, P. F. Hopkins, P. D. Dresselhaus, and S. P. Benz, "Nb/a-Si/Nb Josephson junctions for high-density superconducting circuits," *Appl. Phys. Lett.*, vol. 122, 2023, doi: 10.1063/5.0148250.

[24] D. I. Olaya; J. Biesecker; M. A. Castellanos-Beltran," Nb/a-Si/Nb Josephson junctions for high-density superconducting circuits," *Appl. Phys. Lett*, vol. 122, pp 182601, 2023, doi: 10.1063/5.0148250z.

[25] R. L. Peterson and C. A. Hamilton, "Analysis of threshold curves for superconducting interferometers", *J. Appl. Phys.*, vol. 50, pp 8135-8142, 1979, doi: 10.1063/1.325954

[26] S. Alam, M. A. Jahangir, and A. Aziz, "A Compact Model for Superconductor- Insulator-Superconductor (SIS) Josephson Junctions," in *IEEE Electr. Dev. Lett.*, vol. 41, no. 8, pp. 1249-1252, Aug. 2020, doi: 10.1109/LED.2020.3002448.

[27] Stenson, Adam. "Modeling Josephson Junctions in LTSPice for Use in Superconducting Single Photon Detector Readout Systems." PhD diss., Dept. Elect. Comp. Eng., Univ. of Rochester, Rochester, NY, USA, 2019.