Testing dielectric slab mode excitation, non-rectangular conductor profiles and edge roughness as sources of additional loss in mmWave transmission lines

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2023 IEEE/MTT-S International Microwave Symposium - IMS 2023 | 979-8-3503-4764-7 /23/$31.00 USG | DOI: 10.1109/IMS37964.2023.10188190

***Abstract*— Losses in mmWave transmission lines often exceed first-principles predictions based on measurements of dc-resistivity and a rectangular conductor geometry. In our case, we observed an additional resistance of coplanar waveguides on $DyScO_3$ substrates. Here, we test three hypotheses concerning the source of the additional resistance: dielectric slab mode excitation, non-rectangular conductor profiles, and conductor edge roughness. We compare the ac-resistance and inductance of coplanar waveguides on $DyScO_3$ substrates mounted on metallic and dielectric chucks. To test the non-rectangular conductor profiles and conductor edge roughness, we implement results from atomic force microscopy of the conductor edge in simulations. Our experiments showed no evidence that the slab mode impacted the additional resistance. Rather, we found that conductor edge profile and roughness may account for some observed additional resistance. We expect these findings to impact the choice between stepper lithography and microlens array lithography for rapid prototyping and multiproject wafers in industrial processes.**

I. Introduction

Operating at millimeter wave (mmWaves) frequencies enhances data rates and decreases latency in electronic devices. At ever increasing device operating frequencies, power loss in transmission lines often exceeds predictions based solely on the metal conductivity and the nominal transmission line geometry. Understanding and mitigating these losses is crucial to the advancement of mmWave electronics. To understand this problem better, we studied the distributed circuit parameters of coplanar waveguides (CPWs) on $DyScO_3$. We chose $DyScO_3$ because it serves as a substrate for many epitaxial thin films with extraordinary material physics [1,2].

There are several models for approximating additional loss in transmission lines. Among the most common include radiation [3,4,5], trapezoidal conductor profiles [6,7,8] and surface roughness [9,10,11,12]. In real world transmission lines, these three loss mechanisms coexist, making it easy to attribute loss incorrectly or assign inexplicable loss to physics that is simply not present in the system-under-test.

In the following, we test three hypotheses to account for the additional resistance that we observed in CPWs on $DyScO_3$ substrates: excitation of the dielectric slab mode, non-rectangular conductor profiles and conductor edge roughness. We first present comparative measurements of CPWs on a $DyScO_3$ substrate measured on a dielectric versus a metallic chuck to test for dielectric slab mode radiation. Next, we discuss how we extract a non-rectangular conductor profile and edge roughness from atomic force microscopy (AFM) measurements and how we implement these features into simulations. We find that each factor separately is insufficient to account for the observed additional resistance, although the edge roughness model can be tuned to closely resemble the frequency dependence that is observed in experiment.

II. Methods

A. Wafer Layout and Fabrication

We fabricated CPWs on a 10 mm × 10 mm (110)-oriented 500 µm thick $DyScO_3$ chip with standard lithographic techniques. The electrodes are nominally 500 nm thick gold with a 10 nm titanium adhesion layer. The CPW's nominal geometry is a 20 µm wide center conductor separated from 200 µm wide ground planes by 5 µm wide gaps. Our chip layout included a short circuit reflect and a set of CPW transmission lines with lengths ($l = 0.420$ mm, 0.660 mm, 0.880 mm, 1.340 mm, 2.240 mm, 4.020 mm, 7.500 mm) that were optimized to minimize the maximum error across the frequency range of interest (1 GHz to 110 GHz) when using the multiline thru-reflect-line (mTRL) calibration algorithm [13].

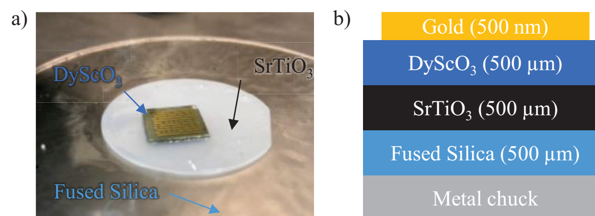

Fig. 1. $DyScO_3$ chip on a dielectric $SrTiO_3$ chuck: (a) photograph, (b) sketched outline of the material layers.

To test the slab mode, we mounted the chip either directly to a metal chuck or to a compound dielectric chuck with 0.5 mm thick $SrTiO_3$ (STO) ($\varepsilon_r \approx 300$) on 0.5 mm thick fused silica ($\varepsilon_r \approx 3.82$) (Fig. 1). We chose a high dielectric constant chuck following [4]. To glue the chip onto the STO chuck, we spin-coated wax onto the chuck and placed the $DyScO_3$ chip on top. We removed any remaining air between the chip and the chuck in a vacuum oven at 134 °C. Measuring the thickness of the whole stack lets us estimate the wax thickness to be below

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50 µm, so we assume that we can neglect the dielectric influence of the wax. The Fused Silica wafer does not fulfill any dielectric role but was solely used for the waxing process.

B. *On-Wafer Calibration*

We used on-wafer ground-signal-ground probes to contact each device and measured two-port scattering parameters with a vector network analyzer (VNA). Next, we applied the mTRL algorithm and determined the propagation constant $\gamma(\omega)$ of the CPWs [13]. As the CPW represents a single-mode transmission line, the propagation constant $\gamma(\omega)$ is [14]:

$$\gamma(\omega) = \sqrt{(R + i\omega L)\,(G + i\omega C)} \tag{1}$$

Here, R, L, C and G denote the frequency-dependent resistance, inductance, capacitance, and conductance per unit length, respectively. We approximate $DyScO_3$ as a dispersion-less and therefore by the Kramers-Kronig relations lossless substrate ($C(\omega) = C_0$ and $G(\omega) = 0$), which is reasonable to assume based on the measurements in [15]. In this approximation, C_0 is determined from a series resistor calibration [16,17]. We obtain R and L including their uncertainties based on the dispersion-less substrate assumption and the measured $\gamma(\omega)$.

C. *Atomic Force Microscopy*

We characterized the edge profile of the conductors using atomic force microscopy (AFM) (Fig. 2). These images suggest deviations from the ideal rectangular edge profile (Fig. 2 b,c). We attribute these deviations to our lithography and metallization process: In this work we used a lift-off resist process, which can produce a sigmoidal shape in the vicinity of the nominal conductor edge. We also observe variation of the conductor profile along the CPW, which we refer to as the roughness. We attribute the roughness to our maskless, direct write lithography and metal deposition process.

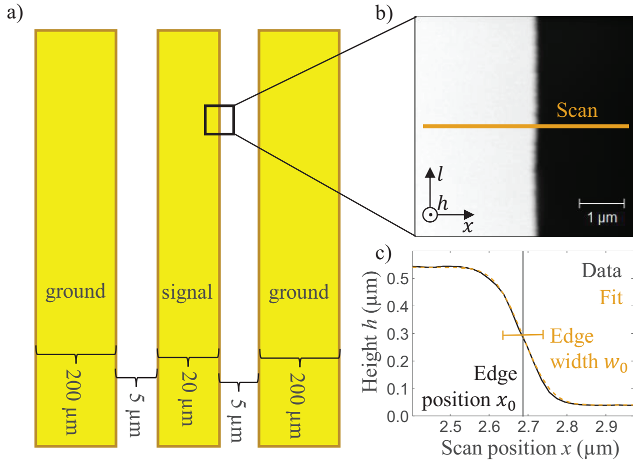

Fig. 2. Extraction of edge position x_0 and edge width w_0 from AFM measurements: (a) Top view sketch of the CPW. (b) Top view of the AFM height profile of the conductor edge. (c) Side view of a single layer AFM scan $h(x)$ and a fit based on (2).

We evaluated our AFM edge profile image (Fig. 2b) by fitting each row with the cumulative distribution function of a Gaussian (Fig. 2c):

$$h(x) = \frac{h_0}{2}\left(1 + \mathrm{Erf}\left(\frac{x - x_0}{\sqrt{2}\,w_0}\right)\right) \tag{2}$$

Here, h is the height at location x across image and h_0 is the average thickness of the conductor. For each of the 251 profiles, which span 5 µm, we obtained two fit parameters: the edge width w_0 and the edge position x_0 (Fig. 2c). Next, we use the average width $\langle w_0 \rangle$ and the standard deviation of the edge position $\sigma(x_0)$ to model the non-rectangular conductor profile and roughness, respectively, using a 2D cross-section simulation. In our case, the mean edge profile had $\langle w_0 \rangle =$ 38 nm and roughness of $\sigma(x_0) = 13$ nm. Note that the three-dimensional shape of the AFM tip limits the observed shape of the conductor. Hence, the edge profile $\langle w_0 \rangle$ should be seen as an upper bound on the sharpness of the conductor edge rather than being interpreted as the physical edge profile. On the other hand, we don't expect the roughness $\sigma(x_0)$ to be subject to this tip convolution. Rather, it might underestimate the physical roughness and thereby the associated additional resistance, as the tip does not probe smaller features than the tip itself.

D. *Finite Element Simulation*

At low frequencies, it is often sufficient to model each conductor as a rectangle with a 2D finite element simulator. In this case, we simulate a conductor with the height and width measured with a low-resolution contact profilometer to account for deviations from the nominal geometry.

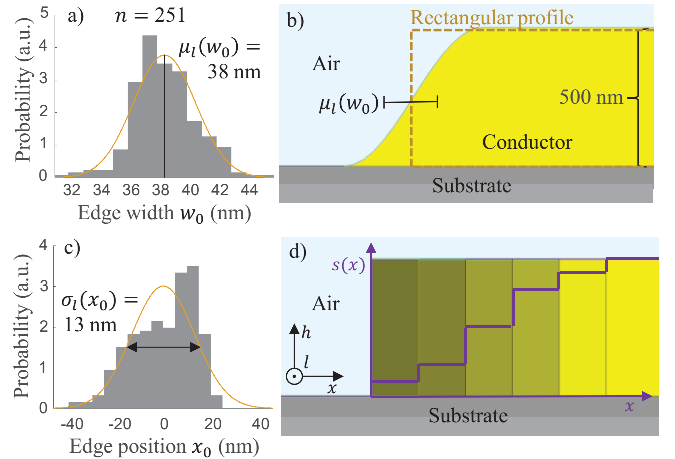

Fig. 3. Conductor edge profile and roughness as extracted from AFM measurements and as implemented in simulation: (a) The distribution of edge width w_0. The mean $\mu_l(w_0)$ is implemented as conductor profile $h(x)$ in (b). The width is exaggerated for better visibility. (c) The distribution of the edge position x_0. The standard deviation $\sigma_l(x_0)$ is implemented in the conductivity profile $s(x)$ in (d) according to (3).

To account for non-ideal conductor profiles measured with AFM, we implemented a rounded conductor edge with width $\langle w_0 \rangle$ in the 2D simulation (Fig. 3 a,b). Separately, to account for edge roughness along the CPW, we implemented a

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conductivity profile $s(x)$ (Fig. 3 c,d) to model conductor profile variation along the CPW [11]. This roughness model assumes that the electromagnetic field interacts with the "mean" conductor surface, which we approximate as a conductivity profile $s(x)$. Hence, we take the standard deviation of the conductivity profile as equal to the standard deviation of the edge position, $\sigma(x_0)$:

$$s(x) = \frac{s_0}{2}\left(1 + \mathrm{Erf}\left(\frac{x - \mu_l(x_0)}{\sqrt{2}\,\sigma(x_0)}\right)\right) \quad (3)$$

Here, s_0 is the bulk conductivity of the metal and $\mu_l(x_0)$ is the mean position of the edge. In our 2D simulation, we approximated the smooth profile $s(x)$ as a stepped profile with five intermediate conductivities (Fig. 3d).

III. Results

A. Dielectric Slab Mode Excitation

To test the slab mode excitation hypothesis, we compared the measured distributed resistance R and inductance L on a metal and dielectric chuck to the simulation of a rectangular conductor (Fig. 4). We expect the slab mode to show up as additional R as radiative loss [3]. The simulation is a quasi-static 2D finite element simulation and therefore does not include the slab mode. In general, it is difficult to simulate the slab mode as it depends on the surrounding wafer architecture [4]. In our experiment, L was consistent between the three different cases (metal chuck, dielectric chuck, and simulation, Fig. 4b). In contrast, the results for R (Fig. 4a), show agreement between the dielectric chuck and metal chuck but both deviate by the same amount from the simulation. This deviation becomes relevant at about 40 GHz, which is also the critical frequency of the dielectric slab mode in our geometry [3]. This critical frequency initially pointed us to the slab mode as the likely culprit for the deviation, but the results on the dielectric chuck suggest otherwise. This observation implies that either the choice of dielectric chuck or the slab mode is not the cause of the additional loss observed in our measurements.

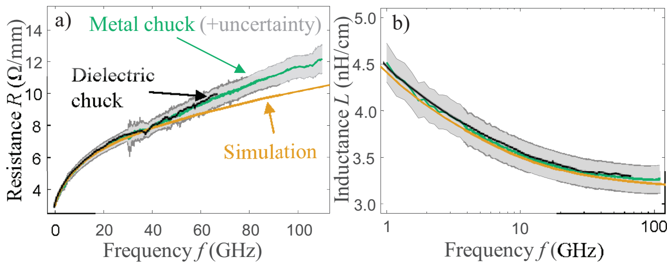

Fig. 4. Measured distributed resistance R (a) and inductance L (b) on a metallic and dielectric chuck compared to the simulation of a rectangular conductor. R and L are respectively plotted on linear and logarithmic frequency scale for better visibility of the deviations. The data on the dielectric chuck is only shown up to 67 GHz.

B. Conductor Edge

To test the effect of the conductor edge profile, we performed a simulation using the measured non-rectangular conductor edge and another simulation using the measured conductor roughness (Fig. 3) and compared them to experimental results (Fig. 5). While these simulations also did not agree with the measured R, they did show an increase in R. To improve the agreement, we performed simulations with an increased non-rectangular conductor edge, $\mu_l(w_0) = 150$ nm, and an increased conductor roughness $\sigma_l(x_0) = 150$ nm. Both these values are larger by a factor of 4 and 12 than the values evaluated from the AFM profiles, respectively.

Even though these values are much larger than what we measured, these simulations demonstrate that the roughness and non-rectangular edge profile do lead to additional resistance R (Fig. 5). They also show how these factors impact R and L as function of frequency. For instance, edge roughness does not significantly impact L, but it does have the same frequency dependence in R as the measurement. On the other hand, increased edge widths did impact the L, which we attribute to the current pushing further into the edges compared to a rectangular profile. Thus, edge roughness and profile can be qualitatively distinguished.

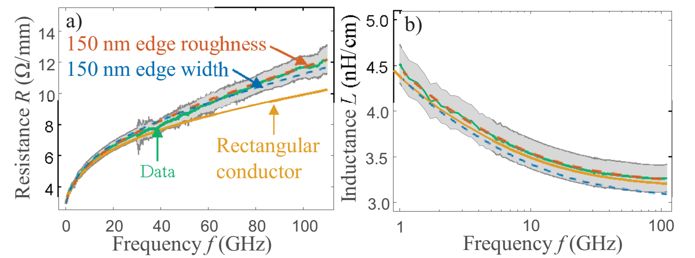

Fig. 5. Simulated distributed resistance (a) and inductance (b) of a rectangular conductor, a non-rectangular conductor with $\mu_l(w_0) = 150$ nm and a conductor with edge roughness $\sigma_l(x_0) = 150$ nm compared to the measurement. R and L are respectively plotted on linear and logarithmic frequency scale for better visibility of the deviations. We omitted the $\mu_l(w_0) = 38$ nm and the $\sigma_l(x_0) = 13$ nm simulations because their deviation from the rectangular conductor simulation are invisible in the figure.

IV. Conclusion

In conclusion, our objective was to understand why the measured distributed resistance per unit length of coplanar waveguides may deviate from 2D simulations of their nominal rectangular geometry. Currently, most research in the literature points to slab mode excitation or conductor roughness as possible explanations for the measured deviation between measurement and simulation. Our experiments showed no evidence that the slab mode influenced the deviations in R between our measurement and simulations. Rather, we found that conductor edge profile and roughness may account for some observed additional R. Future work will attempt to combine both profile and roughness into a single simulation. More broadly, industrial researchers should carefully consider edge profile and roughness for a given lithography and metallization process when designing devices at mmWaves. This finding is particularly true for microlens array lithography that may be prone to step edge artifacts.

Acknowledgment

We thankfully acknowledge fruitful discussions with Wolfgang Heinrich.

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