A field-effect transistor-based room-temperature quantum current source

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Abstract: This work provides a proof-of-concept demonstration of the room-temperature quantum current source based on nanoscale metal-oxide-semiconductor-field-effect-transistor (MOSFET). Using a low leakage MOSFET design, the current source achieved 1.00011 ± 0.00022 charges per cycle without any leakage correction scheme. The achieved accuracy is limited by noise in the very low level of measured current, and by calibration uncertainty

Key words: quantum current; MOSFET; room temperature; charge-pumping

Electrical measurements are almost always the end steps of scientific investigations. Precision electrical measurements are therefore of critical importance to science and technology. Precision electrical measurements are not possible without standards to calibrate against. Of electrical standards, the current standard is the weakest in development. In 2018, the ampere was redefined as of 1/ (1.602176634 x 10^{-19}) elementary charges per second [1], linking electric current to the fundamental unit of charge. The development of a current source that adheres to such a definition, namely controlling the flow of electrons one at a time, has been ongoing for three decades [2-16]. However, two major shortcomings of this approach persist – current level which are too low (picoamps) and the need for sub liquid Helium cryogenic temperatures.

The control of electrons flowing one at a time relies on a phenomenon called Coulomb blockade. By using a small enough quantum dot, an electron inside the dot will prevent additional electrons from entering and electron flow is limited to one at a time. However, it is difficult to reliably make dots small enough that their charging energy is large compared to kT/q at room temperature. Here k is the Boltzmann constant, T is temperature in Kevin and q is the electron charge. Recently, a radical departure from this paradigm has been proposed [17]. In the proposed approach, a broken chemical bond (a quantum state deep in the bandgap occupied by one electron) becomes the ultimately scaled quantum dot. Instead of utilizing Coulomb blockade, the much stronger Pauli's exclusion principle is relied on to ensure that electron flow is maintained at one at a time. This concept can be realized in technologically matured, nanoscale MOSFETs. With the ultimate quantum dot and the stronger electron gating force, the proposed quantum current source will operate reliably at room temperature.

The proposed concept was explored using an advanced MOSFET (90 nm node) optimized for logic operations [17]. MOSFETs optimized for logic performance aggressively thin down the gate oxide, leading to high level of gate leakage current that confounds the demonstration of the quantum current source. Even after employing an elaborate leakage current removal scheme, previous demonstrations were limited to an accuracy of 0.996 charges per charge-pumping cycle. In this work, the earlier demonstration is revisited utilizing advanced MOSFETs optimized for low leakage requirements (MOSFETs in the DRAM peripheral circuitry) to demonstrate the viability of the proposed quantum current source concept.

The proposed MOSFET-based quantum current source concept relies on the well-known charge pumping (CP) method to measure defect states at the interface between SiO_2 and silicon substrate [18]. It works by rapidly switching the MOSFET (changing gate voltage) between strong inversion and strong accumulation. In the strong inversion half cycle, electrons from the source and drain flood the channel and completely fill the defect states with electrons (fig. 1). As the MOSFET transitions

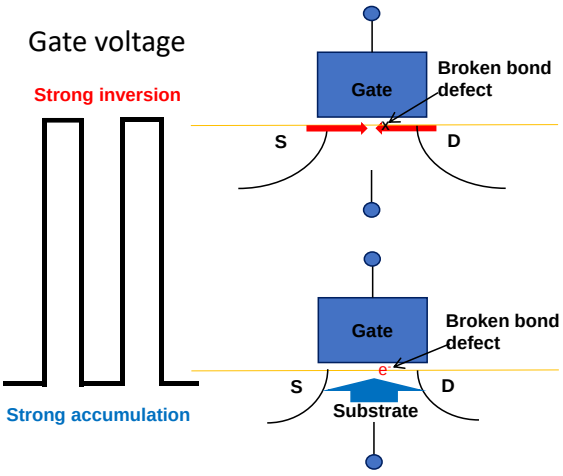

Figure 1 Illustration of a MOSFET charge-pumping measurement of interface states. Left hand side illustrates the square wave applied to the gate terminal switching the MOSFET from strong inversion to strong accumulation rapidly. Right hand side depicts how the electrons flood the channel from source and drain during strong inversion and fill the defect state (broken interface bond). During strong accumulation part of the cycle, the holes flood in after the electrons are returned to the source and drain, neutralizing the electron localized at the defect and producing a substrate current.

to the strong accumulation half cycle, all the electrons in the channel flow back out to the source and drain, except those captured by the defect states. Holes from the substrate quickly build up at the interface and the captured electrons are neutralized. This capture and neutralization combination effectively pump electrons from the source and drain to the substrate, leading to a net substrate current that is directly

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proportional to the number of defects at the interface and the switching frequency. When there is only one defect at the interface, this process then pumps one electron at every pumping cycle – the definition of a quantum current source.

Note that the term "charge-pumping" is also used in Coulomb blockade-based quantum current sources [2-16], the meaning is not the same as the one discussed here. The reason that a different terminology is not chosen here is because the method discussed here has a longer history and is widely employed in the semiconductor field.

The requirement that the MOSFET has only a single interface defect seems challenging, but it is common when the MOSFET geometry is at the nanoscale. High quality SiO_2/Si interfaces have a typical defect density on the order of $10^{10}/cm^2$. A 100 nm by 100 nm MOSFET has an active area of 10^{-10} cm^2 and therefore, on average, has only a few defects per device. Statistically, finding single-defect devices is quite possible. We note that MOSFETs with dimensions much smaller than this (100 nm x 100 nm) are already in production.

There is plenty of evidence that the identity of interface defects are silicon dangling bonds [19, 20] which is a non-bonding quantum state of a silicon atom at the interface between silicon crystal and the amorphous SiO_2 layer. In the absence of a magnetic field, each quantum state can accommodate two electrons with opposite spin. As a non-bonding state, one electron is already there. It can only accept one additional electron with opposite spin because of Pauli's Exclusion. This guarantees that there will never be overfilling which is an important source of error.

Fig. 2 illustrates how the dangling bond quantum state is facilitating the one charge at a time transfer from conduction band (connected to source and drain of the MOSFET) to the substrate. During strong inversion, the high density of inversion electrons quickly fills the dangling bond state, leading to a pair of occupying electrons with opposite spin. In the case where only one interface defect exists, there is no other quantum state within the silicon bandgap and therefore no other electron capture can occur. During the strong accumulation half cycle, one of the electrons will be emitted to the valence band (substrate). The emission of the other electron, leading to a negatively charged dangling bond state requires the silicon change from sp^3 to sp^2 hybridization, which involves a strong barrier [17] (For example, conversion of diamond to graphite is a sp^3 to sp^2 conversion). Thus, during the short time of strong accumulation, the dangling bond returns to neutral state only and the cycle repeats.

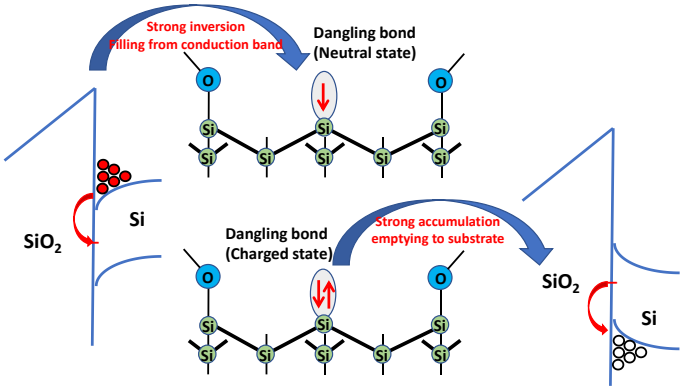

Figure 2, Illustration of how the Pauli's exclusion principle limits the dangling bond interface defect to accommodate a maximum of two electrons. Since it contains one electron, it can only accept one additional electron with opposite spin. During the inversion half cycle, this additional electron is provided by the inversion layer. During the accumulation cycle, one of the electron is emitted to the substrate thereby completes one charge transfer.

Intuitively, the non-bonding state for a pure material should be at the middle between the bonding and antibonding state. Due to symmetry of the molecular orbital hybridization, the dangling bond can actually take two stable energy levels depending on the gate bias and both are deep in the silicon band gap [17] about 0.1 to 0.2 eV above or below mid gap. Thus, even though the captured electron or hole can jump back out to the silicon conduction or valence band, it is difficult because they are about 0.4 eV away. Room temperature operation is possible because of this > 15 kT/q emission loss barrier of the captured electrons .

The MOSFETs used in this work are 90 nm x 70 nm in size with 3.5 nm SiO_2 gate oxide and polysilicon gate. The flat band voltage and threshold voltage are, -0.65 V and 0.65 V, respectively. Only n-channel devices are used. To hunt for suitable single defect devices, the fixed base, variable height CP method [21-23] was used (figure 3a). The fixed base was set at -2 V, well beyond the -0.65 V flat band value for strong accumulation. The top gate voltage was swept from -0.7 V to 2V, spanning below flat band to strong inversion. The CP frequency was 1 MHz. The rise/fall time of the CP waveform was 2 ns. At 1 MHz, one expects a single charge pump to result in 0.16 pA (10^6 electrons per second) of measured current.

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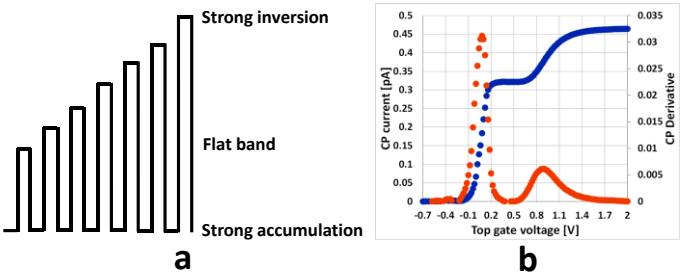

Figure 3 **a**: Illustrating the sweep of top voltage of the charge-pumping (CP) wave form while keeping the base fixed at strong accumulation. The top voltage varies from slightly below flat band to strong inversion. This variable top gate voltage CP scan for defects available for CP. **b**: an example of the scan result showing two steps (blue curve). The first one rises up to 0.32 pA, which is the right magnitude for two defects at 1MHz CP. The second one never reaches 0.48 pA, a defect that is not an interface state. The orange curve is the derivative meant to highlight the transitions.

Fig. 3b shows a representative result. The blue curve is the CP current while the orange curve is the derivative of the CP current. A fast rise from zero to 0.32 pA happens at 0.06 V and levels off at 0.2 V, indicating two defects (0.16 pA + 0.16 pA = 0.32 pA) located at the edge of the channel where the doping level is affected by the source and drain. A second slower rise happens at 0.92 V but did not reach 0.48 pA (3 charges) even at 2V, suggesting this is not a true interface defect. The detailed interpretation of the measured result is beyond the scope of this work. However, it is sufficient to conclude that results shown in fig. 3b indicate the participation of more than one type of defect deems this device unsuitable for the purpose of a quantum current source. Instead, a suitable device should have only one fast rise to 0.16 pA and then plateaus for the remainder of the gate voltage sweep (fig. 4). Reaching 0.16 pA is an important indication that the defect is fully engaged in the CP cycle at least for the frequency of 1MHz, making it a true interface state, and doing so in a single step implies that there are no additional defects playing a role in the capture and emission processes.

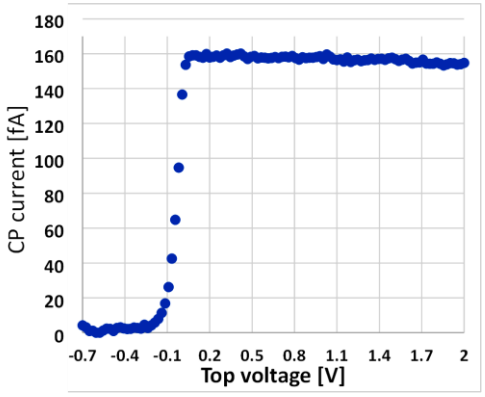

Figure 4 The CP current from a single interface defect. A single step-rise to 0.16 pA level (1 defect) is observed.

The initial survey of nearly 400 devices resulted in only 11 which meet this criterion (2.75%). This number is statistically lower than expected from the average interface state density. However, it is encouraging because billions of such transistors can be fabricated on a single chip which should result in 10's of millions of ideal single defect transistors.

For the selected single defect devices, CP (strong inversion to strong accumulation gate waveform) was measured as a function of frequency. In this measurement, the slope of the line should correspond to the number of charges pumped per cycle. Fig. 5 shows two representative results. As expected, the CP current is linearly dependent on frequency with a slope in Coulombs. Converting to elementary charge per Hz, they are 0.9998 ± 0.0002 (fig. 5a) and 0.9997 ± 0.0008 (fig. 5b).

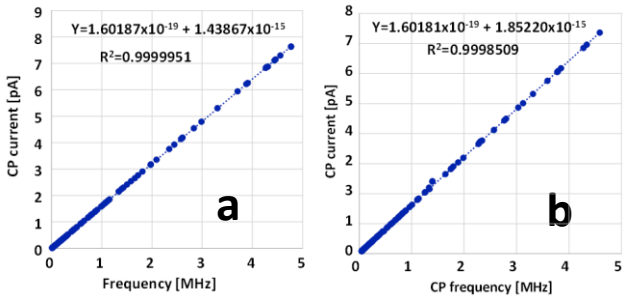

Figure 5 CP current as a function of frequency is a linear function with a slope equals Coulombs. **a** and **b** are two examples with b has a slightly higher noise level and therefore a poorer fit.

To ensure the accuracy of results shown in fig. 5, several calibration steps were taken. First is the calibration of the detector which includes the current amplifier and the digitizer. A low-level current source consisting of a precision voltage source (also calibrated using an 8½ digit calibrated multimeter) and a known 1GΩ resistor was utilized to calibrate the detector. Since the measured current is in the fA to pA range for the calibration, the accuracy of the GΩ resistor is the remaining limiting factor. Without more elaborate temperature stabilization, the current measurement accuracy is limited to ≈200 ppm.

As seen in fig. 4, the CP current from top gate voltage of 0.2 V to 2 V is not constant and subject to a drift. . This is due to the baseline drift of the current amplifier. Fig. 6 shows the measured CP current for a MOSFET that has no defect at the interface (@ 1MHz). The "zero" current level shifts during the measurement.

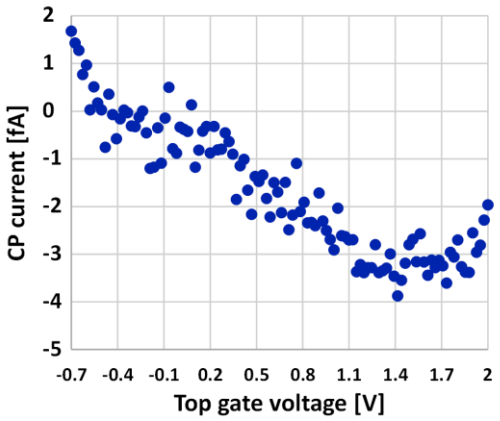

Figure 6 CP current when there is no defect at the interface of the MOSFET. The change in CP current is the baseline drift of the current amplifier.

To minimize the impact of these baseline drifts on accuracy, two methods were employed. The first method involved measuring the CP currents of a higher frequency and a fixed lower frequency in rapid succession (2 seconds) and taking the difference as the CP current associated with the frequency difference. The choice of 2 seconds is a tradeoff between noise reduction by integration time and the potential amount of drift. Longer integration times will decrease the noise but will increase the potential error due to drift. The remaining noise level with the 2 second integration time can be seen from fig. 5 which is around 1.5 fA, which is ~100x lower than the charge pumping current resulting from a single defect.

The second method is to randomize the measurement frequencies so that the drift would not contribute to a systematic error. This is accomplished by using a random number generator to pick the frequency value from range of interest for measurement (logarithmic spacing). This randomization is reflected on the uneven frequency distribution in fig. 5a and 5b. While the plots are arranged sequentially in frequency, the measurement order is random in time.

The measured results of 11 single-defect devices are plotted in fig. 7. The average of the 11 devices are 1.00011 ± 0.00022 charges per cycle. The standard deviation for each device varies significantly. This is due to the noise pick up of the measurement system which is somewhat larger than the detection noise level. The measurement system was housed in a Faraday cage which helps reduce noise but does not eliminate all low frequency noise. There are remaining contributions from the power line noise which varies depending on machinery operations in nearby laboratories.

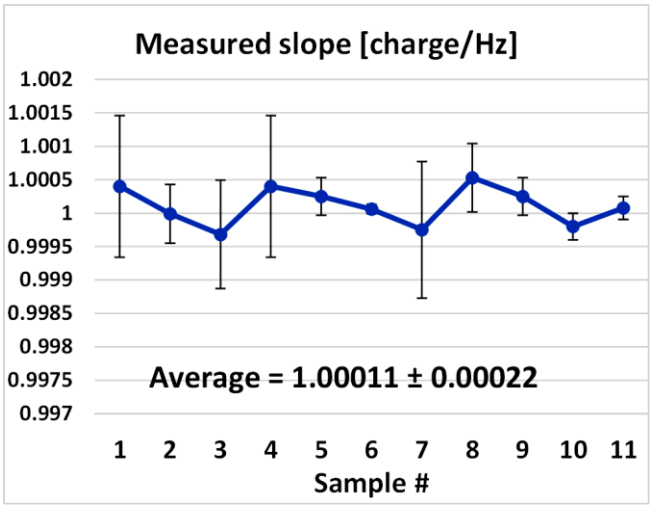

Figure 7 The measured CP vs frequency slope after converting Coulomb to electron charge for 11 single defect devices. The average of all 11 devices is also shown. The errors bars represent standard deviation.

Each of these devices have been measured more than once (generally on the same day) and the results are repeatable. Unstable devices are not included here. The stability of the device is an important question. We used harsher CP condition (-3 V to 3 V) on devices with zero defects and found that it takes hours to create an additional interface defect. We can conclude that the CP conditions utilized in this study (-2 V to +2 V) are mild enough to not generate additional defects. However, we do note some remaining defect instability in some devices (not included in the 11 devices). This includes transient increases/decreases in the number of defects during the measurement. These instabilities are related to the nature of the interface defects which is still a topic of ongoing research.

A comparison with the earlier results in [17], reveals an improvement in the charge per cycle accuracy from 0.996 to 1.00011. In [17], the accuracy was heavily dependent on the leakage current correction which has been minimized in this work due to improved device quality. Note that leakage current is non-zero even for the thicker oxides used in these devices, as can be seen from the zero Hz intercepts of fig 5a and 5b. However, the leakage is low enough in these devices to not limit the ultimate uncertainty achieved in this experiment. The accuracy is close to the accuracy of the current calibration, which is slightly worsened by noise contributions. Within the accuracy limits discussed above, one can conclude that this approach yields one charge per cycle observations and proves the viability of such an approach as a quantum current source.

We have used the measurement shown in fig. 4 to identify “suitable” signal defect devices. In fig. 3 we also showed an example of additional defects contributing to the pumped current at fractional charge and argued that such a device is obviously not suitable as a quantum current source. There is a finite probability that there are additional contributors contributing a very small fraction of a charge per cycle such that one cannot easily tell from curve shown in fig. 4. Such

contributor likely to be near interface defects with energy near the band edge. The probability of having such contributor is very small but not zero. It depends on the quality of the oxide and the design of the transistor. Had it not been for these unwanted, incomplete charge contributors, one could simply use many interface states (from a larger device) to achieve higher current level. As such, we must rely on the combination of measurements depicted in fig. 4 and 5 to guard against such contributors. How well one can do that depends on how low one can reduce the measurement noise. This problem can potentially limit the accuracy of this proposed quantum current source.

Efforts to further improve the accuracy are centered on calibration improvements, decreased measurement noise levels, and the acquisition of lower leakage (thicker oxide) devices. To achieve higher current level, many single defect transistors can be connected in parallel through on-chip circuitry that can select and verify only those transistors that are suitable quantum current sources. Theoretically, millions of single defect-based quantum current sources can be connected to achieve μA level of current without losing accuracy.

The concept of nano MOSFET as room temperature quantum current source is demonstrated at the 220-ppm accuracy level. It has been proven to within the limit of uncertainty given by the combination of calibration (200-ppm accuracy) and noise. This serves as a proof-of-concept demonstration of the viability of a charge pumping based quantum current standard which operates at room temperature.

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