Nb/*a*-Si/Nb-junction Josephson arbitrary waveform synthesizers for quantum information

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***Abstract*—We demonstrate Josephson arbitrary waveform synthesizers (JAWS) with increased operating temperature range for temperatures below 4 K. These JAWS synthesizers were fabricated with externally-shunted Nb/a-Si/Nb junctions whose critical current exhibits improved temperature stability compared to the self-shunted Nb/$Nb_{0.15}Si_{0.85}$/Nb junctions typically used. Vertical stud resistors made of 230 nm of PdAu were developed to provide the milliohm shunt resistance required for junction overdamping while maintaining a small footprint suitable for high-density series arrays embedded in a coplanar waveguide. We evaluated the performance of these resistors from 3.8 K down to 20 mK. We designed, fabricated and tested a JAWS circuit with 4650 externally shunted Nb/a-Si/Nb JJs with a critical current density (J_c) of 0.12 mA/μm^2 and critical current (I_c) of 3 mA. This circuit was designed to be mounted to the 3 K stage of a dilution refrigerator and used to control and calibrate a qubit mounted at the 10 mK stage. To increase the circuit density of the JAWS circuits we made arrays of two-junction vertical stacks. Current-voltage (*I-V*) curves of this JAWS circuit with stacked junctions under microwave excitation show Shapiro steps with quantum-locking ranges similar to those of JAWS circuits used for qubit control.**

***Index Terms*—Josephson junctions, superconducting electronics, Josephson devices, single flux quantum, fabrication process.**

I. Introduction

THE Josephson arbitrary waveform synthesizer (JAWS), with quantum-based accuracy arising from the ac Josephson effect, has been developed as the primary ac voltage standard at audio frequencies [1], [2]. The JAWS circuit contains a series array of N superconducting Josephson junctions (JJs) that transform an imperfect digital input stream of pulses into an analog sequence of quantized pulses. Either a dc-offset sine wave or a pulse generator is typically used as the input drive source at a frequency f near the junction characteristic frequency $f_c = I_c R_s / \Phi_0$, where I_c is the critical current of the junction, R_s is the shunt resistance across the junction, and Φ_0 is the flux quantum. The JAWS output pulses are distinguished from the input drive pulses by their quantized time-integrated voltage of $N\Phi_0 = N(h/2e)$, where h is the Planck constant and e is the electron charge. When the JAWS circuit is "quantum-locked", each pulse in the input sequence produces one single-flux quantum (SFQ) pulse from each JJ in the JAWS circuit. These circuits were designed to operate at or near the boiling temperature of liquid helium ($T = 4.2$ K) and provide a stable, calculable, and reproducible output that is identical for each device and where the output is constant over a range of input bias parameters and environmental conditions; we refer to these ranges as the quantum locking ranges (QLRs).

More recently, NIST has been working on extending JAWS into the RF frequency range (RF-JAWS) to provide arbitrary waveform reference sources for RF metrology to support the communications industry [3]–[6]. Recent work has focused on calibrating higher frequency synthesized waveforms up to 3 GHz [4], [5] and increasing the output power (up to -28 dBm at 1 GHz) [6]. These circuits are also designed for 4 K operation and typically have robust QLRs for RF input power and dc bias current when 1) the temperature T of the device is held stable: $\Delta T \leq 50$ mK, and 2) the RF input frequency f is within ~ 50 % of the junction characteristic frequency f_c, i.e. $f/f_c > 0.5$ [7]. Typical values for our RF-JAWS circuits operated at 4 K have $f_c \sim 20$ GHz with $f/f_c \sim 0.7$. Due to the temperature dependence of the junction I_c, which translates to temperature dependence of both f_c and the nominal input bias values necessary for driving the junctions into quantum-locked behavior, these input bias QLRs can change significantly as the temperature is reduced below 4 K.

In this work, we report on the design, fabrication and testing of RF-JAWS circuits which can produce constant output over a broader temperature range, for nominal temperatures $T \leq 4$ K and fixed input bias values. This increase in the temperature QLR is achieved by using superconductor-insulator-superconductor (SIS) Josephson junctions (JJs) in the JAWS circuits instead of superconductor-normal metal-superconductor (SNS) JJs. We experimentally verify this improvement in device temperature QLR by measuring the circuit output from 3.5 K to 4.1 K and compare to a circuit of our previous (SNS) design. The improvement in operating temperature range and decreased sensitivity to temperature variations enables new applications for JAWS circuits for systems operating below 4 K, such as applications in quantum information where a cryogenic, stable, and reproducible microwave source could be used in the classical circuits that

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 This research is partially supported by the Office of the Director of National Intelligence (ODNI), Intelligence Advanced Research Projects Activity (IARPA), under Interagency Agreement IARPA-20001-D2022-2203120004. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the ODNI, IARPA, or the U.S. government.

interface with a quantum processor [8] or as a reference source for microwave metrology inside a dilution refrigerator (DR). A JAWS circuit described in this work and mounted at the 3 K stage of a DR has been used as a pulse generator to digitally control a transmon qubit mounted at the 10 mK stage [9].

II. Fabrication

Traditionally, NIST has used self-shunted Nb/Nb$_x$Si$_{1-x}$/Nb Josephson junctions to make high-speed, compact arbitrary waveform synthesizers for voltage metrology and more recently for use as RF reference sources [10], [11]. These junction barriers are amorphous (a-) and metallically-doped, providing a self-shunting, normal conduction path through the junction and the necessary level of overdamping (Stewart-McCumber parameter $\beta_c \ll 1$). As mentioned above, the strong temperature dependence of I_c of the junctions used for these synthesizers results in a limited operating temperature range and a sensitivity to temperature changes. To expand the operating range, we developed a process for fabricating long arrays of externally shunted Nb/a-Si/Nb Josephson junctions with a critical current density (J_c) of 0.12 mA/μm^2. As shown in Fig. 1, the measured temperature dependence of I_c for these junctions is dramatically reduced below 4 K as compared to NbSi junctions.

Typically, AlO$_x$ is used as a barrier in junctions for superconducting electronics applications. We use a-Si instead of AlO$_x$ as the junction barrier material because: 1) the a-Si barriers are about 5 times thicker than AlO$_x$ barriers at the same J_c, making it easier to achieve the desired J_c; 2) thicker barriers result in higher yields, lowering the occurrence of outlier junctions with higher than desired I_c; and 3) a-Si junctions allow the possibility of making vertical junction stacks, decreasing the circuit area.

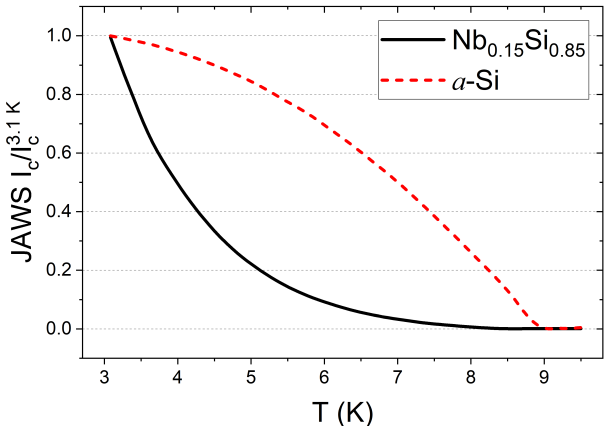

Fig. 1. Measured, normalized I_c vs. temperature for a JAWS device with 4500 Nb/NbSi/Nb junctions and for a similar JAWS device with 4650 Nb/a-Si/Nb junctions. The ratio of slopes at 3.1 K is $\approx$ 20 (NbSi/Si). Below 3 K, the I_c of the Nb/a-Si/Nb JAWS circuit is expected to follow typical SIS asymptotic behavior and the Nb/NbSi/Nb SNS junctions become superconducting shorts via the proximity effect.

The a-Si JAWS circuits are fabricated on 3-in (76.2 mm) silicon wafers with a thermal oxide layer of 150 nm. A schematic of the fabrication steps can be seen in Fig. 2. A trilayer of Nb/a-Si/Nb is deposited by dc sputtering, the substrate is rotated during deposition and kept at room temperature by back-flowing nitrogen gas. Photolithography is done with an i-line stepper. Junctions are defined using reactive ion etching (RIE) in a mixture of SF_6 and C_4F_8 gas and using laser reflection endpoint detection. Next, definition of the base electrode is done using SF_6 RIE. Deposition of resistors is done by electron beam evaporation after preparing a double-layer resist stack consisting of $\approx$ 0.65 μm of lift-off resist topped with 1 μm of imaging resist to define the resistor area. Next, an SiO_2 insulator layer is deposited by electron cyclotron resonance plasma-enhanced chemical vapor deposition (ECR-PECVD). Vias into the insulator over junctions and resistors are etched using CHF_3. After this, Nb is deposited by dc sputtering followed by definition of the wiring layer by RIE as for the base electrode. The last step is deposition by dc sputtering and lift-off of resistors for filters and contact pads.

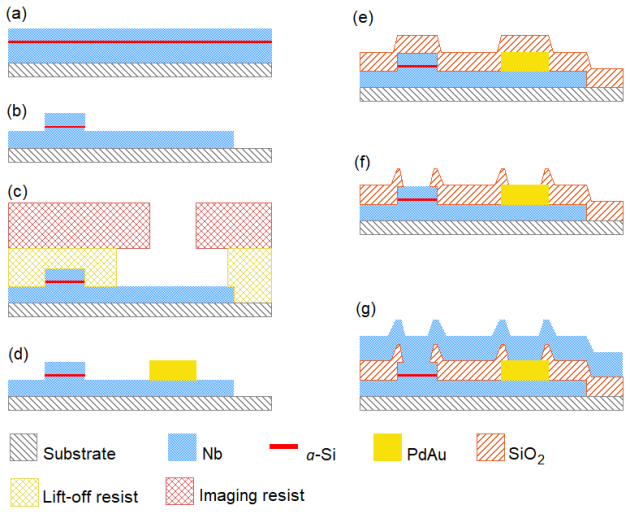

Fig. 2. Fabrication steps. (a) Deposition of trilayer Nb/a-Si/Nb. (b) RIE definition of junctions followed by RIE definition of base electrode. (c) Photolithography with double layer resist for resistor lift-off. (d) Deposition by e-beam evaporation of resistors followed by lift-off. (e) Deposition of SiO_2 insulator by ECR-PECVD. (f) Via opening by RIE over junctions counter electrode and resistors. (g) Deposition of Nb wiring layer followed by RIE definition. Not shown: lift-off deposition of sheet resistors for low-pass filters and contact pads.

A. Junctions

The junction barrier is sputtered from a 3-inch sputter source. The target is phosphorous-doped silicon to allow for dc sputtering. The power used during sputtering is 100 W, the argon pressure is 4 mTorr, and the rate of deposition is 3.8 nm/min. For the desired $J_c = 0.12$ mA/μm^2, the thickness of the barrier is $\approx$ 4.7 nm. The distance from the source to the substrate is $\approx$ 15 cm. The substrate is rotated during deposition, resulting in a radial thickness profile that is 4.6% thinner at the edge compared to the center [9]. Because the critical current density increases exponentially with decreasing barrier thickness, the J_c is $\approx$ 40 % higher at the wafer edge [12]. The circuits were fabricated on 1 cm $\times$ 1 cm chips, and the junction uniformity across this area was sufficient to achieve the desired input bias QLRs. The I_c was reduced from

the typical $\sim$ 10 mA to 3 mA to obtain a wide enough QLR for dc bias of $\sim$ 1 mA without needing higher currents. The target characteristic junction frequency f_c for qubit control was 9 GHz, which determined the value of the shunting resistors R_s to be 6 mΩ. The fabricated value of I_c at 4 K was 3.05 mA and of R_s was 6.9 mΩ, giving f_c = 10.2 GHz.

B. Resistors

Our standard fabrication process for planar resistors consists of a PdAu alloy (53.5 % Pd by weight), sputtered over the patterned wiring layer and defined by a lift-off process. The thickness of the films is 135 nm and the sheet resistance is 2 $\Omega/\square$. Unfortunately, this process configuration cannot be used to achieve acceptable shunt resistor yields with our *a*-Si JAWS design for the following reasons: 1) target resistor values of $O(10$ m$\Omega)$ are too small and 2) contact resistances of the sheet resistor process are too large and too variable compared to the target resistance. To avoid these issues, we developed a process for fabricating cylindrical vertical resistors, solving the contact resistance problem by depositing the resistors over a flat Nb surface that can be well cleaned by an argon plasma before the PdAu deposition and by having a larger contact area as compared to depositing the resistors over a near vertical Nb edge after the wiring definition by RIE for the old process. These vertical resistors provide a small footprint solution suitable for making compact JAWS circuits with more than 4000 overdamped junctions in series and embedded in a 50 Ω coplanar waveguide (CPW). Fig. 3 shows the layout of the whole chip with JAWS circuits and a close-up of the central conductor of the CPW containing the array of shunted junctions. The development of this stud resistor process provides NIST with increased design/fabrication capability for optimizing JAWS and other mixed-signal and digital superconducting circuits for new applications.

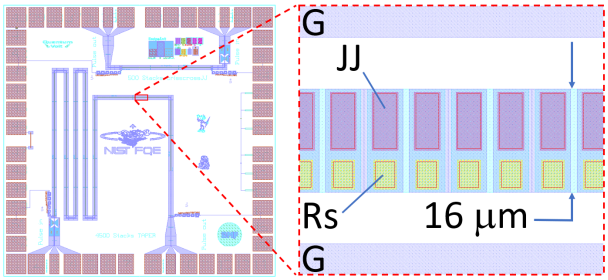

Fig. 3. (Left) Layout of the chip with 2 JAWS circuits; the top array has 500 junctions and the bottom array has 4650 junctions. (Right) Close-up of central region of the coplanar waveguide of the longer array, showing the two ground traces (G) and the signal trace containing the junctions (JJ) and shunt resistors (Rs).

An important consideration is the possibility that, due to the proximity effect, our Nb/PdAu-resistor/Nb stack behaves as a superconducting short (SNS junction) rather than a resistor if the PdAu thickness is insufficient or if the temperature T is low enough. The important length scale in the dirty limit for penetration of superconductivity into the PdAu is given by the normal metal coherence length,

$$\xi_n = \left(\frac{\hbar D}{2\pi k_B T}\right)^{1/2}, \quad (1)$$

and is inversely proportional to $\sqrt{T}$, where $\hbar$ is the reduced Planck constant, k_B is the Boltzmann constant, and D is the diffusion constant for the normal metal [13].

To minimize circuit topography and avoid the addition of steps to our process, we made the thickness of the resistors approximately equal to the typical thickness of the counter electrode plus the amount of overetch into the base electrode. The final thickness was 230 nm and the nominal area 17.5 μm^2. We have measured the resistors at different temperatures down to 20 mK, as seen in Fig. 4. Near 4 K, the behavior is linear for the whole current range. Already at 1.8 K a small nonlinear region is evident near zero current, where the resistance drops by $\approx 3\%$. At 0.7 K and lower temperatures a supercurrent is evident with increasing I_c as T decreases. The maximum I_c, at 20 mK, is < 300 μA. This unintentional junction would effectively form a SQUID loop for $T < 0.7$ K (see Fig. 2), resulting in possible unwanted behavior such as 1) critical current variation due to magnetic flux penetrating the loop and 2) the generation of extraneous pulses. We plan to investigate stud resistors made of thicker PdAu, and alternative resistive materials, at millikelvin temperatures to mitigate this issue. We have not tested our JAWS waveform synthesizers below 3.0 K.

C. Stacked junctions

Reactive ion etching for junction definition yields junction walls with vertical profiles, as the same RIE process mentioned above can be used to etch both Nb and Si. This enables the fabrication of vertical stacks of junctions by simply etching a multilayer of Nb and Si leading to a substantial increase in circuit density and with each junction in the stack having nearly identical area. The demonstration of a JAWS circuit for qubit control used arrays of single junctions, but to maximize circuit density for scalability, we want to use junction stacks. Such stacks are routinely used at NIST in voltage standards circuits, consisting of arrays of many thousands of self-shunted junctions, needed to obtain voltages desired for standards applications [14]. In the case of Nb/*a*-Si/Nb stacks, as shunting resistors are required as mentioned above, we need to include one with the adequate resistance for each stack. We have fabricated circuits with stacks having two JJs per stack. The same fabrication process described above was used with only two changes: 1) single JJs were replaced by stacks of 2 JJs, reducing the array length by a factor of two, and 2) resistor dimensions were modified to double the nominal resistance value. Resistor thickness was increased to match the slightly thicker stack and the resistor area was decreased to 9.2 μm^2.

Cross-sectional images obtained by focused ion beam scanning electron microscopy (FIB-SEM) are shown in Fig. 5. *I-V* curves with Shapiro steps under microwave irradiation, as seen in Fig. 6, demonstrate QLRs adequate for qubit control. The size of the Shapiro steps indicate the uniformity of the I_c of

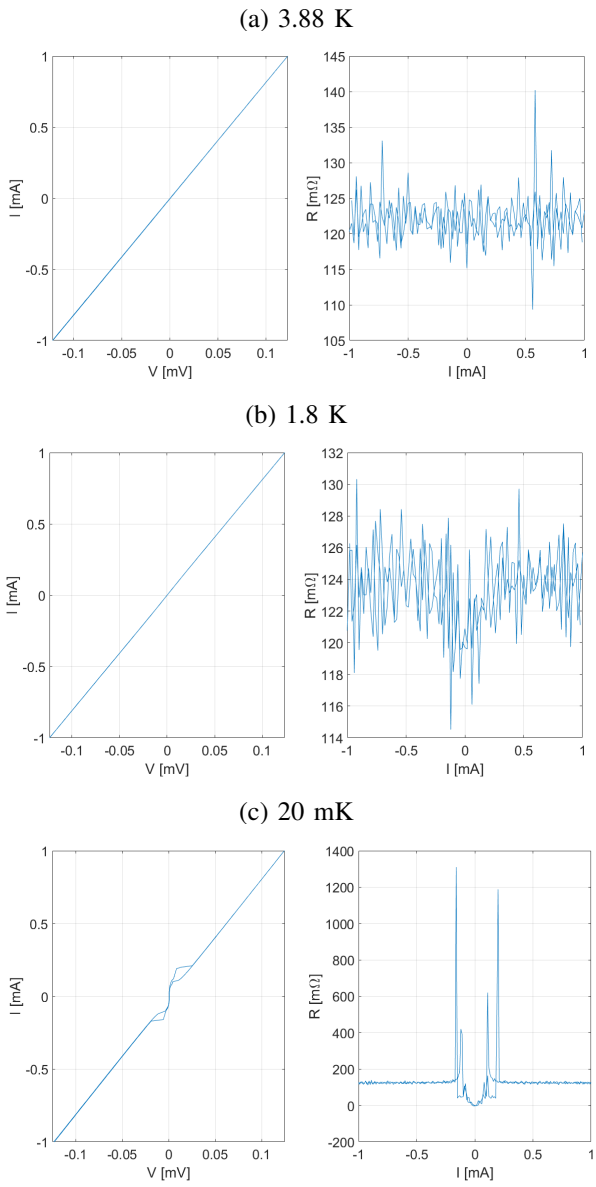

Fig. 4. Measured dc voltage V vs. applied current I for a series array of 20 resistors at three different temperatures. Also shown are resistance R vs. I plots, with R (= dV/dI) derived from the I-V data.

the junctions in the arrays and the capability of using them for stable operation as waveform synthesizers.

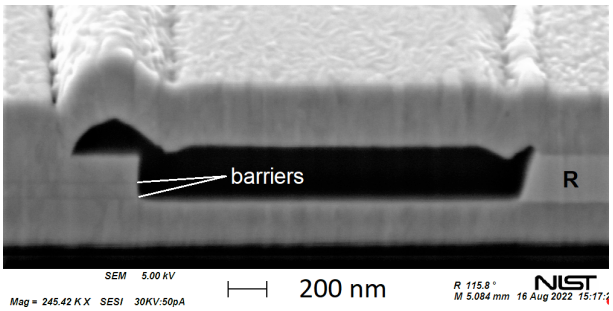

Fig. 5. FIB-SEM cross section of the 2-JJ stack on the left, indicating the a-Si barriers, and the PdAu stud resistor (R) on the right.

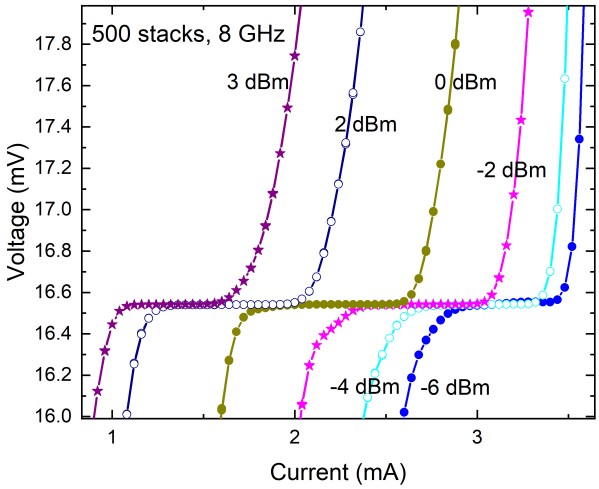

Fig. 6. Measured dc output voltage versus dc bias current for a 500-stack (N = 1000 junctions) series array of Nb/a-Si/Nb junctions cooled to 4 K. The constant-voltage (Shapiro) steps at the value of $h/2e \times N \times f$ are shown at 6 different applied f = 8 GHz microwave powers.

D. Fabricated JAWS circuit

An RF-JAWS circuit with a series array of 4650 Nb/a-Si/Nb individual junctions (no stacks) was fabricated and tested with 2.5 GHz CW input ($f/f_c \sim 0.25$). Fig. 7 shows the first constant voltage Shapiro step measured at different temperatures for this array and for comparison, a similar measurement at 6 GHz was made on a JAWS array with 4500 Nb/$Nb_{0.15}Si_{0.85}$/Nb junctions (1500 stacks of 3-JJs); for this latter circuit, $f_c \sim 20$ GHz and $f/f_c \sim 0.3$. The shift in the step center position and step width with dc bias current (QLR shift) for the circuit with a-Si barriers is 55 μA and 50 μA, respectively, for a 0.64 K change in temperature; in comparison, the same shifts for the circuit with NbSi barriers are 170 μA and 70 μA, respectively, for only a 0.04 K change in temperature. The first step was not observed for the NbSi circuit at 3.47 K and $f = 6$ GHz as the I_c of the array increased from 9.7 mA at 4.11 K to 14 mA. The two circuits shown were measured in the same cryostat, on the same cooldown, using the same measurement setup.

The circuit with a-Si barriers shown here was the same that was mounted at the 3 K stage of a dilution refrigerator (DR) and used as a pulse generator at 2.7 GHz to digitally control a transmon qubit mounted at the 10 mK stage, demonstrating a scalable, stable, repeatable and reproducible solution for qubit control [9]. For this circuit, the target f_c = 9 GHz was an optimization to achieve large QLRs by maximizing f/f_c for $f = 2.7$ GHz while producing narrow junction pulsewidths (high f_c) for good qubit control fidelity [9]. Our design achieved a QLR, measured at 3.1 K and with 2.7 GHz microwave excitation, for dc bias current of 650 μA, with minimal shifts in the QLR with typical observed daily temperature variations of the 3 K stage of the DR (ΔT of $\sim$ 50 mK) and longer term drifts exceeding 200 mK.

III. Conclusion

We have developed a process for fabricating Josephson arbitrary waveform synthesizers using Nb/a-Si/Nb SIS Joseph-

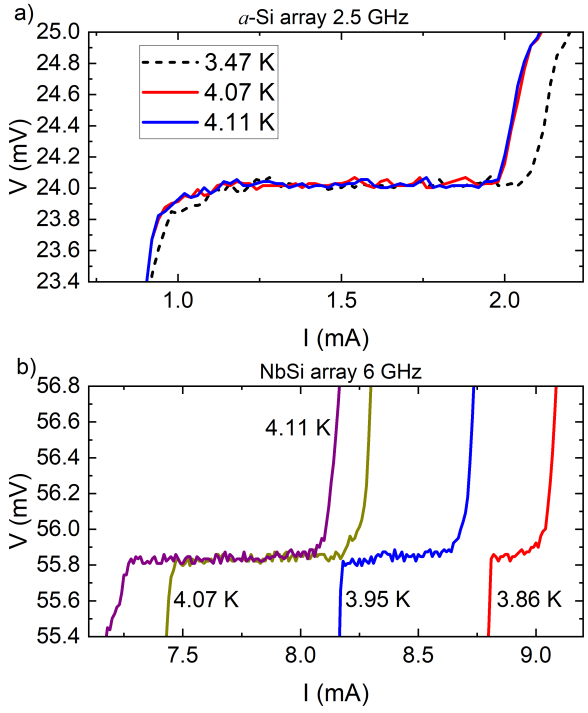

Fig. 7. Measured dc output voltage versus dc bias current with microwave excitation measured at different temperatures for JAWS circuits fabricated with a) $N = 4650$ Nb/a-Si/Nb junctions and b) $N = 4500$ Nb/$Nb_{0.15}Si_{0.85}$/Nb junctions. Fixed microwave power at the generator for a) was 12 dBm, for b) 20 dBm; attenuation from cables and attenuators is -10 dB for 2.5 GHz and -13 dB for 6 GHz. The 4 K measured nominal junction I_c and characteristic frequency for the circuit with a-Si barriers were 3 mA and 9 GHz and for the circuit with NbSi barriers were 10 mA and 20 GHz, respectively. Note the x-axis scale shift between the two plots.

son junctions, replacing the self-shunted, metallically-doped Nb/$Nb_{0.15}Si_{0.85}$/Nb SNS JJs used in our typical ac voltage standard and RF-JAWS circuits. A process for defining PdAu stud shunt resistors was also developed to provide the necessary damping required in our JAWS circuits using these SIS JJs. These JJs with a-Si barriers have critical currents with much smaller temperature dependence for $T \leq 5$ K. A 4650-JJ series array RF-JAWS circuit was fabricated and tested at temperatures between 3 K and 4.1 K, demonstrating a much broader operating temperature range for quantum-locked output compared to a RF-JAWS circuit made of Nb/$Nb_{0.15}Si_{0.85}$/Nb junctions. In other work, this same circuit was mounted at the 3 K stage of a dilution refrigerator and used to digitally control a transmon qubit mounted at the 10 mK stage, demonstrating a scalable, stable, repeatable and reproducible solution for qubit control. JAWS circuits with 2-JJ vertical stacks were also fabricated, allowing a nearly $2\times$ reduction in circuit length for the same number of JJs in the series array. Future work includes development of Nb/a-Si/Nb junctions with thinner barriers and very high critical current densities $J_c > 1$ mA/μm^2 for making very high-speed JAWS and other mixed-signal and digital circuits.

ACKNOWLEDGMENT

The authors thank the Boulder Microfabrication Facility staff for their support in fabrication.

REFERENCES

[1] A. Rüfenacht, N. E. Flowers-Jacobs, and S. P. Benz, "Impact of the latest generation of josephson voltage standards in ac and dc electric metrology," *Metrologia*, vol. 55, no. 5, p. S152, aug 2018. [Online]. Available: https://dx.doi.org/10.1088/1681-7575/aad41a

[2] O. F. Kieler, R. Behr, R. Wendisch, S. Bauer, L. Palafox, and J. Kohlmann, "Towards a 1 V Josephson Arbitrary Waveform Synthesizer," *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 3, pp. 1–5, 2015.

[3] C. A. Donnelly, N. E. Flowers-Jacobs, J. A. Brevik, A. E. Fox, P. D. Dresselhaus, P. F. Hopkins, and S. P. Benz, "1 GHz Waveform Synthesis With Josephson Junction Arrays," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 3, pp. 1–11, 2020.

[4] A. S. Boaventura, J. A. Brevik, D. F. Williams, N. E. Flowers-Jacobs, M. A. Castellanos-Beltran, A. E. Fox, P. F. Hopkins, P. D. Dresselhaus, and S. P. Benz, "Cryogenic Characterization of a Superconductor Quantum-Based Microwave Reference Source for Communications and Quantum Information," *IEEE Transactions on Applied Superconductivity*, vol. 31, no. 9, pp. 1–9, 2021.

[5] N. E. Flowers-Jacobs, J. A. Brevik, A. A. Babenko, A. E. Fox, A. S. Boaventura, P. F. Hopkins, P. D. Dresselhaus, D. F. Williams, and S. P. Benz, "RF Josephson Arbitrary Waveform Synthesizer up to 3 GHz," 2022 Conference on Precision Electromagnetic Measurements (CPEM), Dec. 2022, to be published.

[6] A. A. Babenko, N. E. Flowers-Jacobs, G. Lasser, J. A. Brevik, A. E. Fox, P. D. Dresselhaus, Z. Popović, and S. P. Benz, "A microwave quantum-defined millivolt source," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 12, pp. 5404–5416, 2021.

[7] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Applied Physics Letters*, vol. 68, no. 22, pp. 3171–3173, 1996.

[8] R. McDermott, M. G. Vavilov, B. L. T. Plourde, F. K. Wilhelm, P. J. Liebermann, O. A. Mukhanov, and T. A. Ohki, "Quantum–classical interface based on single flux quantum digital logic," *Quantum Science and Technology*, vol. 3, no. 2, p. 024004, jan 2018. [Online]. Available: https://dx.doi.org/10.1088/2058-9565/aaa3a0

[9] L. Howe, M. A. Castellanos-Beltran, A. J. Sirois, D. Olaya, J. Biesecker, P. D. Dresselhaus, S. P. Benz, and P. F. Hopkins, "Digital Control of a Superconducting Qubit Using a Josephson Pulse Generator at 3 K," *PRX Quantum*, vol. 3, p. 010350, Mar. 2022.

[10] B. Baek, P. D. Dresselhaus, and S. P. Benz, "Co-Sputtered Amorphous Nb_x Si_{1-x} Barriers for Josephson-Junction Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 16, no. 4, pp. 1966–1970, 2006.

[11] P. F. Hopkins, J. A. Brevik, M. Castellanos-Beltran, C. A. Donnelly, N. E. Flowers-Jacobs, A. E. Fox, D. Olaya, P. D. Dresselhaus, and S. P. Benz, "RF Waveform Synthesizers with Quantum-Based Voltage Accuracy for Communications Metrology," *IEEE Trans. Appl. Supercond.*, vol. 29, p. 1301105, Aug. 2019.

[12] D. Olaya, M. Castellanos-Beltran, J. Pulecio, J. Biesecker, S. Khadem, T. Lewitt, P. Hopkins, P. Dresselhaus, and S. Benz, "Planarized Process for Single-Flux-Quantum Circuits With Self-Shunted Nb/Nb_xSi_{1-x}/Nb Josephson Junctions," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 6, pp. 1–8, 2019.

[13] T. V. Duzer and C. W. Turner, *Principles of Superconductive Devices and Circuits*. New York: Elsevier North Holland, 1981.

[14] A. E. Fox, P. D. Dresselhaus, A. Rüfenacht, A. Sanders, and S. P. Benz, "Junction Yield Analysis for 10 V Programmable Josephson Voltage Standard Devices," *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 3, pp. 1–5, 2015.