Demonstrating broadside-coupled coplanar waveguide interconnects to 325 GHz

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***Abstract*— We demonstrate three different broadside-coupled coplanar waveguides to 325 GHz that do not require bump bonds, wire bonds, or direct metal-to-metal bonding. Our design approach used a multimoded distributed theory rather than the conventional $\lambda/4$ approximation. The different interconnects had insertion losses better than 0.7 dB at 63 GHz, 93 GHz, and 120 GHz.**

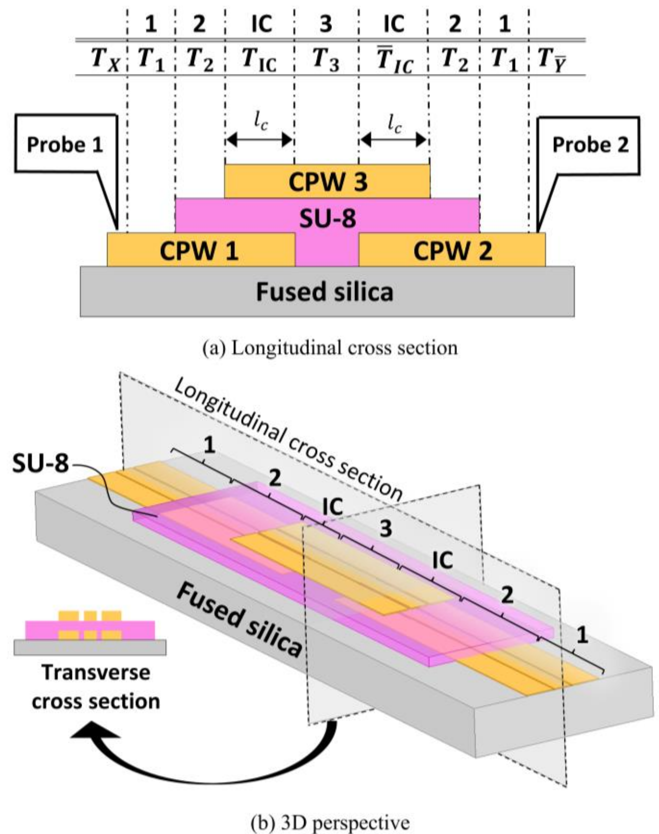
***Index Terms*—Broadside-coupled coplanar waveguide, bumpless, heterogeneous integration, millimeter-wave technology**

I. Introduction

HETEROGENOUS integration enables millimeter-wave (mmWave) and terahertz wireless communication technology by allowing designers to balance cost and performance trade-offs between conventional, cheaper silicon integrated circuits and faster, more expensive compound-semiconductor integrated circuits [1]. Heterogenous integration connects electrodes of integrated circuits from different technologies and allows alternating (ac) and direct (dc) currents to pass between devices. Our motivation was to develop an interconnect that allowed us to connect thermally incompatible technologies with minimal processing.

Looking to the literature, there are several types of contact interconnects, including wire bonds, bump bonds, and metal-to-metal bonds [2], [3], [4], [5], [6], [7] that have different advantages depending on the application. For example, metal-to-metal bonds have the shortest length, minimizing the electrical length of the interconnect that can impact device performance. If there is a break or defect in the electrical contact between the bonded electrodes [8] contact interconnects can fail. In our case, we sought to couple distinct commercial technologies where additional processing could damage the integrated circuits. To solve this problem, we designed an experiment to develop a broadside-coupled coplanar waveguide (CPW) [9], [10], [11], [12], [13], [14] interconnect supported by a distributed theory [15]. Our approach tailors a dielectric layer to optimize the performance for a given CPW geometry.

More generally, contactless interconnects propagate an ac signal between electrodes that are not in direct electrical contact, offering certain advantages, including dc blockage and tunable transmission bands. Contactless interconnects may use lumped or distributed coupling. In the distributed case, transmission lines couple over a length l_c (Fig. 1). While the conventional design approach takes a $\lambda/4$ approximation [16], [17], [18], we used a broadband distributed design approach. We then fabricated, and tested broadside-coupled CPWs. We also performed a sensitivity analysis to understand how the performance of our interconnects vary within realistic fabrication tolerances.



(a) Longitudinal cross section

(b) 3D perspective

Fig. 1 A broadside-coupled coplanar waveguide test structure. (a) A longitudinal cross section schematic (not to scale) that shows the distinct regions and labels all variables in the model. Region IC labels the interconnect. (b) A 3D schematic drawn in perspective (not to scale) that shows the labeled regions and the respective cross sections.

Our experiment tested three different broadside-coupled CPWs, measuring performance with the conventional back-to-back approach. Although the experiment is an idealized test case, we developed the muiltilayer, monolithic fabrication process such that one can tune the dielectric thickness to improve insertion loss and change the coupling length to

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optimize bandwidth. The three different broadside-coupled CPWs had ~0.7 dB of loss at 63 GHz, 93 GHz, and 120 GHz for the 500 µm, 250 µm, and 125 µm coupling lengths respectively. At 325 GHz, the 125 µm length and less than 1.1 dB of insertion loss. Both analytical predictions and simulations agreed with our summarized measurements. To our knowledge, this work is the highest frequency demonstration of broadside-coupled coplanar waveguides (Table I).

TABLE I
Comparison of Broadside-coupled, Contactless Interconnects

Ref.	Passband (GHz)	Insertion Loss (dB)	Type
[9]	2 - 7	NA	CPW ↔ CPW
[19]	2 - 8	≤ 3	CPW ↔ CPW
[20]	4 – 10	NA	MS ↔ CPW
[21]	2.8 – 8.5	≤ 2.1	MS ↔ MS
[22]	50 - 75	3.4	CPW ↔ DWG
[16]	270 - 325	1.7	MS ↔ CPW
This Work	12 – 152 27 – 289 54 – 325	0.7 0.65 0.65	CPW ↔ CPW

* MS: Microstrip. CPW: coplanar waveguide. DWG: Dielectric waveguide

II. Design and Fabrication

Our test structure (Fig. 1) has three coplanar waveguides (CPWs) separated from each other by an SU-8 spacer layer.[1] These CPWs form a series of distinct regions. Between Probe 1 and Probe 2, the structure is nominally symmetric. 'Region 1' is a CPW of length 210 µm with air above and fused silica below. 'Region 2' is a CPW of length 210 µm encapsulated by the 2.5 µm thick SU-8 spacer layer, which can be tailored for a given application. 'Region IC' has the contactless interconnect where CPW 3 is broadside-coupled to either CPW 1 or CPW 2. 'Region 3' is 420 µm long and transmits electrical signals between the two interconnects contained by 'Regions IC'. The length l_c of the interconnect regions determines the center frequency and bandwidth of the interconnect. Our experiment tested three lengths for l_c = 500 µm, 250 µm, or 125 µm. Table II shows the cross-sectional geometries of each region. Each region had a ~50 Ω characteristic impedance. 'Region IC' design minimized insertion loss in the first passband.

TABLE II
Cross-sectional Geometries for Region 1, 2, 3, and IC

Width (µm)	Region 1	Region 2	Region IC	Region 3
Center Conductor	30.0	28.0	30.0	33.0
Gap	3.0	4.0	5.0	3.0
Ground Plane	50.0	50.0	48.0	48.5

Our fabrication process had four monolithic layers: a 665 nm thick SU-8 layer, a 665 nm thick bottom Au conductor layer, a 2.5 µm thick SU-8 layer, and a 500 nm thick top Au layer. Both Au layers include a 10 nm thick Ti adhesion layer. The SU-8 footprint [Fig. 2(a)] used a thinned SU-8 2002 spun at 3000 rpm. The following Au layer used a conventional lift-off resist process and electron beam evaporation to deposit an Au layer of the same thickness in the SU-8 pockets [Fig. 2(b)]. Matching the thickness of the first two layers ensured that the subsequent SU-8 spacer layer was qualitatively flat [Fig. 2(c)]. Next, the 2.5 µm thick SU-8 layer, was fabricated by spinning SU-8 2002 at 2000 rpm. Each of the SU-8 layers used typical exposure and develop processes [23]. We then patterned and deposited the final 500 nm thick Au layer on top of the SU-8, using the same lithography and deposition steps mentioned earlier [Fig. 2(d)]. Image processing tools verified that all features had relative alignments within 1 µm.

III. Measurement

From DC to 110 GHz, we used an Anritsu MS4647A vector network analyzer with 1 mm coaxial extender heads. From 140 to 220 GHz and 220 to 325 GHz we used a 50 GHz PNA-X 5245A with WR-5.1 and WR-3.4 waveguide extenders, respectively. All bands used 50 µm pitch ground-signal-ground

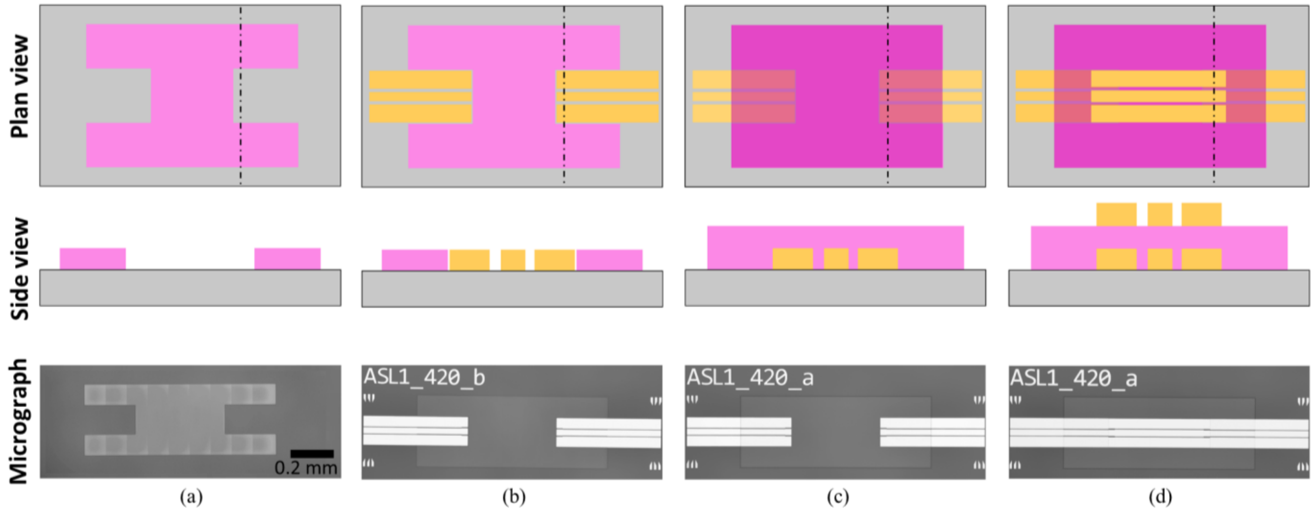

Fig. 2 Fabrication process flow for the interconnect test structures investigated in this work. End view perspectives are cross-sections of the dashed vertical line in the corresponding plan view. Micrographs are optical microscope images of the interconnect test structure at each fabrication step.

[1] Certain commercial equipment, software and/or materials identified here merely specify the experimental procedure. Such identification does not imply recommendation or endorsement, nor that those used are necessarily the best available for the purpose.

(GSG) probes to measure a co-fabricated mTRL calibration [24] and a series resistor calibration [25] of 'Region 1' to correct the data to 50 Ω. This calibration translated the reported measurement reference plane to the boundary between 'Region 1' and 'Region 2' (Fig. 1, bottom).

IV. Interconnect Performance and Discussion

The transfer (T-) matrix model of the full test structure is the matrix product $\boldsymbol{T_X T_1 T_2 T_{IC} T_3 \overline{T}_{IC} T_2 T_1 T_{\overline{Y}}}$ (Fig. 1, bottom). Our on-wafer mTRL calibration removes $\boldsymbol{T_X}$, $\boldsymbol{T_{\overline{Y}}}$, and $\boldsymbol{T_1}$. The corrected T-matrix model is then $\boldsymbol{M_C = T_2 T_{IC} T_3 \overline{T}_{IC} T_2}$, which is set to a reference impedance of 50 Ω. Due to the symmetry of this matrix model, the insertion loss of a single interconnect is approximately the measured insertion loss divided by two. All reported full-wave simulations and measured S-parameters have the T-matrix form of $\boldsymbol{M_C}$ (Fig. 3). The simulations and measurements agreed over the entire measurement bandwidth up to 325 GHz for each test structure.

We measured the S-parameters of three interconnect test structures (Fig. 3 top, middle, and bottom rows, respectively). At low frequencies, the interconnect acts as a dc block because there is no electrical contact between the bottom Au layer and the top Au layer. As frequency increases, the transmission [Fig. 3(a)] through each device increases, reaching a maximum at a frequency f_1. As frequency increases beyond f_1, the transmission of each interconnect decreases until it reaches a minimum at approximately −15 dB. This periodic alternation between transmission maxima at f_n and transmission minima continues, dividing the measurement into a series of transmission bands. The bandwidth of the *n*th transmission band, Δf_n, is defined as 3-dB bandwidth of a single interconnect.

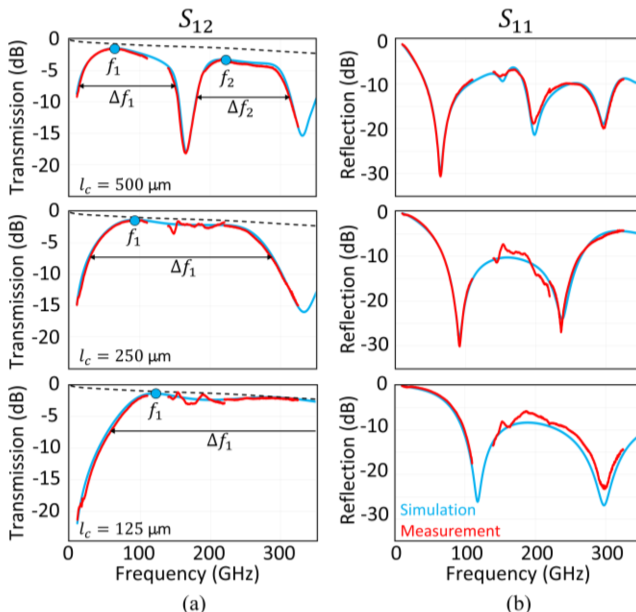

Fig. 3 Simulated and experimentally measured transmission (S_{12}, (a)) and reflection (S_{11}, (b)) coefficients for interconnect test structures with coupling lengths l_c equal to (top row) 500 μm, (middle row) 250 μm, and (bottom row) 125 μm. The maximum simulated transmission in each passband is indicated by the blue circular marker in (a). The dashed lines in (a) represent the net insertion loss of the transmission line regions and therefore set an upper bound on the transmission of the back-to-back configuration.

Table III summarizes the performance of the first transmission band as a function of l_c. Our results agree with the predicted performance over the entire measurement band by analytical theory and simulations with small discrepancies that could be due to the back-to-back approach. De-embedding the interconnect ($\boldsymbol{T_{IC}}$) from the measurement model ($\boldsymbol{M_C}$) should improve agreement between the predicted response and the measured data, which is the subject of future work.

While our test structure is an idealization, its useful because it shows a best-case performance for our motivating a flip-chip application. We can get a sense of design sensitivity of $S_{IC,12}$ by performing a series of full-wave simulations. In our case, we varied four design variables: misalignment along the longitudinal axis (± 3 μm), misalignment along the transverse axis (± 3 μm), rotational misalignment (± 0.5°) and thickness of the SU-8 (± 300 nm). Interestingly, the transmission was relatively insensitive to these variables, changing no more than 0.5 dB, suggesting that broadside-coupled interconnects are robust within realistic fabrication tolerances.

TABLE III
Interconnect Performance

l_c (μm)	f_1 (GHz)	Δf_1 (GHz)		Insertion loss, $-S_{12}(f_n)$ (dB)	
		Here	Ref. [15]	Here	Ref. [15]
500	63	140	135	0.7	0.7
250	93	262	273	0.65	0.5
125	120	> 250	546	0.65	0.4

* S-parameters from this work are divided by 2 because they were measured in a back-to-back configuration.

V. Conclusion

This work tests a distributed design for broadside-coupled CPWs that transmit ac signals with low insertion loss over a broad bandwidth up to 325 GHz. Our best-case experiment demonstrates three different distributed contactless interconnects to 325 GHz, measuring a minimum insertion loss of approximately 0.7 dB at 63 GHz, 93 GHz, and 120 GHz. Future work will use these interconnects to connect integrated circuits that do not have compatible technologies or cannot tolerate extensive processing. Extending our result to a scenario where one bonds a chip ($\epsilon = 10$) onto a carrier ($\epsilon = 3.82$), one can achieve comparable insertion loss and bandwidth by only changing the gap width in 'Region IC' from 5 μm to 12 μm for a chip-to-chip separation of 5 μm. More broadly, the broadside-coupled CPW interconnects shown here could reduce the total number of contact bonding sites and minimize the points of failure, providing increased yield at lower cost.

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