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Quasi-continuous dc voltage standard using sinusoidal and pulse-driven Josephson junction arrays

Dimitrios Georgakopoulos[1,*], **Ilya Budovsky**[1] **and Samuel P Benz**[2]

[1] National Measurement Institute, Australia, West Lindfield, New South Wales, Australia
[2] National Institute of Standards and Technology, Boulder, CO, United States of America

E-mail: dimitrios.georgakopoulos@measurement.gov.au

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Abstract

Josephson voltage standards (JVSs) provide a primary realization of the volt, the unit of electromotive force. They generate direct current (dc) voltages up to 10 V and show agreement better than 1 nV V^{-1} at 10 V. For JVSs based on Josephson junction arrays (JJAs) that are driven by sinusoidal radiofrequency (RF) power, commonly referred to as continuous wave-driven JJAs (CWD JJAs), the minimum voltage that can be generated is limited to the voltage across one Josephson junction (JJ) for practical devices. To achieve this resolution, they may require a perfect JJA chip. JVSs based on a pulse-driven (PD) JJA require high performance electronics (i.e. high bandwidth, low distortion and jitter, pulse shaping filters and large memory) to achieve their minimum and maximum voltage. We have combined two CWD JJAs and two PD JJAs driven by two microwave inputs to one chip to generate quasi-continuous dc voltages up to the sum of the full-scale voltages of both JJAs that are robust to the imperfections of the JJs and have relaxed requirements on the RF electronics driving the JJA, compared to the existing CWD JVSs and PD JVSs, respectively. By use of the JJA chip at the National Measurement Institute Australia, we demonstrate its feasibility to generate voltages up to 1 V. Preliminary evaluation of the system shows that the voltage uncertainty can be 11 nV ($k = 2$) or better and the theoretical resolution is better than 1 nV from 0 V to 1 V. The main requirement is that all the JJs must have quantum locking ranges with respect to the power and frequency of the RF bias and for the PD JJAs to have a constant voltage over a range of dc bias current. Although this development is not a replacement for existing state-of-the-art JVSs, we anticipate that it will be an alternative fit-for-purpose solution for metrological applications under non-ideal operating conditions or when the components of the state-of-the-art solutions are not available.

Keywords: Josephson arbitrary waveform synthesizer, Josephson junction, Josephson standards, programmable Josephson voltage standard, quantum electrical standards, voltage generation

(Some figures may appear in colour only in the online journal)

1. Introduction

A Josephson voltage standard (JVS) utilizes the accuracy of the ac Josephson effect to produce voltages that are calculable from first principles [1]. At direct current (dc), JVS systems show agreement better than 1 nV V^{-1} at 10 V [2, 3]. Modern JVSs are based on superconductor-normal metal-superconductor [4–6] Josephson junction arrays (JJAs). For dc voltages, the JJA is driven by either continuous-wave (CW) radiofrequency (RF) irradiation or by a suitable train of RF pulses.

The CW-driven (CWD) RF biased JJAs are employed in the so-called programmable Josephson voltage standard (PJVS)

* Author to whom any correspondence should be addressed.

to produce either selectable, stable dc voltages or step-wise approximated ac voltages up to 10 V dc or peak ac (see for example [7]). PJVSs contain a number of sub-JJAs, with each sub-JJA containing a number of Josephson junctions (JJs). The number of the JJs per sub-JJA is chosen in such a way to produce a number of predetermined voltages [2, 6, 8–10]. For practical devices, the minimum voltage that a CWD JJAs can generate is limited to the voltage across one junction, typically 5 μV–155 μV, depending on the RF bias frequency. Some existing standards based on a CWD JJA can produce quasi-continuous voltages for most, but not necessarily the whole, of the voltage range, even in the presence of non-ideal junctions, by adjusting the frequency of the RF bias. For example, a JJ designed to operate at 15 GHz produces a voltage of about 31 μV. To produce a voltage of 1 μV, the frequency must be changed to 0.484 GHz, and to produce 10 nV, the frequency must be changed to 0.00483 GHz. These frequencies are not covered by existing chip technologies, and the design of JJAs covering three orders of magnitude in frequency is a formidable task. If the JJAs have missing junctions or a non-flat first quantum step, then the chip may be of limited use in practical applications or may not be usable at all, depending on its specific circuit configuration and application.

In pulse-driven (PD) JJA based standards, a JJA is biased by a suitable pattern of RF pulses to produce either dc voltages or ac waveforms of almost arbitrary shape [11] (typically referred to as Josephson arbitrary waveform synthesizer, JAWS). Standards based on PD JJAs can produce rms voltages up to 4 V [12]. They are mainly used for the generation of ac waveforms in a number of applications [13–18], and they have been proposed for use in the generation of small dc voltages [19]. However, for any specific voltage range, there is a trade-off between the repetition frequency of the pattern of pulses, the length of the pattern of pulses and the number of junctions in the JJA. At low voltages, say less than 1 μV, they require long pulse patterns (with code length of several megabits) and therefore pattern generators with large memory and high-speed interfaces (hundreds of megabits per second) [19], particularly when used in real-time applications (i.e. applications with a feedback loop running at a few kilohertz). Alternatively, small voltages can be produced by reducing the repetition frequency, in which case pulse shaping filters may be required [20]. Commercial state-of-the-art pattern generators have these capabilities, but they are expensive and may not be justified for this sort of application. Higher voltages (greater than 0.2 V) require a large number of junctions (greater than 20 000) and a fast repetition frequency (15 GHz). At higher voltages, say 0.25 V, the density of the RF pulse pattern increases, causing a number of restrictions on the RF drive electronics (see for example [21]).

Another approach to generate dc voltages with low uncertainty that is based on the use of two PJVS chips having two different RF drives was proposed in [22] and implemented in [23–26]. This approach can produce quasi-continuous voltages up to 10 V and is effective even in systems having a few imperfect junctions per PJVS chip [26].

In this work we use a different approach, similar to [22], but instead of using two different PJVS chips, we use one chip containing JJAs with some of them operated as CWD and some as PD to produce quasi-continuous voltages up to the full scale of the chip without requiring state-of-the-art electronics. The outputs of the CWD JJAs and PD JJAs are combined in such a way as to generate quasi-continuous voltages with nanovolt resolution even in the presence of missing JJs. Furthermore, the requirements for the RF bias are relaxed compared to PD JJAs working at their full output voltage. The main requirement is that the JJs in both the PD and CWD arrays must have quantum locking ranges with respect to both RF bias power and frequency, and that the PD JJA must have a quantum locking range with respect to RF pulse amplitude.

It is noted that Behr *et al* [27] used a PJVS and PD JJAs to generate pure ac waveforms, which is similar in some respects but has significant differences with the approach presented in this paper. In [27], the PJVS chip must have a number of operational CWD JJAs to produce a stepwise approximated waveform. The PD JJAs are operated at high pulse densities, require long patterns of pulses (32 megabits), and the operation of the system requires optimising nine parameters. In this work, the required number of CWD JJAs and the PD JJAs driving electronics requirements are relaxed (section 2), and the system operation requires fewer parameters to optimise (five instead of nine). The work presented in this paper is a further development of [22] and could be considered a variation of [27], and its main purpose is to provide an alternative fit-for-purpose solution for metrological applications in non-ideal operating conditions or when state-of-the-art solutions are not available. It is not intended to replace existing JVSs. In this paper, we describe the principle of operation and the implementation of the system, present measured results that characterize its performance and provide an estimate of the relevant measurement uncertainties.

2. System operation

2.1. Basic principle of operation

The CWD and PD JJA voltage standard consists of N CWD JJAs and one PD JJA (figure 1). The CWD JJAs require one current bias source for each JJA and one CW RF synthesizer for all the JJAs of the chip. The PD JJA requires a ternary pattern generator that produces the required pattern of pulses.

The output voltage of the CWD JJAs is given by:

$$V_{\mathrm{CWD}} = \frac{1}{K_J} f_1 \sum_{i=1}^{N} c_i n_i, \tag{1}$$

where, K_J is the Josephson constant 483597.8484 GHz V^{-1}, f_1 is the bias frequency of the CWD JJAs, n_i is the number of junctions of the i-th JJA and c_i is the quantum step number of the i-th JJA (–1, 0, or +1). The parameters n_i and c_i can

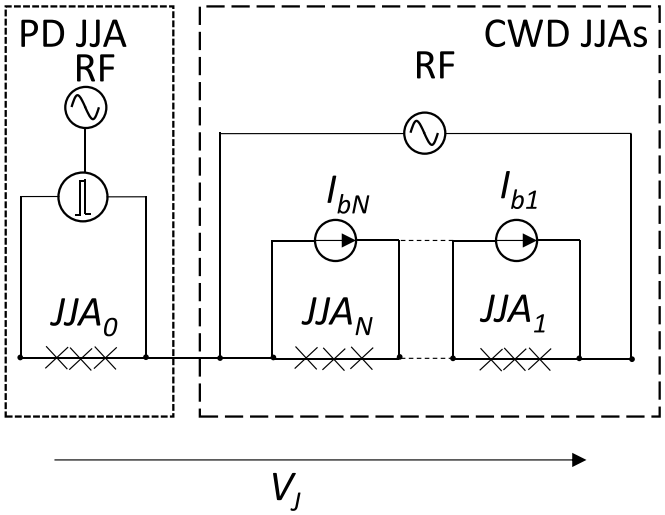


Figure 1. Basic schematic diagram of the CW-driven and pulse-driven JJAs voltage standard.

take only integer values, whereas f_1 can be any real value in a specified frequency range (which depends on the JJA being used), within the resolution of the RF synthesizer (typically 1 Hz or lower).

The output voltage of the PD JJA is:

$$V_{\mathrm{PD}} = \frac{1}{K_J} f_2 np, \tag{2}$$

where f_2 is the repetition frequency of the pattern generator (which depends on the JJA being used and the RF electronics driving the JJA), n is the number of junctions of the PD JJA and p is the average density of pulses (p <1). For small voltages the value of p decreases, so the memory requirements of the pattern generator increase. As in the case of the CWD JJAs, f_2 can take any real value in a specified frequency range within the resolution of the RF synthesizer, p is a rational number and n can take only integer values.

The combined output voltage of the CWD and the PD JJAs is:

$$V_J = V_{\mathrm{CWD}} + V_{\mathrm{PD}}. \tag{3}$$

The value of V_J can be adjusted by $2N+4$ parameters, $N+3$ of which can be adjusted during system operation, giving a large number of combinations to produce quasi-continuous voltages in the range from 0 V up to the sum of the maximum voltages that the CWD JJAs and the PD JJAs can generate.

To achieve quasi-continuous voltages over the whole voltage range, the voltage range is separated into a number of suitable subranges. For a concrete example, with reference to figure 1, consider the following scenario:

- the CWD JJAs consists of only one CWD JJA of N_1 junctions and its frequency can vary by an amount Δf_1 from nominal; and
- the PD JJAs have only one JJA with n junctions and its repetition frequency can vary by Δf_2 from nominal.

Table 1. Example of voltage subranges of the V_J.

Minimum voltage	Maximum voltage
$0V(V_{\mathrm{CWD}} = -V_{\mathrm{PD}})$	$N_1 \frac{\Delta f_1}{K_J} + pn \frac{\Delta f_2}{K_J}$
$N_1 \frac{\Delta f_1}{K_J} + pn \frac{\Delta f_2}{K_J}$	V_{PD}
V_{PD}	$V_{\mathrm{CWD}} - V_{\mathrm{PD}}$
$V_{\mathrm{CWD}} - V_{\mathrm{PD}}$	$V_{\mathrm{CWD}} + V_{\mathrm{PD}}$

The positive voltage range can then be separated into the subranges in table 1. The negative voltage range can be separated into subranges likewise.

The larger the overlap between the maximum and minimum voltages within successive voltage subranges, the more robust to non-ideal junctions the output voltage of the system is. The voltage resolution is primarily determined by the RF source's frequency resolution. For typical implementations, sub-nanovolt resolution can be achieved with commercial RF synthesizers with a frequency resolution as low as 1 Hz.

Zero output voltage is generated by setting the CWD JJAs and the PD JJAs to produce voltages of equal absolute value and opposite polarity. This allows the PD JJA voltage to have high p values, typically 0.1–0.25, so that the memory requirements are minimal. For example, for a repetition frequency of 15.1124 GHz and a JJA with 25 600 junctions, a pattern with $p = 0.25$ can produce 0.2 V. This pattern of pulses only requires a pattern of 16 bits compared to a megabit-long pattern required by a single PD JJA. Also, this setting for the generation of zero voltage is beneficial to evaluate the quantum locking range during system operation so as to confirm that the JJAs are producing quantum-based voltages.

To demonstrate the resilience of the suggested method to non-ideal JJs that present a superconducting short in the presence of RF and dc bias, consider the JJA chip described in [28]. It has four JJAs and microwave circuit designs, with each JJA having 12 800 JJs. This chip has two RF bias launches, so it can be configured to have two CWD JJAs and one PD JJA. Each CWD JJA can generate about 0.397 V at 15 GHz. Assuming that the PD JJAs can generate 0.25 V, then the maximum voltage at the output of the series-connected JJAs is 1.044 V. If the frequency of the RF-bias can be changed by 1 GHz, then the system will be able to produce the same maximum voltage with the same voltage resolution over the whole voltage range if the two CWD JJAs have no more than 536 missing junctions in total. If more junctions of the CWD JJAs are missing, then the maximum voltage is reduced, but it can still produce quasi-continuous voltages up to the maximum voltage.

2.2. System description

Figure 2 shows the block diagram of the experimental realization of the basic schematic diagram in figure 1. It includes two

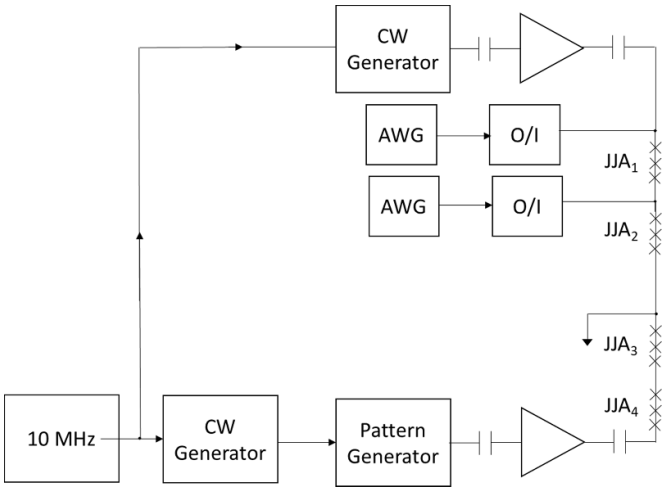


Figure 2. Block diagram of the CW and pulse-driven JJAs voltage standard.

CW RF synthesizers (Hewlett Packard 83 640 A[3]), a ternary pattern generator (Sympuls Bipolar Pattern Generator 30G-TER), two battery powered broadband RF amplifiers (CENTELLAX UA0L65VM), two arbitrary waveforms generators (AWGs, Agilent 33 250 A), two optically isolated amplifiers (O/I, QPRI ISO8), and one chip having four National Institute of Standards and Technology (NIST) JJAs and microwave circuit designs [28]. The JJAs are connected with superconducting interconnects. Two JJAs (JJA_1 and JJA_2, each having 12 800 JJs) are configured as CWD JJAs, whereas the other two JJAs (JJA_3 and JJA_4) are configured as one PD JJA having 25 600 JJs. The combined output of the PD JJAs generate up to 0.25 V. This is not a limitation of the JJAs chip, but a limitation of the combination of the pattern generator and the RF amplifiers that drive the JJAs.

With reference to table 1 for this JJA arrangement, the system can generate 0 V by operating the CWD JJAs at 7.5562 GHz and the PD JJAs at 15.1124 GHz. Dc voltages from—1 mV to + 1 mV are generated by changing the frequency of the PD JJAs from 15.0368 GHz to 15.1876 GHz with $p = 0.25$. For voltages from 1 mV to 0.2 V, the PD JJA is only used and is operated at 15.1124 GHz, with p from 0.00125 to 0.25, by adjusting the frequency appropriately in the range 15.03684 GHz to 15.1876 GHz, when it is needed. Voltages greater than 0.2 V up to 0.597 V are generated by combining the CWD JJAs operated at 15 GHz to generate 0.397 V and the PD JJAs to produce the corresponding negative or positive voltage. Similarly, voltages greater than 0.597 V to 1 V are generated by combining the two CWD JJAs (operated at 15 GHz) and the PD JJAs. In this arrangement, the maximum memory needed for the pattern generator is less than 4 kilobytes, significantly less than the hundreds of megabytes needed to produce voltages in the same voltage range using only PD JJAs.

A combination of two cascaded dc blocks (inner-conductor type) and attenuators is connected at the input and the output of each RF amplifier (shown as capacitors in figure 2) act as pulse-shaping filters. Since the density of the pattern of pulses is relatively low for the voltage range of interest, their function is not as critical as in the AC voltage applications (as for example in [18]). Statistically equivalent results to those obtained in section 3 were obtained using one cascade of dc block and attenuators. Both CW synthesizers are referenced to a 10 MHz signal derived from a caesium beam atomic clock.

The choice of the JJA chip in our setup was due to its availability in our laboratory. The chip described in [28] can be used as two PD JJAs and can be combined with other PJVS chips (such as those in [9, 10]), not necessarily in the same cryostat, to produce quasi-continuous voltages up to 10 V. When the PD JJAs and the CWD JJAs are in the same cryostat, it is preferable to connect the PD and the CWD JJAs using a superconducting wire. When the PD JJAs and the CWD JJAs are connected with a normal wire, e.g. when the JJAs are not in the same cryostat, special precautions (e.g. better isolation of the biasing electronics, grounding considerations, and screening of the measurement system) should be taken to avoid error voltages, for example due to noise.

3. System evaluation

The basic principle of our approach is based on summing the outputs of the CWD and PD JJAs. The methods for the evaluation of the CWD JJAs are well known (see for example [2]). The evaluation of our combined system was performed in two stages. Firstly, the PD JJAs were evaluated for their performance at dc, and secondly, the PD and CWD JJAs were evaluated together for the generation of dc voltages up to 1 V.

3.1. Evaluation of the PD JJAs

The evaluation of a PD JJA must show that its output is unaffected by [29]: (a) the specific JJA used; (b) the biasing electronics (pattern generator, RF amplifiers, dc blocks and connecting cables); (c) the RF power applied to the JJA; and, (d) the repetition frequency and RF pattern of pulses. Criteria (1) and (2) have been demonstrated elsewhere for ac operation [18, 29].

To demonstrate that the PD JJAs fulfill criterion (3), we measured the current–voltage characteristics of the PD JJAs at 0.2 V (used to realise 0 V in table 1). We generated 0.2 V at a repetition frequency of 15.1124 GHz for a number of currents. In particular, we changed the dc bias current supplied to the PD JJAs through the AWG-O/I combination and measured the output voltage of the PD JJAs (shown in figure 2) with a Keysight 3458 A multimeter (K3458A). The number of power-line cycles of the K3458A was set to 20. We repeated this measurement for different RF power settings of this pattern of pulses. Figure 3 shows the difference between the measured voltages and nominal. Each data point in figure 3 is an average of 10 readings. These settings were used in all the experiments

[3] Commercial instruments are identified in this paper only to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Measurement Institute, Australia or the National Institute of Standards and Technology, nor does it imply that the equipment identified is necessarily the best for the purpose.

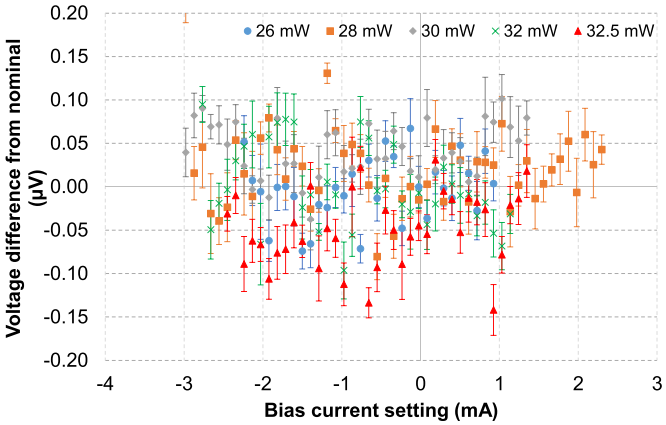


Figure 3. Difference from the nominal of the voltage measured using the K3458A versus dc bias current for different RF power biases. The error bars show the type-A uncertainty ($k = 1$) of the measurement.

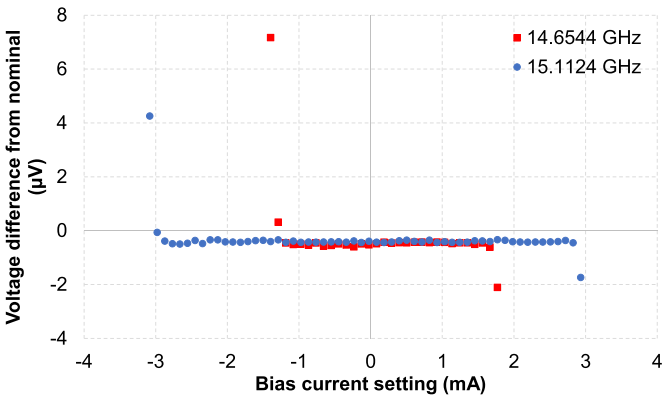


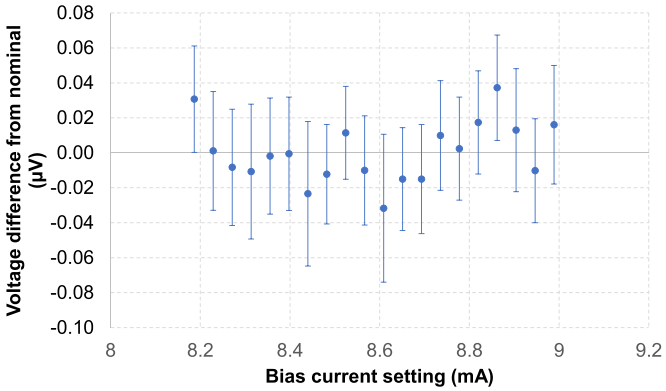
Figure 4. PD JJA voltage difference from nominal, measured with a K3458A, versus dc bias current for different pulse patterns and repetition frequencies.

reported in this Section, except as stated otherwise. Figure 3 shows that the voltage is unaffected by the specific RF power used (all the data points agree within the Type A uncertainty of the measurement and taking into account the measurement transfer capability of the K3458A), whereas the bias current range of the step is affected by the RF power, indicating that the quantum locking range for dc bias is different when the RF power is changed.

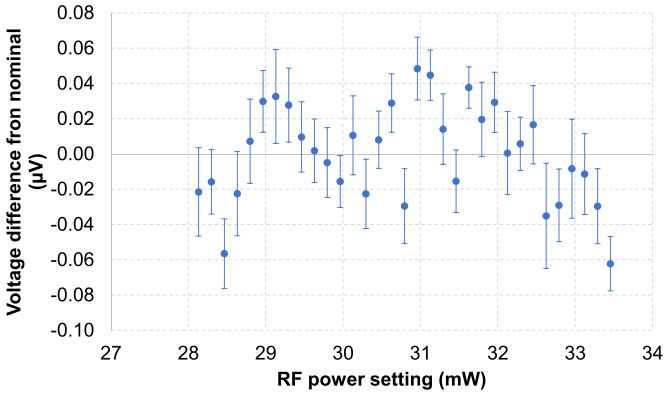
To demonstrate that the PD JJAs fulfill criterion (4), we generated two voltages of 0.2 V using different patterns of pulses and repetition frequencies (14.6544 GHz and 15.1124 GHz). We then changed the dc bias current supplied through the AWG-O/I combination and measured the output of the two PD JJAs (shown in figure 2) with the K3458A. Figure 4 shows the difference of the measured voltage from nominal. The pattern of pulses and the repetition frequency do affect the bias current range of the voltage step but not the voltage of the step.

3.2. *Evaluation of the combined PD and CWD JJAs*

Having established that the PD JJAs have quantum locking ranges for RF power, dc bias, and pulse repetition frequency



(a)



(b)

Figure 5. (a) Current–voltage characteristic of the CWD JJA and (b) the RF power-voltage characteristic of the PD JJA. The error bars show the type-A uncertainty ($k = 1$) of a series of five measurements.

and for different pulse patterns, the basic experiments to demonstrate the feasibility of the proposed system were:

(a) comparison of the PD with the CWD JJAs at the same voltage that defines the lower part of the range in table 1 (i.e. 0.2 V); and,
(b) comparison of the two CWD JJAs at their maximum voltage (0.397 V), which is also used to define the various parts of the voltage scale in table 1.

Firstly, we compared the PD JJAs with the CWD JJAs at 0.2 V. The RF bias frequency of the CWD JJAs was 7.5562 GHz and for the PD JJAs 15.1124 GHz. For this experiment we measured the current–voltage characteristic of the CWD JJA and the RF power-voltage response of the PD JJA for both positive and negative voltages. The output voltage was measured using a K3458A digital multimeter. Figures 5(a) and (b) show the results for only the positive voltage (difference between the measured and the nominal voltage).

Each of the data points in figure 5 shows the weighted average of five current–voltage and RF power-voltage scans. For each scan, each voltage measurement was the average of 10 readings of the 3458 A. From the data in figure 5, we calculated the corresponding slopes using a weighted least- squares fit. The slope for the CWD JJA

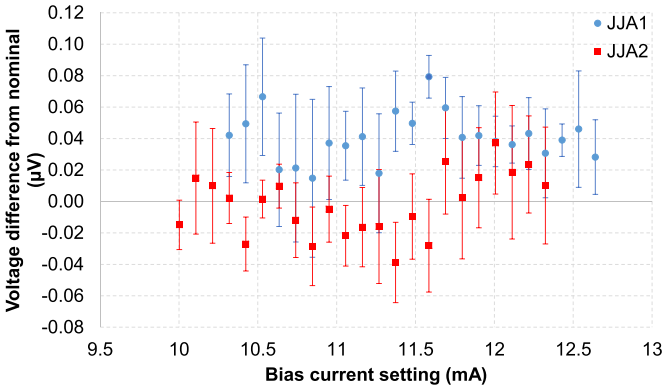


Figure 6. Current–voltage characteristic of the CWD JJAs. The error bars show the type-A uncertainty ($k = 1$) of the measurement.

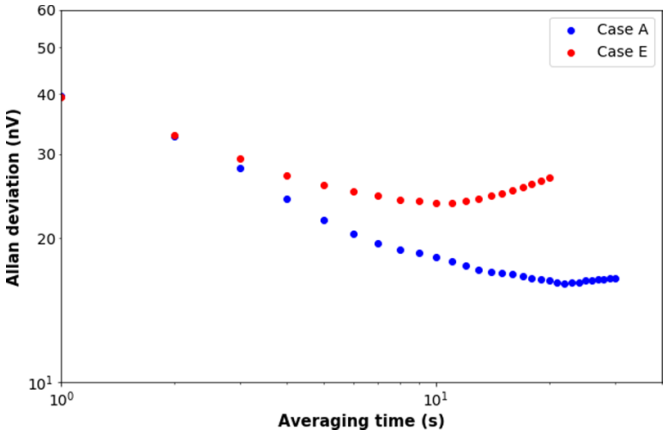


Figure 7. Allan deviation for 0 V. See text for details.

was + 0.008 μV mA^{-1} (figure 5(a)) and for the PD JJA—0.002 μV mW^{-1} (figure 5(b)). For the negative voltages, the slope for the CWD JJA was + 0.005 μV mA^{-1} and for the PD JJA—0.004 μV mW^{-1}. The corresponding uncertainties for the slopes for the CWD JJA were 0.03 μV mA^{-1} and for the PD JJA 0.003 μV mW^{-1}, respectively.

Then we fixed the bias current of the CWD JJA and the RF power of the PD JJAs to the middle of the corresponding steps. We then compared the voltages produced by the CWD JJAs and PD JJAs using the measurement sequence forward-reverse-reverse-forward polarity to reduce the effect of the unwanted thermal emfs. The difference between the CWD JJA and the PD JJA was 0.4 nV with a Type A uncertainty of 5 nV ($k = 1.0$), for an average of 10 measurements.

Next, we compared the two CWD JJAs at 0.397 V, the maximum voltage that one CWD JJA, which defines the V_{CWD} value in table 1, can generate. We again measured the current–voltage characteristics of the two CWD JJAs for both positive and negative output voltages. The slope for JJA_1 was 4 nV mA^{-1} with an uncertainty of 7 nV mA^{-1} and −3 nV mA^{-1} for JJA_2 with an uncertainty of 5 nV mA^{-1}. Figure 6 shows the results for the positive voltages. The bias current of the two CWD JJAs was set to the middle of the step and the two JJAs were compared using the forward-reverse-reverse-forward measurement sequence. Their difference was −0.03 nV with a Type-A uncertainty (k =1) of 3 nV, for an average of 20 comparisons.

The noise floor of the system is relatively high for a JVS. To investigate whether the noise floor is due to any particular component in the system, we did a number of comparisons at 0 V, using different configurations. Firstly, we compared the CWD JJAs without connecting the RF power cable to the JJAs and with the O/I amplifier disconnected (A). We then compared them by connecting the RF power cable to the JJAs without applying any RF power to the JJAs and with the O/I amplifier still disconnected (B). Next, we compared the two CWD JJAs with both the RF power line and the O/I amplifier connected but we did not apply any RF power (C). Finally, we applied RF power and zero bias current through the O/I amplifier to the CWD JJAs (D). For completeness, we included the 0 V comparison by setting the CWD JJAs and PD JJAs at 0.2 V in series opposition (E) and the 0 V comparison by setting the CWD JJAs in series opposition (F). Table 2 summarizes the results. Figure 7 shows the Allan deviation of the cases A and E described above.

Table 2. Comparison of the CWD JJAs at 0 V (see text for details).

Voltage generation method	Mean value (nV)	Type A uncertainty ($k = 1.0$) (nV)
A	—0.2	4.8
B	+ 0.9	4.4
C	+ 0.3	4.9
D	+ 0.4	3.3
E	+ 0.4	4.9
F	—0.03	3.0

Table 2 shows that the noise floor of the system in normal operation is not dominated by a specific source, e.g. RF amplifiers or the optical isolation amplifiers. However, the Allan deviation (figure 7) shows that the bias electronics introduce some correlation to the measurement at averaging times greater than 10 s.

In practical measurements, we use the Allan deviation to estimate the best averaging time of the system and then make measurements over time intervals separated by several times the correlation time of the noise process, estimated from its autocorrelation function. In this way, the Type A uncertainty can be reduced to the levels reported in this section. For example, case E of figure 7 gives consistent results with the corresponding 3 nV Type A uncertainty reported above (average of 20 comparisons, with 10 readings per polarity, forward and reverse, in each comparison). Lowering the noise floor of the system is the focus of ongoing efforts at the National Measurement Institute, Australia.

Next, we combined the output of the CWD and PD JJAs to produce a voltage of 1 V. Figure 8 shows the RF power-voltage characteristic at 1 V and figure 9 the Allan deviation when the RF power was adjusted to the middle of the step. The Allan deviation in figure 9 is consistent with the Allan deviation presented in figure 7 and the noise of the 3458 A at 1 V presented in [30].

Finally, to demonstrate that our combined system can measure the gain of digital voltmeters, we measured the gain of

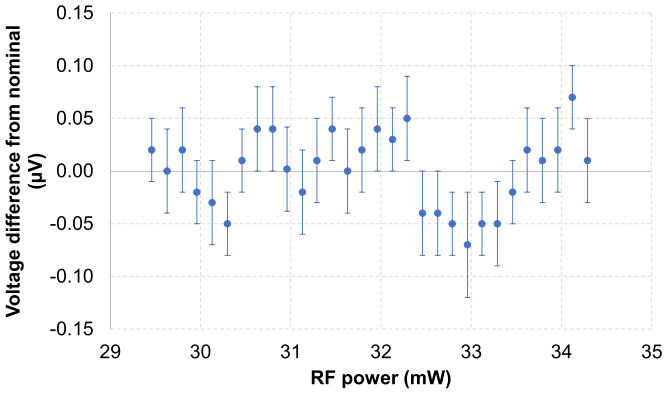


Figure 8. RF power—voltage characteristic of the CWD JJAs. The error bars show the type-A uncertainty ($k = 1$) of the measurement.

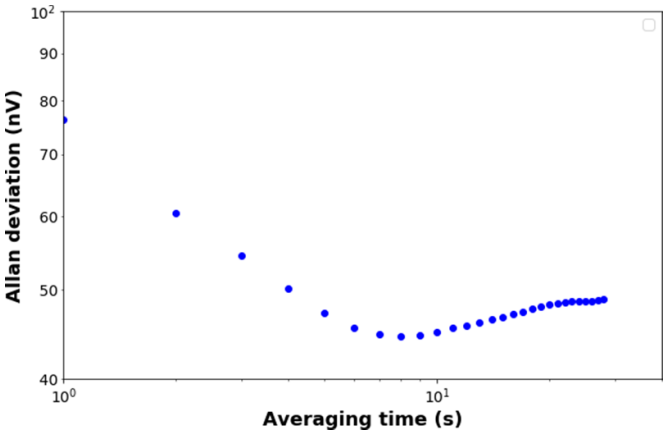


Figure 9. Allan deviation at 1 V.

a 1 mV range of an Agilent 34 420 A nanovoltmeter using both our combined system and the conventional JVS of National Measurement Insitute Australia (NMIA) [31]. For this voltage range of the 34 420 A, the voltage was produced by setting one CWD JJA and the PD JJAs in series opposition at 0.2 V and changing the frequency of the PD JJA. The gain correction of the 34 420 A was measured to be (62.4 ± 17) nV with the conventional JVS and (62.0 ± 23) nV with the combined system. For the gain correction, 10 points (five for each polarity) were used. The reported uncertainties are the total measurement uncertainties ($k = 2$) and contain the standard error of the slope and the standard error of the estimate of the linear fit. The two systems agree well within their uncertainties (E_n ratio of 0.07).

4. Uncertainty budget

The main uncertainty components of the voltage generated by the new system are due to:

(a) Errors in setting the frequency (offset and resolution of the RF source or the frequency measurement equipment if used);
(b) Leakage in the connecting leads (the leakage resistance of the connecting leads allows currents to flow through the finite series resistance of the connecting leads leading to a type B error); and,
(c) Standard deviation of the measurement.

Table 3. Typical uncertainty components.

Component	Type	u_i (nV)
RF source offset	B	0.1
RF source resolution	B	0.04
Leakage	B	1.5
ESDM	A	5
Combined uncertainty		5.3
Expanded uncertainty (k =2.0)		10.6

Table 3 shows typical values of these components. The leakage was measured using the technique described in [32]. As estimated standard deviation of the mean (ESDM) in table 3, we use the ESDM of the comparison of the CWD JJAs.

5. Conclusion

We have developed a voltage standard based on a combination of CWD and PD JJAs that can produce quasi-continuous voltages and is robust to non-ideal JJAs. The approach demonstrated in this paper can be robust to non-ideal JJs (i.e. missing JJs and JJs that have a flat zero quantum step but do not have a flat first step when they are configured as CW). Although the PD JJAs can have missing junctions, they should have quantum locking ranges for pulse power and dc bias current.

Our combined system produced voltages with uncertainties of about 11 nV for a number of different JJA configurations. To achieve its maximum voltage, the PD JJAs are not operated with pulse patterns having a high density of pulses, so the bandwidth and distortion requirements of the RF driving electronics are reduced and pulse shaping filters are not required, compared to PD JJAs operating at high density patterns of pulses. The PD JJAs can produce very low dc voltages (theoretically less than 1 nV, but the lowest voltages are practically limited by noise to less than 10 nV at present) without the need of long pulse patterns, hence the memory requirements of the pattern generators for the PD JJAs are minimal. Also, simple and low computational load algorithms (worst case scenario, three comparisons, one subtraction, five multiplications, and one addition) can be used to generate the voltages, compared to the dual CWD JJAs described in [23]. The last two features make the system suitable for use in the feedback loop of a slow control system (e.g. a sampling rate of some tens of samples per second).

However, the noise floor of our CWD and PD JJAs system is relatively high for a JVS. Further work is required to reduce the noise floor of the system.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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ORCID iD

Dimitrios Georgakopoulos https://orcid.org/0000-0002-5687-7229

References

[1] Jeanneret B and Benz S P 2009 Application of the Josephson effect in electrical metrology *Eur. Phys. J. Spec. Top.* **172** 181–206
[2] Solve S and Stock M 2012 BIPM direct on-site Josephson voltage standards comparisons: 20 years of results *Meas. Sci. Technol.* **23** 124001
[3] Rüfenacht A, Tang Y-H, Solve S, Fox A E, Dresselhaus P D, Burroughs C J, Schwall R E, Chayramy R and Benz S P 2018 Automated direct comparison of two cryocooled 10 volt programmable Josephson voltage standards *Metrologia* **55** S152–73
[4] Benz S P 1995 Superconductor-normal-superconductor junctions for programmable voltage standards *Appl. Phys. Lett.* **76** 2714–6
[5] Kieler O F, Kohlmann J and Müller F 2007 Improved design of SNS Josephson junction series arrays for an ac Josephson voltage standard *Supercond. Sci. Technol.* **20** S318–22
[6] Yamamori H, Yamada T, Sasaki H and Shoji A 2008 A 10 V programmable Josephson voltage standard circuit with a maximum output voltage of 20 V *Supercond. Sci. Technol.* **21** 105007
[7] Tang Y-H, Wachter J, Rüfenacht A, FitzPatrick G J and Benz S P 2015 Application of a 10 V programmable Josephson voltage standard in direct comparison with conventional Josephson voltage standards *IEEE Trans. Instrum. Meas.* **64** 3458–66
[8] Dresselhaus P D, Elsbury M M, Olaya D, Burroughs C J and Benz S P 2011 10 volt programmable Josephson voltage standard circuits using NbSi-barrier junctions *IEEE Trans. Appl. Supercond.* **21** 693–6
[9] Kohlmann J, Müller F, Kieler O, Behr R, Palafox L, Kahmann M and Niemeyer J 2007 Josephson series arrays for programmable 10-V SINIS Josephson voltage standards and for Josephson arbitrary waveform synthesizers based on SNS junctions *IEEE Trans. Appl. Supercond.* **56** 472–5
[10] Wende G *et al* 2003 Josephson voltage standard circuit operation with a pulse tube cooler *IEEE Trans. Appl. Supercond.* **13** 915–8
[11] Benz S P and Hamilton C A 1996 A pulse-driven programmable Josephson voltage standard *Appl. Phys. Lett.* **88** 3171–3
[12] Flowers-Jacobs N E, Rüfenacht A, Fox A E, Waltman S B, Schwall R E, Brevik J A, Dresselhaus P D and Benz S P 2019 Development and applications of a four-volt Josephson arbitrary waveform synthesizer *2019 IEEE Int. Superconductive Electronics Conf. (ISEC)* (*Riverside, CA*) pp 1–2
[13] Lipe E T, Kinard J R, Tang Y-H, Benz S P, Burroughs C J and Dresselhaus P D 2008 Thermal voltage converter calibrations using a quantum ac standard *Metrologia* **45** 275–80
[14] Filipski P S, Boecker M, Benz S P and Burroughs C J 2010 Establishing an ac Josephson voltage standard at NRC *CPEM 2010 Conf. Digest* (*Daejeon, Korea)* vol 2010 pp 22–23
[15] van den Brom H E, Kieler O F O, Bauer S and Houtzager E 2017 Ac-dc calibrations with a pulse-driven ac Josephson voltage standard operated in a small cryostat *IEEE Trans. Appl. Supercond.* **66** 1391–6
[16] Overney F, Flowers-Jacobs N E, Jeanneret B, Rüfenacht A, Fox A E, Underwood J M, Koffman A D and Benz S P 2016 Josephson-based full digital bridge for high-accuracy impedance comparisons *Metrologia* **53** 1045–53
[17] Benz S P, Dresselhaus P D and Burroughs C J 2011 Multitone waveform synthesis with a quantum voltage noise sourse *IEEE Trans. Appl. Supercond.* **21** 681–6
[18] Georgakopoulos D, Budovsky I, Benz S P and Gubler G 2019 Josephson arbitrary waveform synthesizer as a reference standard for the measurement of the phase of harmonics in distorted waveforms *IEEE Trans. Appl. Supercond.* **68** 1927–34
[19] Behr R, Kieler O and Schumacher B 2017 A precision microvolt-synthesizer base on a pulse-driven Josephson voltage standard *IEEE Trans. Appl. Supercond.* **66** 1385–90
[20] Dresselhaus P D 2022 Personal communication
[21] Flowers-Jacobs N E, Waltman S B, Fox A E, Dresselhaus P D and Benz S P 2016 Josephson arbitrary waveform synthesizer with two layers of wilkinson dividers and an FIR filter *IEEE Trans. Appl. Supercond.* **26** 1400307
[22] Chong Y, Kim M S and Kim K T 2006 Fast and almost continuously programmable Josephson voltage standard system with multiple microwave drive *CPEM 2006 Conf. Digest* (*Torino*) pp 382–3
[23] Georgakopoulos D, Budovsky I F, Hagen T, Sasaki H and Yamamori H 2012 Dual RF drive quantum voltage standard with nanovolt resolution based on a closed-loop refrigeration cycle *Meas. Sci. Technol.* **23** 124003
[24] Georgakopoulos D, Budovsky I, Grady S and Hagen T 2013 Quantum calibration system for digital voltmeters at voltages from 10 nV to 10 kV *IEEE Trans. Appl. Supercond.* **62** 1581–6
[25] Li H H, Gao Y and Wang Z M 2014 Microvolt Josephson voltage set-up based on two programmable Josephson arrays *CPEM 2014 Conf. Digest* pp 744–5
[26] Georgakopoulos D 2016 Maximizing the resolution of a dual RF drive programmable Josephson voltage standard *IEEE Trans. Appl. Supercond.* **64** 1503–8
[27] Behr R, Kieler O F O, Schleußner D, Palafox L and Ahlers F—J 2013 Combining Josephson systems for spectrally pure ac waveforms with large amplitudes *IEEE Trans. Instrum. Meas.* **62** 1634–9
[28] Flowers-Jacobs N E, Fox A E, Dresselhaus P D, Schwall R E and Benz S P 2016 Two-volt Josephson arbitrary waveform synthesizer using wilkinson dividers *IEEE Trans. Appl. Supercond.* **26** 1400207
[29] Georgakopoulos D, Budovsky I F and Benz S P 2021 Evaluation of a Josephson arbitrary waveform synthesizer at low voltages for the calibration of lock-in amplifiers *IEEE Trans. Appl. Supercond.* **70** 1502107
[30] Lapuh R, Voljc B and Lindic M 2016 Keysight 3458A noise performance *CPEM 2016 Conf. Digest Ottawa, Canada* pp 1–2
[31] Reymann D, Solve S, Budovsky I and Rigby R 2006 Comparison of the Josephson voltage standard of the NMIA and the BIPM, Rapport BIMP-2006/09
[32] NCLS International 2002 Josephson voltage standard, recommended intrinsic/derived standards practice, RISP-1