RF Josephson Arbitrary Waveform Synthesizer With Integrated Superconducting Diplexers

Akim A. Babenko, *Graduate Student Member, IEEE*, Nathan E. Flowers-Jacobs, *Member, IEEE*, Gregor Lasser, *Member, IEEE*, Justus A. Brevik, *Member, IEEE*, Anna E. Fox, *Senior Member, IEEE*, Paul D. Dresselhaus, Zoya Popović, *Fellow, IEEE*, and Samuel P. Benz, *Fellow, IEEE*

***Abstract*—We present the design and characterization of a broadband RF Josephson arbitrary waveform synthesizer (RF-JAWS) with a series array of 4500 Josephson junctions (JJs) and integrated low-pass/high-pass five-pole superconducting diplexers. The integrated diplexers enable broadband filtering of the feedthrough signal components in the drive-current pulses with decade-wide instantaneous bandwidth. The diplexers have at least 30 GHz passband with less than 0.8 dB insertion loss. The JJ array is driven with a delta-sigma pulse sequence that encodes 10 kHz and 1.005 GHz tones, and generates an open-circuit voltage of 22 mV rms (−26.18 dBm available power assuming a 50 Ω Thevenin equivalent source) at 1.005 GHz—a 25% increase compared to the state of the art. The drive current pulses undergo a three-step equalization to compensate for the linear distortion of the room-temperature electronics, the on-chip diplexers, and the remaining on- and off-chip components. The measured parasitic feedthrough voltages at 1.005 GHz are around −33 dBc, and their effect on the quantum locking ranges (QLRs) is quantified by measurements. The results demonstrated in this article show a significant step toward a broadband, integrated, quantum-based microwave voltage source with useful power above −30 dBm.**

***Index Terms*—Equalizers, Josephson junctions (JJs), pulse measurements, superconducting integrated circuits, superconducting microwave devices.**

I. Introduction

THE RF Josephson arbitrary waveform synthesizer (RF-JAWS) demonstrated over the past several years [1], [2], [3] is being developed as a quantum-based microwave voltage source for absolute power metrology that is currently based on calorimetry [4], [5], [6]. The RF-JAWS is a superconducting IC that can generate voltage waveforms with amplitudes calculable from the magnetic flux quantum $\Phi_0 = h/2e$, where h is the Planck constant and e is the elementary charge. A photo of the chip presented in this article is shown in Fig. 1. This RF-JAWS circuit consists of an array of 4500 Josephson junctions (JJs) connected in series, operating at a temperature of 4 K and embedded in a coplanar waveguide (CPW) transmission line. The JJ array is driven by a pattern of current pulses ("Drive In" in Fig. 1) [7], [8], [9], so that every drive pulse forces each JJ to produce a single voltage pulse with a time-integral of exactly $\Phi_0 \cong 2.06783385$ mV· ps. The ranges of bias parameters over which this single flux response is maintained are defined as the quantum locking ranges (QLRs). The total voltage pulse across the JJ array is the sum of the voltage pulses produced by each JJ. The resulting voltage across the array can be measured directly

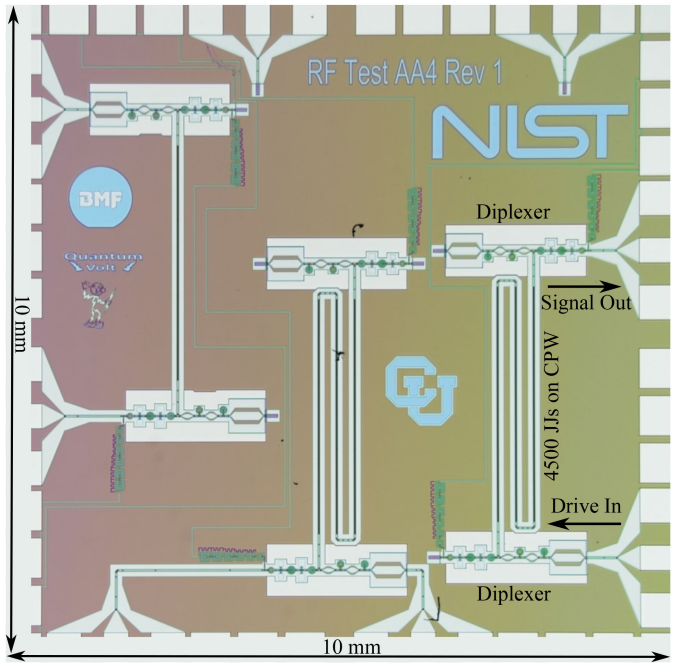

Fig. 1. Photo of the 10×10 mm^2 chip with RF-JAWS circuits. The circuit on the right is used in this article and consists of 4500 Josephson Junctions (JJs) loading a coplanar waveguide (CPW). The diplexers surrounding the JJs provide broadband reflectionless filtering and termination for the current pulses that drive the JJs. The signal flow is marked with arrows. The rest of the chip is occupied by two similar test circuits (bottom, left) and test terminations (top). "Drive In" is the drive current input, and "Signal Out" is the microwave voltage output.

Manuscript received 3 June 2022; revised 5 August 2022; accepted 8 August 2022. Date of publication 24 August 2022; date of current version 2 September 2022. The work of Akim A. Babenko was supported by NIST under an NIST-PREP Fellowship. This article was recommended by Associate Editor I. V. Vernik. *(Corresponding author: Akim A. Babenko.)*

Akim A. Babenko, Gregor Lasser, and Zoya Popović are with the Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, CO 80309 USA (e-mail: akim.babenko@colorado.edu; gregor.lasser@colorado.edu; zoya.popovic@colorado.edu).

Nathan E. Flowers-Jacobs, Justus A. Brevik, Anna E. Fox, Paul D. Dresselhaus, and Samuel P. Benz are with the Superconductive Electronics Group, National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: nathan.flowers-jacobs@nist.gov; justusbrevik@gmail.com; anna.fox@nist.gov; paul.dresselhaus@nist.gov; samuel.benz@nist.gov).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TASC.2022.3201188.

Digital Object Identifier 10.1109/TASC.2022.3201188

at dc/audio frequencies and as an output power at microwave frequencies ("Signal Out" in Fig. 1).

A dc-to-100 kHz JAWS is currently implemented as a primary standard for voltage metrology by the National Institute of Standards and Technology (NIST) [10], [11] and Physikalisch-Technisch Bundesanstalt (PTB) [12], [13], [14]. This primary standard is used to verify the performance of less accurate ac-dc thermal transfer standards [15]. The RF-JAWS is intended to provide a new, quantum-SI-referenced arbitrary waveform source with high spectral purity and signal-to-noise ratio for existing [16], [17], [18] and next-generation communications, to complement and improve calorimeter-based microwave power calibration.

Various efforts to improve RF-JAWS sources focused on filtering of the pulse drive in order to minimize the undesired feedthrough error in the quantum-accurate microwave waveforms, described in Section 6.3 of [19]. This feedthrough error comes from the imperfections in the room-temperature electronics that provides the drive current. When significantly above the system noise floor, that error degrades the RF-JAWS performance. As in the case of low-frequency JAWS [20], digital signal processing (DSP) of the drive current pulse shapes was done using room temperature instrumentation to filter and reject the feedthrough error in RF-JAWS [3]. An analog-signal processing (ASP) approach with a narrowband on-chip bandstop filter [1] is shown to greatly reduce the impact of RF drive on the output, but severely limits the source bandwidth. A commercially available room-temperature broadband filter was used in [3] to improve the source bandwidth, but this approach adds attenuation and dispersion to the drive current signal path. Also in [3], the synthesized microwave voltage amplitude was increased by compensating for the distortion of the broadband filter using digital drive-current pulse equalization. An on-chip superconducting filter offers the possibility of further increase in RF-JAWS output voltage due to the wider filter passband and lower loss. Moreover, the filter frequency response can be designed to match the requirements of a particular RF-JAWS circuit implementation.

In this article, we demonstrate the first RF-JAWS superconducting IC with integrated broadband superconducting diplexers. In Section II, we review the RF-JAWS operation and present new DSP and ASP techniques to compensate for the drive-current distortion that is caused by room-temperature and cryogenic components in the signal path. We also describe the design and layout of the superconducting diplexers. In Section III, we present the QLR measurement setup and results that verify the correct operation of the RF-JAWS at an output magnitude that is 25% larger than the previous state of the art [1], [3], [21]. We also measure the residual feedthrough error due to the pulse drive reaching the output despite the on-chip diplexers and the effect of the feedthrough on the pulse-amplitude QLR measurements.

II. RF-JAWS Circuit Design and Signal Processing

In this section, we review the RF-JAWS operating principles and discuss the parasitic feedthrough voltage from the drive current and new DSP and ASP techniques for distortion compensation.

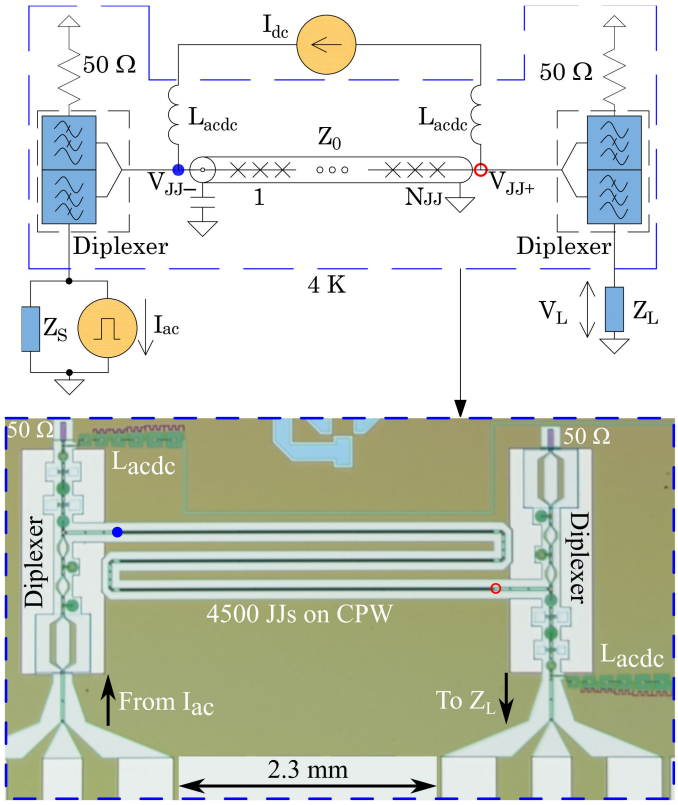

Fig. 2. Top: Circuit diagram of an RF Josephson arbitrary waveform synthesizer (RF-JAWS), driven and biased by currents I_{ac} and I_{dc}. The $\times$ symbol denotes a JJ. Bottom: Photo of the on-chip RF-JAWS circuit with a $N_{JJ} = 4500$ JJ array.

A. RF-JAWS Operation, Circuit Design and Layout

An RF-JAWS circuit consists of an array of thousands of Josephson junctions (JJs) operating at 4 K, with a circuit schematic as shown in Fig. 2. The JJs are integrated in series in the center conductor of a coplanar waveguide (CPW) transmission line of characteristic impedance Z_0. The junctions are driven by a pulse-density-modulated pattern of current pulses I_{ac}, in this article at a maximum available rate of 14.4 G-pulses per second, and a dc bias current I_{dc} [7], [8], [9]. The ranges of pulse amplitude or dc bias over which a positive or negative current pulse causes each JJ to produce a single voltage pulse are referred to as QLRs. The generated output pulse is the sum of the voltage pulses produced by all the JJs in the array. In this work, we use superconductor/normal-metal/superconductor (SNS) junctions with critical current of $I_c = 9.5$ mA and normal resistance $R_n = 4$ mΩ [22] per junction. The photo of one of the two identical diplexers in the RF-JAWS superconducting IC (see Fig. 2) is shown in Fig. 3.

The fabrication process consists of two niobium (Nb) metallic layers separated by 350 nm of silicon-dioxide with Nb via interconnects, as in [3], [23], and[24], allowing for metal-insulator-metal (MIM) capacitors and planar inductors. A resistive 2 $\Omega/\square$

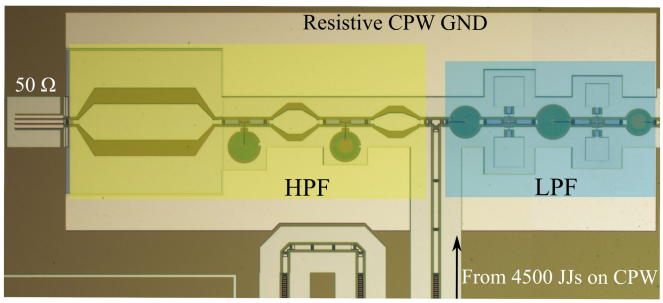

Fig. 3. Zoom-in photo of the diplexer connected to the output of the 4500-JJ array (right-hand side in Fig. 2). The shaded areas show the high-pass filter (HPF) and the low-pass filter (LPF).

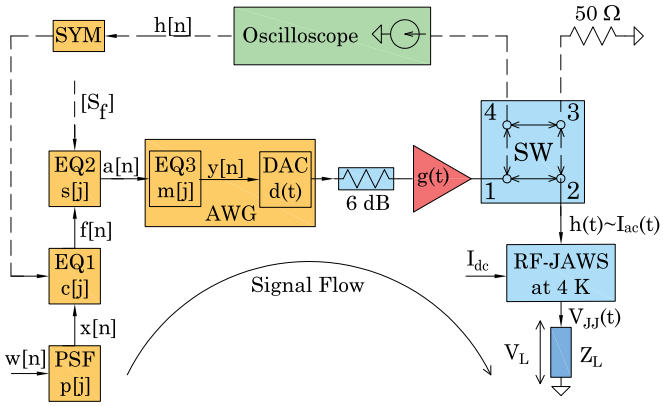

Fig. 4. RF-JAWS mixed-signal processing block diagram. Dashed lines denote off-line signal flow. The digital-to-analog converter (DAC) with impulse response d(t) and the amplifier g(t) are used to generate and amplify the analog delta-sigma pulses h(t) that are proportional to the drive current I_{ac}. The oscilloscope and switch (SW) are used to sample the analog signal h(t) for processing in the symmetrization block SYM. The pulses h(t) drive the RF-JAWS circuit at 4 K that generates the quantum-based voltage V_{JJ}. The waveforms are measured as the power across the load Z_L.

gold-palladium (AuPd) metallization is included at the top Nb electrode level. The silicon substrate is 350 μm thick and has a 2 $\Omega/\square$ backside AuPd layer with no via interconnect. The CPW ground is thus not connected to the backside metal. The top and backside metallic layers can therefore support parasitic parallel-plate modes. We found in the simulations that the resistive CPW ground (2 $\Omega/\square$ AuPd 120 nm thick metallization connected to the top Nb layer, see Fig. 3) suppresses the parasitic modes without attenuating the CPW mode [25].

The diplexer design is a combined five-pole 50 Ω singly-terminated lumped-element LPF and HPF with a 2.5 GHz cutoff [25]. The HPFs have a passband from 2.6 to 27 GHz with less than 0.8 dB insertion loss and >10 dB return loss. In the RF-JAWS circuit (see Fig. 2), the drive current pulses first get high-passed by the HPF at the input of the nominally 50 Ω JJ-loaded CPW transmission line. Each pulse then forces each of the 4500 JJs to generate exactly one voltage pulse while propagating through the loaded CPW line. At the end of the array, the HPF of the second diplexer terminates the drive current pulses and the output voltage pulses are then low-passed in the LPF of that diplexer. Due to the passband of the diplexers being greater than a decade and lossless superconducting electrodes, their HPFs provide nearly lossless propagation and termination of the drive current pulses, as well as of the JJ voltage pulses.

The synthesized voltage waveform $V_{JJ}(t)$ is determined by the drive pulse pattern I_{ac} and number of junctions, N_{JJ}, equal to 4500 in this work. Generating arbitrary waveforms is accomplished by using delta-sigma (Δ-Σ) modulation. At each Δ-Σ time step $T_{clk} = 1/f_{clk}$, all the JJs are driven by current to produce either a positive pulse, for drive current pulse corresponding to a $+1$ symbol in the delta-sigma code, a negative pulse (-1), or no pulse (0). This approach can synthesize high-signal-to-noise ratio signals using a limited number of pulse output levels [26] (in this case three) while minimizing the associated digitization noise within some bandwidth around a synthesis frequency f_t. A Δ-Σ modulator is a feedback loop that shapes this quantization noise with a noise transfer function (NTF) that has a notch around f_t. Low-pass (LP) Δ-Σ modulation was used to encode JAWS waveforms from dc to 100 kHz [7], [9], [11], while band-pass (BP) Δ-Σ modulation is used for RF JAWS [1], [2], [21]. The highest f_t synthesis frequency is limited primarily by the highest available f_{clk} and the feedback parameters of the Δ-Σ modulator [26]. The f_t has a resolution limited by the number of samples in the Δ-Σ pattern and the resolution of f_{clk}.

At microwave frequencies, it is difficult to measure voltages directly and typically a power measurement across a known load, e.g. $Z_L = 50\ \Omega$, is measured. The low-frequency component of V_{JJ} is measured directly across the JJ array, e.g. with low-pass filters (L_{acdc} as in Fig. 2). The generated JJ pulse train propagates to the load Z_L where V_L is measured. This measured voltage depends on V_{JJ}, Z_S, and Z_L. The on-chip value of V_{JJ} is known exactly, and Z_S and Z_L can be evaluated using calibrated scattering-parameter (S-parameter) measurements along with the impedance of the JJ array Z_{JJ}, as detailed in [21] and [27]. In this work, the demonstration of diplexer performance does not require a full S-parameter calibration and therefore we take $Z_S = Z_L = 50\,\Omega$ and $Z_{JJ} = 0\,\Omega$ when calculating RF power generated by the JJ array, as was shown to be a good approximation in [21]. In the remainder of the article, we present new digital and analog drive-current signal processing techniques, and circuit designs that substantially enhance RF-JAWS performance.

B. Drive Current Mixed-Signal Processing

The RF-JAWS mixed-signal (analog and digital) processing diagram used in this work is shown in Fig. 4. The drive current generation begins with the 3-level digital Δ-Σ pulse sequence $w[n]$ ($n = 0, \ldots, N-1$) of length N, as described in Section II-A. The Δ-Σ clock rate at 14.4 giga-pulses per second is nearest-neighbor interpolated to a 57.6 GSa/s sampling rate of the digital-to-analog converter (DAC) in the arbitrary waveform generator (AWG). The commercially available instruments and components used in this article are identical to the ones in [3][1].

[1]Commercial instruments and devices are referenced in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified is necessarily the best available for the purpose.

Drive current at the synthesis frequency creates a parasitic "feedthrough" voltage that adds coherently to the quantum-based JJ voltage signal, through $Z_{\rm L}$ and any nonzero series impedance of the RF-JAWS IC and cabling (see top Fig. 2). We reduce this error by attenuating the power at the synthesis frequency f_t in the drive signal. As described in Section II-B and Fig. 3 of [3], we digitally high-pass filter the pulse drive by using 5-level (-1, -0.5, 0, 0.5, 1) drive pulse shapes. For these pulse shapes, the central, unity-area, ± 1 pulse is surrounded by two half-area ∓ 0.5 pulses, reducing the drive signal power at f_t by more than 30 dB at frequencies up to 1 GHz. Due to the JJ nonlinearity, only the central ± 1 drive current pulse is sufficiently above I_c to force each JJ to create a voltage pulse with integrated area Φ_0. The half-area ± 0.5 pulses do not cause the JJs to pulse, and perform only high-pass filtering of the drive current. The 3-to-5-level conversion is implemented by the pulse-shaping filter (PSF) block in the signal processing chain.

The PSF and equalizers EQ1, EQ2, and EQ3 are finite-impulse-response (FIR) filters [28] with coefficients (taps) $p[j]$, $c[j]$, $s[j]$ and $m[j]$ ($j \in \mathbb{Z}$), respectively. The equalizers EQ1-EQ3 compensate for the distortion that occurs in the drive-current signal path as follows. The initially ideal 5-level Δ-Σ pulse sequence $x[n]$ (see Fig. 4), with EQ1-EQ3 deactivated ($c[j] = s[j] = m[j] = \delta[j]$, where δ is the Kronecker delta function) reaches the DAC of the AWG unchanged as $y[n] = a[n] = f[n] = x[n]$. The 5-level pulses then propagate through and get distorted by the following:

1) The frequency response of the room temperature drive-current signal path—the DAC in the AWG plus the amplifier [g(t) in Fig. 4] that is necessary to provide the drive current peak pulse amplitude.
2) The frequency response of the high-pass filter (HPF) in the on-chip superconducting diplexers used in the RF-JAWS IC (see Figs. 2 and 3).
3) The frequency response of the room-to-cryogenic temperature cabling.

First, we compensate for the room temperature drive-current signal path using EQ1. We determine EQ1 using the transfer switch SW in the dashed position, the sampling oscilloscope and a symmetrization (SYM) DSP block (see all in Fig. 4). Briefly, analog room-temperature components used here mainly distort the 5-level pulses by creating asymmetries in them, and the SYM block aims at symmetrizing the pulses back to their initial shape. The room-temperature components, as well as the symmetrization algorithm, are presented in detail in [3].

Second, the EQ2 equalizer compensates for the S-parameters of the HPF used in the on-chip superconducting diplexer at the input of the JJ array in the RF JAWS IC (see Fig. 2). Previously, we designed, fabricated and characterized the on-wafer frequency response of the diplexers, as reported in [25]. In particular, we measured the 2×2 S-parameter matrix $[S_{\rm f}]$ from 10 MHz to 27 GHz for a two-port network made of the three-port diplexer whose LP port was terminated, as for the left-side diplexer in Fig. 2. The elements in $[S_{\rm f}]$ are next used to calculate the EQ2 filter taps $s[j]$ and equalize the 5-level pulses f[n] as follows.

1) Calculate the frequency response $s[\omega]$ of the EQ2 coefficients $s[j]$ as $e^{j \cdot arg(1/S_{21})}$, where j is the imaginary unit and $arg()$ denotes the argument (phase) of a complex number. The S_{21} magnitude of > -0.8 dB within its passband from 2.6 to 27 GHz [25] is essentially flat and negligible for equalization purposes.
2) Calculate the discrete Fourier transform (DFT) for the Δ-Σ pulse sequence f[n] of length N at the input of EQ2 to obtain its frequency-domain representation $f[\omega]$.
3) Calculate the equalized-waveform frequency response $a[\omega] = f[\omega] \cdot s[\omega]$ on a frequency grid limited to the diplexer's HPF passband.
4) Calculate the inverse DFT (IDFT) of the equalized waveform as $a[n] = IDFT(a[\omega])$.

Third, EQ3 compensates for the linear distortion in the cabling between the top of the dewar at room-temperature and the diplexers in front of the JJ array at 4 K. That linear distortion makes the drive current pulses $I_{\rm ac}$ at the JJ array different compared to the pulses $h(t)$ at the top of the dewar that were equalized by EQ1. Following [3], we used time-efficient low-frequency dc-bias QLR measurement to perform a manual, adaptive optimization of the EQ3 taps $m[j]$. The EQ3 equalizer is a 16-tap real-time FIR at 57.6 GSa/s. In past work, this QLR-based manual equalization technique was used to compensate for the distortion of the entire drive-current signal path [11], [20], [29]. As in [3], we rely on the low-frequency QLR for optimizing the microwave waveform synthesis by using a two-tone delta-sigma waveform.

The Δ-Σ waveform used here generates an open-circuit voltage across the JJ array of 0.088 mV rms at 10 kHz and 21.955 mV rms (-26.18 dBm into 50 Ω) at 1.005 GHz—a 25% increase compared to the state of the art 17.564 mV rms at 1.005 GHz reported in [3]. As in [3], we chose a synthesis frequency of 1.005 GHz to avoid intermittent spurs observed in the measurement setup at 1 GHz that was used in [1]. The amplitude increase is provided by the wider bandwidth and lower insertion loss of the integrated superconducting diplexers used in this work compared to [3]. The programmed digital waveform is 500 μs or 28.8 million samples long, comprising five 10 kHz periods and 502 500 periods at 1.005 GHz. This waveform length allows the Δ-Σ algorithm to achieve a calculated average spurious-free dynamic range of about 100 dBc within a bandwidth of 10 MHz around 1.005 GHz. The Δ-Σ NTF is a convolution of a fourth-order BP NTF centered around 1.005 GHz and a first-order LP NTF (see Fig. 4 in [3]).

III. Stability and Feedthrough Measurements

In this article, we demonstrate that the JAWS with on-chip diplexers is operating correctly at large output amplitude by measuring QLRs with respect to variations in the $I_{\rm dc}$ magnitude and $I_{\rm ac}$ peak pulse amplitude. When these parameters are varied outside the QLR, one or more JJs in the array will no longer generate exactly one voltage pulse for each drive current pulse. The measurement setup used to perform these measurements is described in Section III-A. Missing or extraneous pulses in the frequency domain are quantified from the measured amplitude

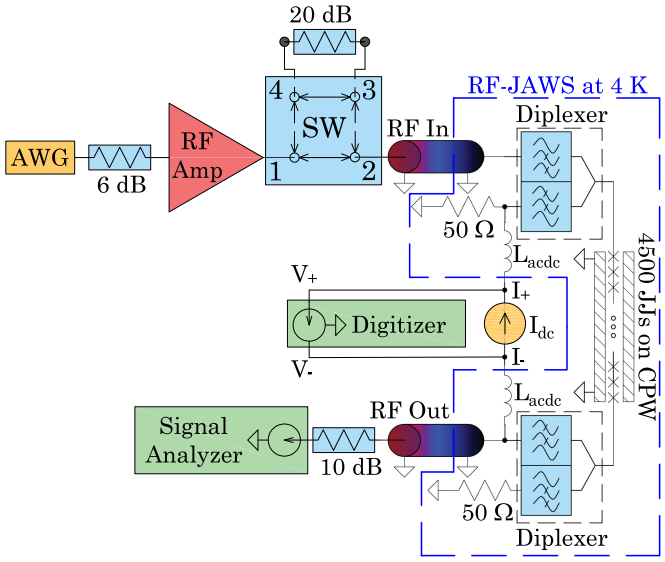

Fig. 5. Diagram of the quantum locking range (QLR) measurement setup. The AWG and RF amplifier output the delta-sigma patterns equalized using DSP from Fig. 4. Ports 3 and 4 of SW can be bypassed (solid position) or connected to a 20 dB attenuator to measure the feedthrough signal (dashed position). The drive-current is filtered with the HPF of the diplexer at the RF input of the JJ array. The open-circuit voltage is measured across the JJ array with the digitizer and the dc current bias is applied using a current source I_{dc}, in a four-probe configuration. At the RF output, the microwave tones are measured with the signal analyzer after LPF and 10 dB attenuator.

of the synthesized voltage at frequencies below 1 MHz and microwave spectra around 1.005 GHz. Within the QLR, the amplitude and spectral purity do not change as a drive and/or bias parameter is varied, as we show in Section III-B. Several effects lead to systematic errors within the QLR: the bias parameters affect the timing and shape of the JJ pulses [30], [31]; and the drive pulse feedthrough changes with the I_{ac} pulse amplitude. We explain the effect of the large feedthrough error on the QLR measurements in Section III-C.

A. QLR Measurement Setup

The diagram of the setup is shown in Fig. 5. The AWG, RF amplifier, and switch (SW) are the same as in the mixed-signal diagram (see Fig. 4). The current source I_{dc} biases the JJs and the digitizer is used to measure V_{JJ} for frequencies up to 1 MHz. Both instruments are connected to the corresponding $I_{\pm}$ and $V_{\pm}$ contacts of the JJ array in a four-probe configuration, as shown in Fig. 5. The feedthrough signal is measured with the SW in the state shown by the dashed lines and the QLRs are measured with the SW in the state shown by the solid lines. Specifically, we show that the Δ-Σ pattern of drive-current pulses forces each JJ to create a single voltage pulse per drive pulse by measuring both the dc-bias and pulse-amplitude QLRs simultaneously at dc, 10 kHz and 1.005 GHz. The models of the particular instruments and devices used here are identical to those in [3].[2]

[2]Commercial instruments and devices are identified in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified is necessarily the best available for the purpose.

The QLRs at 10 kHz are obtained by changing either the dc-bias current or the AWG's programmed pulse amplitude while digitizing the voltage across the JJ array at 1 MSa/s. We evaluate the magnitude of the 10 kHz tone and its total harmonic distortion (THD) as a function of either bias or drive parameter. The dc-bias QLR can be measured quickly and accurately by applying I_{dc} as a triangular ramp at 1 Hz and digitizing an entire period of the ramp in a single digitizer acquisition [20]. The pulse-amplitude QLR, however, is measured on a point-by-point basis. We also use the dc component of V_{JJ} to verify the operation of our JJ array. Because the two-tone Δ-Σ pattern ideally has a zero dc component, it will deviate from zero outside the QLR due to missing or extraneous JJ pulses and, in contrast, will remain constant within the QLR. Following [3], this time-efficient low-frequency dc-bias QLR measurement is used to perform a manual, adaptive optimization of the EQ3 taps to compensate for the frequency response of the room-to-cryogenic temperature cabling.

The microwave signal proportional to the JJ voltage (V_L in Figs. 2 and 4) is measured at room temperature after 10 dB attenuation at the "RF Out" cable. The 10 dB attenuator reduces the return loss at the diplexer output, and therefore, the VSWR of the drive current along the JJ array. Also, because the LPFs in the on-chip diplexers are of fifth order, the attenuator helps prevent the compression of the signal analyzer caused by high-power, out-of-band tones in the synthesized Δ-Σ pulse pattern. The signal analyzer is used to measure the spectra at and around the synthesized 1.005 GHz tone, acquired with 2 Hz resolution and video bandwidths for each dc current point produced by I_{dc} [1] and for each pulse-amplitude point produced by the AWG.

B. QLR Measurement Results

The dc-bias and pulse-amplitude QLR measurements are shown in Fig. 6. The dc voltage magnitude is the metric used to quantify the QLR at dc as in [32] [(a) and (d) in Fig. 6]. The rms voltage amplitude of the 10 kHz tone and its total harmonic distortion (THD) up to 500 kHz are used to quantify the low-frequency QLR, as in [11], [20] [(b) and (e) in Fig. 6]. The power at 1.005 GHz and the average power spectral density (PSD) within $\pm$250 kHz around the tone are the two metrics used to quantify the microwave-frequency QLR [1], [21] [(c) and (f) in Fig. 6]. The microwave power of $\cong -37.7$ dB at the signal analyzer is consistent with the $\cong$ 10 dB attenuation from the combination of room temperature attenuation, the room-to-cryogenic temperature cabling attenuation, and the mismatch of the signal analyzer. We obtained a QLR over a dc-bias range greater than 1 mA at an AWG amplitude of 0.400 V_{p-p} [(a)–(c) in Fig. 6] and a fractional pulse-amplitude QLR greater than 7 % (0.400 V_{p-p} to 0.430 V_{p-p}) at 0 mA dc-bias current [(d)–(f) in Fig. 6]. Over these ranges, the low-frequency THD and rms voltage do not depend on the bias or the drive parameter, and are constant to better than 2 dB within the QLR and better than 0.3 μ V, respectively. The 1.005 GHz average PSD and tone power are constant with a flatness better than 0.2 and 0.005 dB, respectively. Outside of these ranges, the curved dependencies indicate missing or extraneous JJ voltage pulses compared to

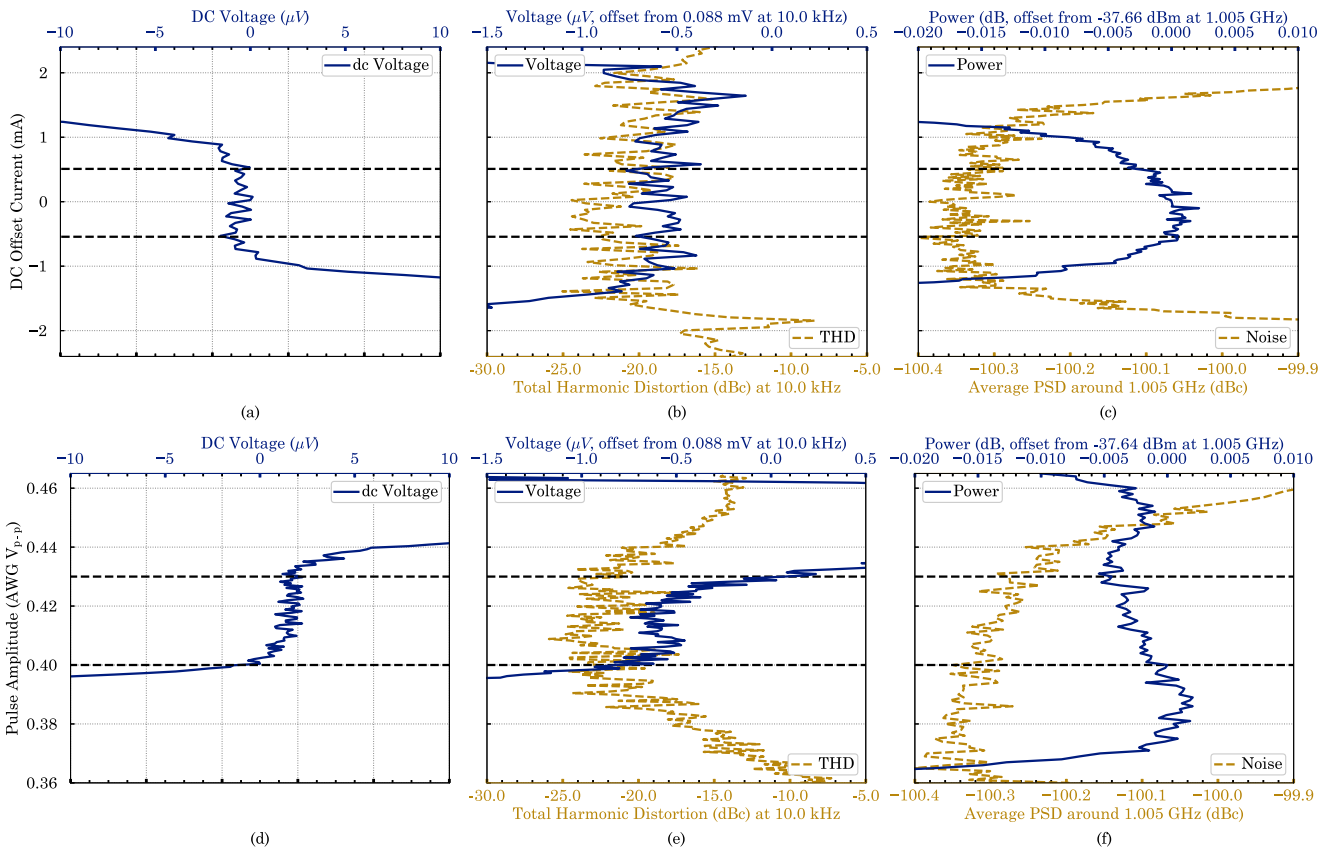

Fig. 6. QLR at dc (a), (d), 10 kHz (b), (e) and 1.005 GHz (c), (f) versus dc offset current $I_{\rm dc}$ (a)–(c) and programmed AWG peak-to-peak amplitude (d)–(f). The dc-bias QLRs are measured at a 0.400 $V_{\rm p-p}$ AWG amplitude and the pulse-amplitude QLRs are measured at $I_{\rm dc} = 0$. The horizontal black dashed lines show the QLR margins.

the drive signal. We show in Section III-C that the slope in the pulse-amplitude QLR measurements at 1.005 GHz [see Fig. 6(f)] is due to the large −33 dBc feedthrough that increases by 0.4 dB with the drive-current pulse amplitude.

To better visualize this measurement, we expanded the microwave QLR measurements to a 2-D sweep over both the dc-bias and the pulse amplitude, as shown in Fig. 7. The values of the parameters used for the detailed sweeps in Fig. 6 are shown as lines in Fig. 7. The tone power and average PSD were expected to have roughly elliptical combined QLR [3], Fig. 11]. We see, however, an asymmetry in the tone-power QLR [see Fig. 7(a)] due to again the high feedthrough amplitude that varies with respect to the pulse amplitude and in time. Note that each dc-bias sweep in Fig. 7 took about 13 min and the pulse-amplitude sweep step was 2 mV. This reduced the pulse-amplitude QLR compared to Fig. 6(f) due to the variation of the feedthrough over time that is caused by the drift in the room-temperature drive-current electronics (AWG, RF amplifier and cabling in Fig. 5.

C. 1.005 GHz Feedthrough Measurements

We evaluate the parasitic feedthrough voltage dependencies on both dc bias and the pulse amplitude, as well as its variation over the typical 13-min QLR measurement sweep time. The observed feedthrough is consistent with the curvature within the QLR for the 1.005 GHz tone versus pulse amplitude observed in Fig. 6(f). As described in Section III-A, we measured the feedthrough signal at 1.005 GHz using the SW in the state shown by the dashed lines in Fig. 5 which inserts the 20 dB attenuator after the RF amplifier. To also assess the possible variations of the feedthrough with time, we make two sweeps—from the maximal to the minimal value and back, with each sweep taking about 13 min.

The parasitic feedthrough measurements are shown in Fig. 8. In Fig. 8(a), the dc bias was swept between 2 and −2 mA while measuring the power at 1.005 GHz. Overall, the feedthrough varies by no more than 0.1 dB across the entire sweep and is essentially constant (to within the trace noise of the signal analyzer and the noise of the current source) within the ±0.5 mA QLR observed in Fig. 6(c). In Fig. 8(b), the programmed AWG pulse amplitude was swept between 0.5 $V_{\rm p-p}$ and 0.3 $V_{\rm p-p}$ while again measuring the power at 1.005 GHz. There is a variation of the feedthrough voltage by about 3 dB over the entire sweep and about 0.4 dB (from −33.5 to −33.1 dBc) within the 0.400 $V_{\rm p-p}$ to 0.430 $V_{\rm p-p}$ QLR observed in Fig. 6(f).

The magnitude of the total complex voltage $V_{\rm L}$ across the load impedance $Z_{\rm L}$ (in our case the impedance of the signal analyzer) at 1.005 GHz can be written as

$$|V_{\rm L}| = |V_{\rm fund} + V_{\rm fdt}| \tag{1}$$

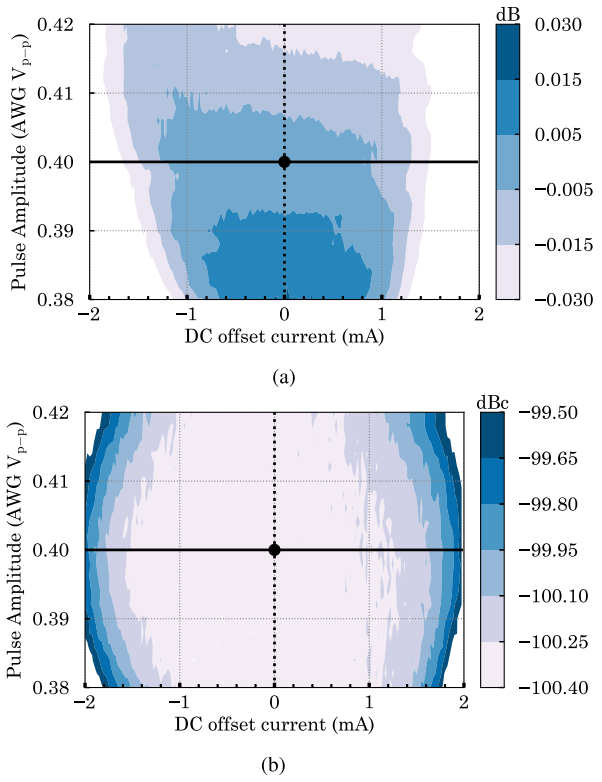

Fig. 7. Combined dc-bias and pulse-amplitude QLRs for the synthesized 1.005 GHz tone in terms of tone power deviation (a) and average PSD (b) DC-bias sweep in Fig. 6(c) follows the horizontal solid lines and the pulse-amplitude sweep in Fig. 6(f) follows the dotted vertical lines.

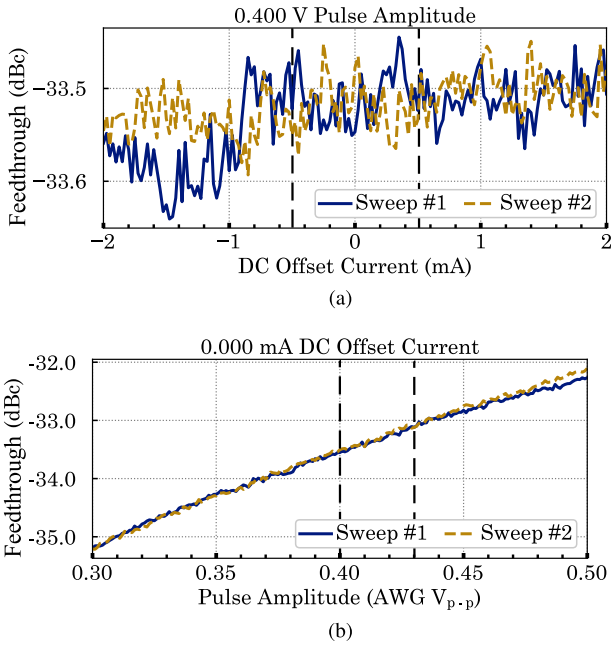

Fig. 8. Repeated feedthrough measurements at 1.005 GHz versus dc offset current (a) and drive current pulse amplitude (b). The power on the y-axis is normalized to the −36.7 dBm measured raw power at 1.005 GHz with JJs pulsing at nominal pulse-amplitude and dc-bias settings described in Figs. 6 and 7, after taking into account the 20 dB attenuator.

where V_{fund} is the complex voltage across the load due to the generated JJ voltage V_{JJ} and V_{fdt} is the complex voltage across the load due to the feedthrough. Assuming that V_{fund} and V_{fdt} are perfectly in- or out-of-phase, the observed feedthrough variation across the QLR of 0.4 dB [see Fig. 8(b)] would result in a change in the measured V_{L} of 0.008 dB. This is consistent with the observed variation [see Fig. 6(f)] because the relative phase of V_{fdt} also varies within the QLR due to the current-dependent Josephson inductance [22]. This dependence is also likely to explain the 0.002 dB curvature of the dc bias QLR at 1.005 GHz observed in Fig. 6(c), even though there is no variation in $|V_{\text{fdt}}|$ with dc bias [see Fig 8(a)].

IV. Conclusion

In this article, we demonstrate the first RF-JAWS with broadband integrated superconducting diplexers. The use of the integrated filtering enables 25% larger microwave amplitudes compared to the state-of-the-art, thanks to broader passband and lower loss. We also employed a new drive-pulse equalization scheme that accounts for the frequency response of the on-chip diplexers. We determined that the system was stable and operating correctly by measuring quantum-locking ranges. We also estimated the time-dependent and drive-parameter dependent impact of a ≅ -33 dBc feedthrough on the QLR measurements. While not detrimental, this large feedthrough will have to be taken into account when characterizing an application-ready RF-JAWS system. This work opens opportunities for designing and fabricating diplexers of different types, orders and cutoff frequencies and using the simulated data directly to equalize the drive current pulses to compensate the dispersion associated with the filters.

Future work will include designing diplexers of higher orders to improve the feedthrough filtering, and identifying the maximum allowable self-resonant frequencies of those diplexers to avoid severe distortion of the drive current caused by the resonances. We will also investigate the effect of bias- and drive-current-dependent feedthrough phase on the variation of the JJ voltage within the QLR explore ways to minimize the drifts in our measurement setup to reduce their impact on the QLR measurements.

Acknowledgment

The authors would like to thank the NIST Boulder Microfabrication Facility for the support in the fabrication of the superconducting JAWS chips described in this work. Z. Popovic would like to thank Lockheed Martin Endowed Chair in RF Engineering at the University of Colorado. This work is a contribution of the U.S. government and is not subject to U.S. copyright.

References

[1] C. A. Donnelly et al., "1GHz waveform synthesis with Josephson junction arrays," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 3, pp. 1–11, Apr. 2020.
[2] P. F. Hopkins et al., "RF waveform synthesizers with quantum-based voltage accuracy for communications metrology," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, pp. 1–5, Aug. 2019.

[3] A. A. Babenko et al., "A microwave quantum-defined millivolt source," *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 12, pp. 5404–5416, Dec. 2021.
[4] R. A. Ginley, "Traceability for microwave power measurements: Past, present, and future," in *Proc. IEEE 16th Annu. Wireless Microw. Technol. Conf.*, 2015, pp. 1–5.
[5] T. M. Wallis, T. P. Crowley, D. X. LeGolvan, and R. Ginley, "A direct comparison system for power calibration up to 67 GHz," in *Proc. Conf. Precis. Electromagn. Meas.*, 2012, pp. 726–727.
[6] F. R. Clague and P. G. Voris, "Coaxial reference standard for microwave power," Nat. Inst. Stand. Technol., Boulder, CO, USA, Tech. Note 1357, pp. 1–52, 1993.
[7] J. X. Przybysz et al., "Josephson junction digital to analog converter for accurate AC waveform synthesis," U.S. Patent 5 812 078, Sep. 22, 1998.
[8] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Appl. Phys. Lett.*, vol. 68, no. 22, pp. 3171–3173, 1996. [Online]. Available: https://doi.org/10.1063/1.115814
[9] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, L. A. Christian, and J. X. Przybysz, "Pulse-driven Josephson digital/analog converter," *IEEE Trans. Appl. Supercond.*, vol. 8, no. 2, pp. 42–47, Jun. 1998.
[10] N. E. Flowers-Jacobs, A. Rüfenacht, A. E. Fox, P. D. Dresselhaus, and S. P. Benz, "Calibration of an AC voltage source using a Josephson arbitrary waveform synthesizer at 4V," in *Proc. Conf. Precis. Electromagn. Meas.*, 2020, pp. 1–2.
[11] N. E. Flowers-Jacobs, A. E. Fox, P. D. Dresselhaus, R. E. Schwall, and S. P. Benz, "Two-volt Josephson arbitrary waveform synthesizer using Wilkinson dividers," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 6, pp. 1–7, Sep. 2016.
[12] O. F. Kieler, J. Kohlmann, R. Behr, F. Muller, L. Palafox, and J. Niemeyer, "SNS Josephson junction series arrays for the Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 2, pp. 187–190, Jun. 2007.
[13] O. F. Kieler, R. Iuzzolino, and J. Kohlmann, "Sub-μm SNS josephson junction arrays for the Josephson arbitrary waveform synthesizer," *IEEE Trans. Appl. Supercond.*, vol. 19, no. 3, pp. 230–233, Jun. 2009.
[14] M. Kraus et al., "Measurement and analysis of high-frequency voltage errors in the Josephson arbitrary waveform synthesizer," *Meas. Sci. Technol.*, vol. 31, no. 12, 2020, Art. no. 125003.
[15] J. M. Underwood, "Uncertainty analysis for AC-DC difference measurements with the AC Josephson voltage standard," *Metrologia*, vol. 56, no. 1, 2018, Art. no. 15012.
[16] 3GPP. Release 8. 2020. [Online]. Available: https://www.3gpp.org/specifications/releases/72-release-8
[17] 3GPP. Release 10. 2020. [Online]. Available: https://www.3gpp.org/specifications/releases/70-release-10
[18] 3GPP. Release 15. 2020. [Online]. Available: https://www.3gpp.org/release-15
[19] C. Donnelly, "Development of a quantum-based superconducting radio-frequency voltage standard," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, Mar. 2019.
[20] N. E. Flowers-Jacobs, A. A. Babenko, A. E. Fox, J. A. Brevik, P. D. Dresselhaus, and S. P. Benz, "Zero-compensation Josephson arbitrary waveform synthesizer at 1.33 V," in *Proc. Conf. Precis. Electromagn. Meas.*, 2020, pp. 1–2.
[21] J. A. Brevik et al., "Cryogenic calibration of the RF Josephson arbitrary waveform synthesizer," in *Proc. Conf. Precis. Electromagn. Meas.*, 2020, pp. 1–2.
[22] T. V. Duzer and C. W. Turner, *Principles of Superconductive Devices and Circuits*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1999, ch. 4.
[23] B. Baek, P. D. Dresselhaus, and S. P. Benz, "Co-sputtered amorphous Nb_x Si_{1-x} barriers for Josephson-junction circuits," *IEEE Trans. Appl. Supercond.*, vol. 16, no. 4, pp. 1966–1970, Dec. 2006.
[24] A. S. Boaventura et al., "Microwave modeling and characterization of superconductive circuits for quantum voltage standard applications at 4 K," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 2, pp. 1–7, Mar. 2020.
[25] A. A. Babenko et al., "Cryogenic decade-passband superconducting integrated diplexer," in *Proc. IEEE-MTT Int. Microw. Symp.*, 2022, pp. 1–4.
[26] G. T. S. Pavan and R. Schreier, *Understanding Delta-Sigma Data Converters*, 2nd ed. Hoboken, NJ, USA: Wiley, 2017.
[27] A. S. Boaventura et al., "Cryogenic calibration of a quantum-based radio frequency source," in *Proc. 95th ARFTG Microw. Meas. Conf.*, 2020, pp. 1–4.
[28] H. E. Kallmann, "Transversal filters," *Proc. IRE*, vol. 28, no. 7, pp. 302–310, 1940.
[29] N. E. Flowers-Jacobs, S. B. Waltman, A. E. Fox, P. D. Dresselhaus, and S. P. Benz, "Josephson arbitrary waveform synthesizer with two layers of Wilkinson dividers and an FIR filter," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 6, pp. 1–7, Sep. 2016.
[30] C. A. Donnelly et al., "Quantized pulse propagation in Josephson junction arrays," *IEEE Trans. Appl. Supercond.*, vol. 30, no. 3, pp. 1–8, Apr. 2020.
[31] C. A. Donnelly, J. A. Brevik, P. D. Dresselhaus, P. F. Hopkins, and S. P. Benz, "Jitter sensitivity analysis of the superconducting Josephson arbitrary waveform synthesizer," *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 11, pp. 4898–4909, Nov. 2018.
[32] C. J. Burroughs et al., "NIST 10 V programmable josephson voltage standard system," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 7, pp. 2482–2488, Jul. 2011.

Akim A. Babenko (Graduate Student Member, IEEE) received the B.S. degree in electronics and nanoelectronics and the M.S. degree in radiophysics from Kuban State University, Krasnodar, Russia, in 2017 and 2019, respectively. His B.S. and M.S. research was on the vector network analysis of microwave mixers. He is currently working toward the Ph.D. degree in electrical engineering with the National Institute of Standards and Technology, Boulder, CO, USA, on the Quantum Voltage Project.

Upon graduation in 2017, he did a summer internship with Fermilab, Batavia, IL, USA, developing DSP firmware for superconducting accelerating RF cavities. He joined Prof. Popovic's group with the University of Colorado, Boulder, CO, USA, in Fall 2018. He works on designing multidecade bandwidth passive and active monolithic microwave integrated circuits (MMICs) in III–V and superconductor technologies, as well as developing new measurement, and signal processing techniques for RF Josephson arbitrary waveform synthesizes.

Nathan E. Flowers-Jacobs (Member, IEEE) received the B.S. degree from the California Institute of Technology, Pasadena, CA, USA, in 2001, and the Ph.D. degree from the University of Colorado-Boulder, Boulder, CO, USA, in 2010, both in physics.

He worked with MIT Lincoln Laboratory modeling radar cross sections for two years before entering graduate school with JILA and the University of Colorado-Boulder for his work on a quantum-limited detector of nanomechanical motion based on electron tunneling across an atomic point contact. From 2010 to 2014, he was a Postdoctoral Associate with Yale University, New Haven, CT, USA, working on nanomechanical displacement measurements at the quantum limit using optical cavities. In 2014, he joined the Quantum Voltage Project with the National Institute of Standards and Technology (NIST), Boulder, CO, USA, and has been working on development, characterization, and applications of the Josephson arbitrary waveform synthesizer (JAWS), an ac Josephson voltage standard based on pulse-biased arrays of Josephson junctions.

Dr. Flowers-Jacobs was the recipient of the IEEE Council on Superconductivity Van Duzer Prize in 2019.

Gregor Lasser (Member, IEEE) received the Dipl.-Ing. and the Dr. Techn. degrees in electrical engineering (both with distinction) from the Vienna University of Technology, Vienna, Austria, in 2008 and 2014, respectively.

In 2015, he joined the University of Colorado, Boulder, CO, USA, where he has been an Assistant Research Professor since August 2017. In January 2022, he joined Chalmers University of Technology, Gothenburg, Sweden, as an Assistant Professor. His research interests include broadband supply and bias modulated power amplifiers, analog linearization, electronically augmented antennas, and active interference cancellation circuits.

Dr. Lasser's research so far has received several prices, starting with the second prize EEEfCOM innovation award in 2008 for his diploma thesis project. From 2016 to 2021, he has served as the Vice Chair of the IEEE Denver joint AP-S/MTT section. His doctoral dissertation on passive RFIDs for automotive sensors received the department award of the electrical engineering and information technology department of the Vienna University of Technology. In April 2017, he received the best paper award of the WAMICON conference.

Justus A. Brevik (Member, IEEE) received the B.S. degree from the University of Washington, Seattle, WA, USA, in 2002, and the Ph.D. degree from the California Institute of Technology, Pasadena, CA, USA, in 2012, both in physics. He received the Ph.D. degree for his work on the measurement of cosmic microwave background polarization using the BICEP2 telescope.

He joined the National Institute of Standards and Technology (NIST) Boulder, CO, USA, as a National Research Council Fellow in 2012, where he worked on transition edge sensor detectors and the microwave superconducting quantum interference device multiplexer for astrophysics applications. In 2014, he joined a startup company attempting to launch thermal rockets into space using beamed microwave power generated by gyrotrons. He returned to NIST-Boulder in 2015 to work in the Quantum Voltage Project, where he is developing a Josephson arbitrary waveform synthesizer capable of creating quantum-accurate waveforms in the gigahertz regime for telecommunications and quantum information applications.

Dr. Brevik was thew recipient of the IEEE Council on Superconductivity Van Duzer Prize in 2019.

Anna E. Fox (Senior Member, IEEE) received the Ph.D. degree in electrical engineering from Drexel University, Philadelphia, PA, USA, in 2009.

From 2009 to 2010, she was a National Research Council Postdoctoral Researcher with the Optoelectronics Division, National Institute of Standards and Technology, Boulder, CO, USA, where she worked fabricating superconducting transition-edge sensors for use at optical wavelengths. She continued her work in transition-edge sensor fabrication in the NIST Quantum Sensors Project where she fabricated arrays of TES bolometers for cosmic microwave background detection. She has been with the NIST Quantum Voltage Project since 2013 pursuing the design and fabrication of voltage standard devices such as the programmable Josephson voltage standard and the ac Josephson voltage standard.

Dr. Fox was the recipient of the 2016 and 2019 IEEE Council on Superconductivity Van Duzer Prize.

Paul D. Dresselhaus was born in Arlington, MA, USA, on January 5, 1963. He received the B.S. degree in physics and electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1985 and the Ph.D. degree in applied physics from Yale University, New Haven, CT, USA, in 1991.

In 1999, he joined the Quantum Voltage Project, with the National Institute of Standards and Technology (NIST), Boulder, CO, USA, where he has been developing novel superconducting circuits and broadband bias electronics for precision voltage waveform synthesis and programmable voltage standard systems. He has been the Project Leader of the Quantum Voltage Project with NIST since October 2015. He was with Northrop Grumman, Falls Church, VA, USA, for three years, where he designed and tested numerous gigahertz-speed superconductive circuits, including code generators and analog-to-digital converters. He also upgraded the simulation and layout capabilities with Northrop Grumman, to be among the world's best. He has also been a Postdoctoral Assistant with State University of New York, Stony Brook, NY, USA, where he worked on the nanolithographic fabrication and study of Nb-AlOx-Nb junctions for single-electron and SFQ applications, single-electron transistors and arrays in Al-AlOx tunnel junctions, and the properties of ultrasmall Josephson junctions.

Dr. Dresselhaus was the recipient of two U.S. Department of Commerce Gold Medals for Distinguished Achievement and the IEEE Council on Superconductivity Van Duzer Prize in 2006, 2016, and 2019.

Zoya Popović (Fellow, IEEE) received the Dipl. Ing. degree in electrical engineering from the University of Belgrade, Belgrade, Serbia, and the Ph.D. degree in electrical engineering from Caltech, Pasadena, CA, USA.

She was a Visiting Professor with the Technical University of Munich, Munich, Germany, from 2001 to 2003, and with ISAE, Toulouse, France, in 2014, and was a Chair of Excellence with Carlos III University in Madrid, Madrid, Spain, from 2018 to 2019. She has graduated over 65 Ph.D.s and currently advises 17 doctoral students. She is currently a Distinguished Professor and the Lockheed Martin Endowed Chair in Electrical Engineering with the University of Colorado, Boulder, CO, USA. Her research interests include high-efficiency power amplifiers and transmitters, microwave and millimeter-wave high-performance circuits for communications and radar, medical applications of microwaves, quantum sensing and metrology, and wireless powering.

Dr. Popović was the recipient of two IEEE MTT Microwave Prizes for best journal papers, the White House NSF Presidential Faculty Fellow award, the URSI Issac Koga Gold Medal, the ASEE/HP Terman Medal, and the German Alexander von Humboldt Research Award. She was elected as a Foreign Member of the Serbian Academy of Sciences and Arts in 2006. She was named IEEE MTT Distinguished Educator in 2013 and the University of Colorado Distinguished Research Lecturer in 2015.

Samuel P. Benz (Fellow, IEEE) was born in Dubuque, IA, USA, on December 4, 1962. He received the B.A. degree (*summa cum laude*) in physics and math from Luther College, Decorah, IA, USA, in 1985 and the M.A. and Ph.D. degrees in physics from Harvard University, Cambridge, MA, USA, in 1987 and 1990, respectively.

In 1990, he joined the National Institute of Standards and Technology (NIST), Boulder, CO, USA, as a NIST/NRC Postdoctoral Fellow and became a permanent Staff Member in January 1992. He has been the Project Leader of the Quantum Voltage Project with NIST since October 1999, and a Group Leader of the Superconductive Electronics Group since 2015. He has worked on a broad range of topics within the field of superconducting electronics, including Josephson junction array oscillators, single flux quantum logic, ac and dc Josephson voltage standards, Josephson waveform synthesis, and noise thermometry. He has over 290 publications and is the holder of four patents in the field of superconducting electronics.

Dr. Benz is a fellow of NIST and the American Physical Society (APS). He is a Member of Phi Beta Kappa and Sigma Pi Sigma. He has received three U.S. Department of Commerce Gold Medals for Distinguished Achievement, the 2016 IEEE Joseph F. Keithley Award, and the IEEE Council on Superconductivity Van Duzer Prize in 2006, 2016, and 2019. He was awarded an R.J. McElroy Fellowship (1985–1988) to work toward the Ph.D. degree.