Cryogenic Decade-Passband Superconducting Integrated Diplexer

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***Abstract* — We demonstrate a decade-passband superconducting diplexer operating from dc to 27 GHz, integrated in a niobium, Josephson junction (JJ) compatible process. Both low- and high-pass branches of the diplexer are singly-terminated 5-pole Butterworth filters with a 2.5 GHz cutoff. Several diplexer test circuits were characterized with on-wafer cryogenic two-port calibration by terminating the third port of the device. Insertion loss below 0.8 dB are measured across the entire frequency range. Good agreement between measurements and simulations up to 27 GHz suggests that the upper diplexer band extends to the over-a-decade simulated 40 GHz. This device can be integrated in large-scale superconducting JJ-based quantum processors, broadband sensors, amplifiers and sources.**

***Keywords* — Diplexers, superconducting integrated circuits, superconducting filters, cryogenic on-wafer calibration.**

I. Introduction

Superconducting microwave and millimeter(mm)-wave circuits are an important technology for some approaches to quantum computing [1], sensing [2] and metrology [3]. To achieve superconducting operation and enable non-classical behavior, the devices typically operate at cryogenic temperatures. While initial signal generation and final measurements occur at the room temperature, there is a need for cryogenic passive microwave devices integrated with active quantum devices such as e.g. Josephson junctions (JJs) [4], to avoid additional cabling and associated loss in highly-integrated systems. Filters are an essential part of superconducting microwave front ends. For example, low-pass filters are required in bias networks [4], and highly-selective band-pass/-stop filters are essential for multiplexed quantum sensors [5]. Diplexers are also useful for JJ-based voltage sources [3], [4], where decade-bandwidth passbands are required for pulsed signal filtering.

Contiguous multiplexers consist of several singly-terminated filtering branches with a common input [6], each providing low-loss transmission to an output that covers a specific frequency range. When two such branches are combined, the filter is referred to as a diplexer. It is difficult to achieve an over-an-octave passband per branch with transmission-line filter elements (open-/short-circuited stubs, coupled lines etc.) due to their periodic frequency response. Lumped-reactance implementations, however, have bandwidth limitations only due to self-resonance frequencies (SRFs).

Wideband superconducting transmission-line-based filter and multiplexer designs have been reported [7]–[10] with passbands up to 2.5 octaves and covering a variety of microwave and mm-wave bands from UHF to W-band. With the exception of the triplexer in [9], none of the prior work reports on-wafer calibrated cryogenic performance, which is relevant for e.g. large-scale quantum-computing applications [1].

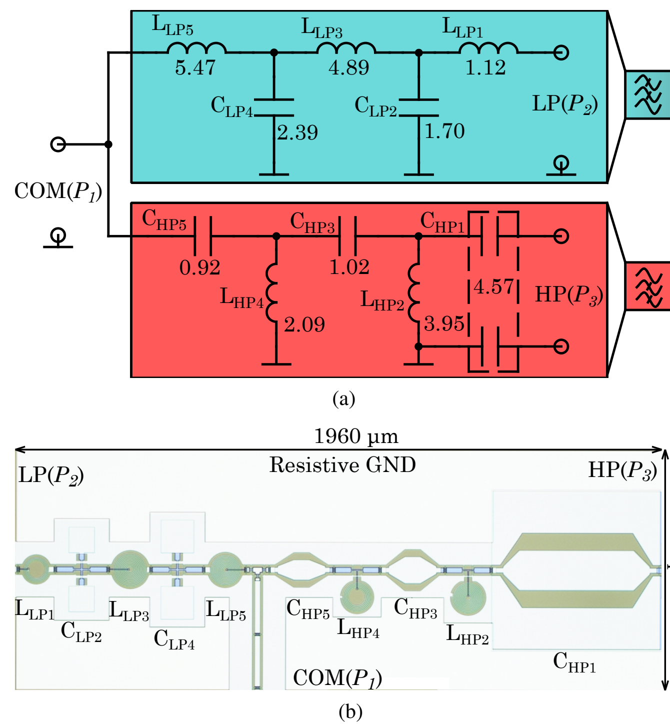
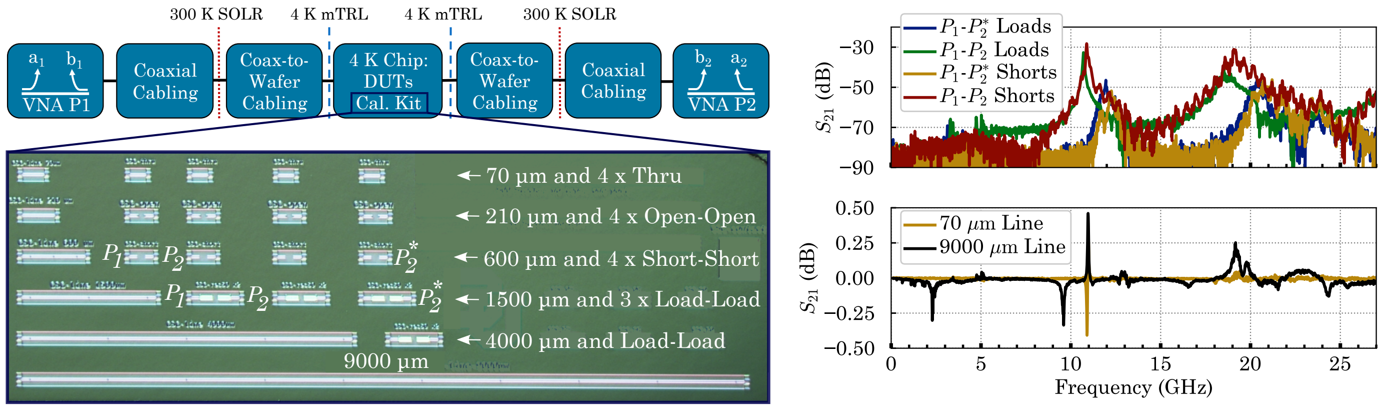


Fig. 1. Schematic (a) and photo (b) of the superconducting lumped-element low-pass/high-pass diplexer. COM denotes the common port, LP – low-pass, HP – high-pass. In (a), all capacitances are in pF and inductances are in nH. The $C_{HP1} = 4.57$ pF value is the short-circuit signal-ground capacitance.

In this paper, we demonstrate a decade-passband superconducting lumped-element diplexer embedded in coplanar waveguide (CPW) and integrated in a JJ-compatible process. The low-pass (LP) branch has the cutoff frequency of 2.5 GHz, while the high-pass (HP) branch is designed with a passband from 2.6 GHz to 40 GHz. The circuit schematic and layout of the diplexer are shown in Fig. 1. The diplexer is characterized using on-wafer calibration at 4 K, and the performance measured up to 27 GHz agrees well with simulations.

II. Lumped-Element Diplexer Design

The diplexer circuit consists of LP and HP singly-terminated Butterworth branches. The fifth order of the filters was chosen as a tradeoff between flatter group delay and stop-



(a)

(b)

Fig. 2. (a) Calibration and measurement diagram and photo of the on-wafer calibration kit. The P_x and P_x^* labels indicate locations of probe landings used in (b). (b) Coupling between Short and Load standards calibrated at 300 K (top), as well as transmission of 70 µm and 9000 µm lines calibrated on-wafer at 4 K (bottom). Both tiers of the calibration indicate resonant coupling between the on-wafer standards that results in calibration errors at select frequencies. For comparison, the coupling between the probes was below −60 dB after the 300 K calibration when they were above the chip and at any horizontal spacing.

band attenuation. To achieve a broad upper passband, we used lumped elements with values calculated following [6]. The design and EM simulations were performed in the Cadence AWR environment and the 2.5-D electromagnetic simulator AXIEM. The metal-insulator-metal (MIM) capacitors in the HP branch, shown in Fig. 1b, were designed inside the CPW line to maintain a 50 Ω impedance, while obtaining the desired capacitance value. We chose the rectangular MIM capacitors in the LP branch for interconnect simplicity. Circular spiral inductors were used for the smallest possible area and high SRF. An ac-coupled ground, required for the targeted application in one of the branches, was implemented with $\mathrm{C_{HP1}}$.

The fabrication process, compatible with JJ integration, consists of two niobium (Nb) metallic layers separated by 350 nm of silicon-dioxide with Nb via interconnects, similar to [11]. That allows for the MIM capacitors and the planar inductors. A resistive 2 Ω/□ gold-palladium (AuPd) metallization is included at the top Nb electrode level. The silicon substrate is 350 µm thick and has a 2 Ω/□ backside AuPd layer with no via interconnect. The CPW ground is thus not connected to the backside metal that is eventually mounted to a copper chuck. The top and backside metallic layers can therefore support parasitic parallel-plate modes. We found in the simulations that the resistive CPW ground (Fig. 1b) dampens the parasitic modes without attenuating the CPW mode. The resistive CPW ground is the 2 Ω/□ AuPd 120 nm thick metallization connected to the top Nb layer.

III. Cryogenic On-Wafer Measurements

The diplexer test circuits were characterized with a cryogenic probe station. The calibration diagram and the on-wafer mTRL calibration kit are shown in Fig. 2a. We first performed a coaxial Short-Open-Load-Reciprocal (SOLR) [12] vector network analyzer (VNA) calibration at the room temperature, followed by an on-wafer multi-line Thru-Reflect-Line (mTRL) [13] calibration at 4 K that moves the reference planes from external coaxial to on-wafer probe connections. The mTRL kit consists of multiple identical pairs of one-port standards: Short-Short (used as "Reflect" [13]); and Load-Load (used for reference-impedance re-normalization to 50 Ω [14]) at different spacings. It also has a zero-length ("Thru") CPW line, and (70, 210, 600, 1500, 4000 and 9000) µm CPW lines to cover the entire 27 GHz frequency range (10 MHz step). The fabricated chip with the calibration standards and the diplexer was mounted on a copper chuck for thermal contact at 4 K.

Fig. 2b demonstrates the resonant coupling between the mTRL kit components after applying the first-tier SOLR (around 11 GHz and 19 GHz, top subplot) and second-tier mTRL (additionally around 2.5 GHz and 10 GHz, bottom subplot) corrections. In particular, the top plot shows the coupling between the Short and Load standards when landing the measurement probes closer to (P_1-P_2 in Fig. 2a) and farther away from each other (P_1-P_2^*, used in the calibration). We measured a similar resonant coupling for the Open standards. The bottom subplot demonstrates the mTRL-calibrated transmission for the shortest and longest line standards with additional lower-frequency resonances for the latter. These extra resonances around 2.5 GHz and 10 GHz are not a concern since the 9000 µm line was used in the mTRL calibration primarily below 2.5 GHz, where its phase shift is well below 160° [13].

The photos of fabricated two-port test circuits are shown in Fig. 3a-c. Two ports of the three-port diplexer were measured for each circuit, while the third port was terminated with nominally 50 Ω. The Load standard was used as the termination and had at least 20 dB measured return loss over the entire measurement frequency range. Fig. 3d shows measured results compared with the EM simulations of the diplexer with an ideal 50 Ω termination at all ports. Both simulations and measurements in Fig. 3d show the 2.5 GHz cutoff frequency, as well as <0.8 dB insertion and >10 dB return loss within the decade-wide 2.6 GHz to 27 GHz passband. The parasitic resonances degrading the performance are only seen in simulations above 40 GHz, since our VNA was limited up to 27 GHz.

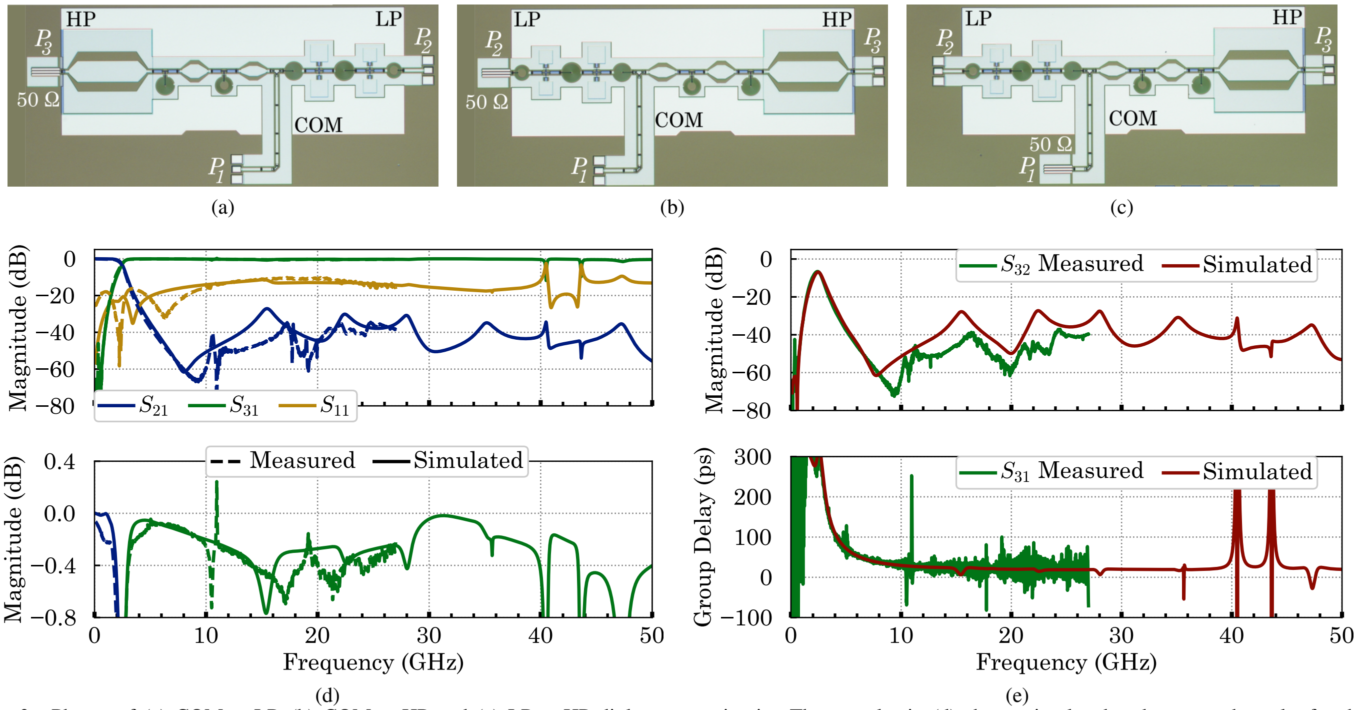


Fig. 3. Photos of (a) COM-to-LP, (b) COM-to-HP and (c) LP-to-HP diplexer test circuits. The top plot in (d) shows simulated and measured results for the main transmission and reflection responses. The bottom plot in (d) magnifies the passbands of the LP and HP branches. The top plot in (e) shows the measured and simulated isolation between the LP and HP branches. The bottom plot in (e) demonstrates the group delay of the HP branch.

Fig. 3e shows the isolation between LP and HP ports (top subplot), measured with the circuit in Fig. 3c, as well as the group delay response (bottom subplot) of the HP transmission coefficient from the circuit in Fig. 3b, demonstrating good agreement between simulations and measurements. On the same chip, we fabricated a test circuit identical to the one in Fig. 3b but with a superconducting CPW ground. The measurements with the superconducting versus resistive grounds were almost identical in terms of both insertion and return loss.

IV. Conclusion

In summary, we have demonstrated a diplexer with a record 2.6 GHz to 27 GHz, decade-wide HP passband, integrated in a JJ-compatible niobium-on-Si process. The simulations indicate that the HP passband extends up to 40 GHz, as shown by the solid lines in Fig. 3. Given the good agreement up to 27 GHz, it is likely that the diplexer's HP passband would cover a 2.6 GHz to 40 GHz (16:1) range. The low insertion and high return loss across the multi-octave passband make this circuit useful for integration into 4 K superconducting quantum circuits. The agreement between simulations and measurements enables designs of other types of integrated superconducting filters.

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