Understanding Early Failure Behavior in 3D-Interconnects: Empirical Modeling of Broadband Signal Losses in TSV-Enabled Interconnects

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***Abstract*— We develop an empirical model for measured frequency-dependent insertion loss ($|S_{21}|$). The model parameters are determined with a stochastic optimization implementation of the Levenberg–Marquard method. We compare measured $|S_{21}|$ on through silicon via (TSV)-interconnects, from two different providers, as a function of the extent of thermal annealing. The frequency-dependent changes in the electrical characteristics of the interconnect are attributed to silanol (Si-OH) and other dangling bond polarizations at the Si–SiO interface between the silicon substrate and the lateral silicon oxide that isolates the coaxial metal core from the silicon substrate. The changes in the polarizations are traceable to changes in the chemistry of the isolation dielectric during thermal annealing. The data also suggest that the evolution of the chemical defects inherent in the "as-manufactured" products may be responsible for some of the signal integrity degradation issues and other early reliability failures observed in TSV-enabled 3-D devices.**

***Index Terms*— 3D-interconnects, chemical defects, dielectric polarization, empirical modeling, insertion loss, stochastic optimization, thermal cycling, TSV.**

I. Introduction

THE mechanical and electrical properties of integrated circuits (ICs) change during the fabrication process and over time, even in storage, due to the changes in chemistry of the materials of construction [1], [2]. A root cause of wear-out is the thermomechanical stresses that develop in the bulk materials and at material interfaces under normal operating temperature fluctuations. Thus, the reliability of electronic devices depends on the materials of construction, integration schemes, thermal history, use conditions, the structures of the devices, and test conditions. Hence, there is the need for predictive models to correlate the dominant fundamental failure modes and their respective root cause mechanisms (i.e., physics of failure). We expect the reliability of through silicon via (TSV) to depend on the materials choices and the process flow; for example, the low-temperature processes used, as in the "via-last" process flow results in metastable materials due to the incomplete reactions in the films deposition processes such as the SiOH-rich subatmospheric pressure (SACVD) isolation oxide used to achieve adequate sidewall coverage along the entire length of the high aspect ratio features [3], [4], [5], [6]. Such low-temperature (∼200 °C) SACVD silicon oxide when heated condenses to result in increased hydrostatic stress in the coaxial copper [7]. We recently reported on the evolution of the electrical properties of the isolation dielectrics in TSVs and suggested that the thermal stress change in the TSV structure is the result of chemical transformation of the metastable materials in the "as-manufactured" products and may be responsible for the defects formation and growth in the devices [8]. We have previously established a strong correlation between device failure rate and the effective Young's modulus of the encapsulating dielectric stack; the in-fab yield fall-out rate increases with increasing stiffness of the encapsulating layer due to the increase in thermal stress in the metal-dielectric composite [9]. In that report, we also showed that an increased concentration of silanol (SiOH) reduces the stiffness of the encapsulating SiO, leading to reduced local defect formation. Thus, the chemistry of the materials of construction is critical to the reliability of the device.

The current work is motivated by these apparent correlations between material choices and device performance. Here, we reexamine accelerated TSV aging data [10] to develop a predictive model linking the device's reliability with the thermal history. Here, we compare two different TSV-enabled two-level stacked test devices fabricated by SEMATECH

Manuscript received 8 June 2022; revised 25 August 2022; accepted 1 September 2022. Date of publication 23 September 2022; date of current version 24 October 2022. Certain commercial equipment, instruments, or materials are identified in this report to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose. The review of this article was arranged by Editor P. Thadesar. *(Corresponding author: Yaw S. Obeng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2022.3204936.

Digital Object Identifier 10.1109/TED.2022.3204936

(Albany, NY, USA) with "via-last" process flow [11] and the "via-mid" process flow from CEA-LETI (Grenoble, France) [12]. The emphasis of this work is to compare the impact of material choices dictated by the respective process flows on microwave signal dissipation in the respective test devices. While the SEMATECH flow employed a low-temperature SACVD, the LETI process flow used thermally grown SiO [12], as the isolation layer to electrically separate the coaxial metal from the silicon host substrate. We expect the two device types to behave differently electrically and in their sensitivities to external stress. The devices studied in this work are comprised of dedicated ground-signal-ground (GSG) RF-test structures in which the signal line incorporates daisy chains of two-level stacked dies with TSVs of various lengths. The SEMATECH test devices were comprised of daisy chains of 60 signal TSVs of Ø 5 μm diameter $\times$ 50 μm deep fabricated in host Si with resistivity: $\sim$18 Ω cm, while the LETI test structures were comprised of chains of two signal TSVs, 10 μm diameter and 100 μm deep in similar silicon host. As the device configurations enable direct access to intrinsic reliability of TSV interconnects, the observed and predicted $|S_{21}|$ include losses in the bond pads, the interconnection lines, as well as the TSVs. These test structures are similar to those described in the literature [10], [15]. The samples were stored at room temperature in a nitrogen-purged enclosure for more than nine months before being used for this study.

We have shown elsewhere that there is significant die-to-die variation in the insertion loss magnitude ($|S_{21}|$) of "as-manufactured" wafers because of large differences in the local stress due to the high local SiOH concentration and preexisting defects in the DUT [13], [14]. The die-to-die variability in the electrical properties could also have geometrical contributions, such as those due to process topography variability [e.g., across-wafer total thickness variation (TTV)] that leads to differences in TSV height, and isolation SiO thickness variability, as well as process-induced defects such as those related to impurities, voids, cracks from the copper fill electroplating, and damage from the plasma etching of pattern definition. The variability could also be linked to the local intrinsic electrical defects. Hence, the die-to-die variability of $|S_{21}|$ and the degradation of $|S_{21}|$ with thermal exposure could be the result of a combination of structural, material properties changes, and intrinsic electrical defects.

The measured $|S_{21}|$ also changes with thermal exposure; Figs. 1 and 2 show increasing insertion loss with an increasing number of thermal cycles for a single die each from the LETI and SEMATECH, respectively. In general, for each die, the insertion loss increases, i.e., $|S_{21}|$ decreases, as the number of thermal cycles increases due to the formation of mechanical and other sources of scattering, such as stress-induced defects in the microwave signal path [10]. We have shown elsewhere that the mean hydrostatic stress in a SEMATECH fabricated Cu TSV changes from (16 $\pm$ 44) MPa in the "as-received" to (123 $\pm$ 37) MPa after 1000 thermal cycles [7]. Inspection of these figures shows that the insertion losses are much larger in the SEMATECH samples than in the LETI samples. This difference illustrates the potential impact of process flow, material choices, and architecture on device robustness.

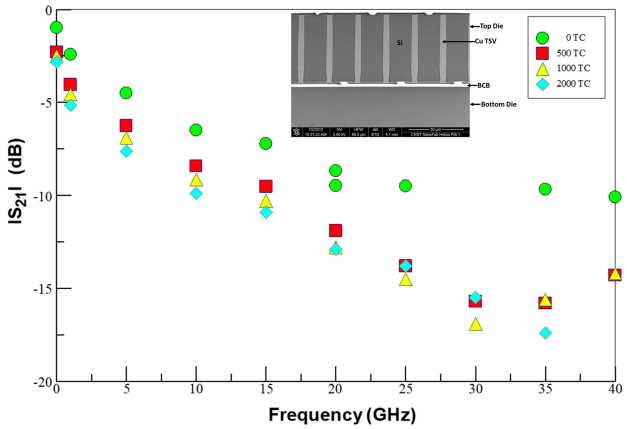

Fig. 1. Evolution of insertion losses ($|S_{21}|$) with thermal cycling of a single die produced by SEMATECH [10]. (Inset: cross-sectional SEM micrograph of a segment of the TSV daisy chains.)

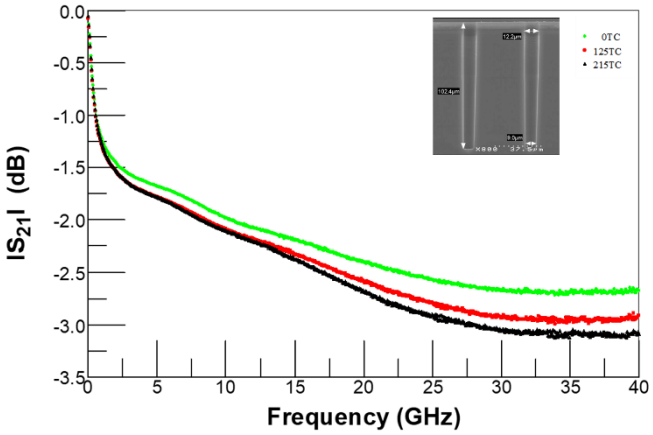

Fig. 2. Evolution of insertion losses ($|S_{21}|$) with thermal cycling of a single die produced by CEA-LETI [12]. (Inset: cross-sectional SEM micrograph of the two TSV test structures.)

II. Modeling

Here, we present a statistical empirical model that accounts for thermal effects and characterizes incipient defects and their evolution as the device ages. The statistical empirical model captures the changes in the electrical properties of the DUTs as the materials of construction change during thermal aging. The presented model is a modified model of defects in TSV-enabled interconnects from [15], which describes the TSV isolation dielectric and conductor failure in a single equivalent circuit model. In nanoscale systems, boundary layers and interfaces strongly influence the electrical properties [16]. In modeling the broadband electromagnetic response of TSV-enabled test structures, we must consider the impact of all the signal propagation modes on the signal integrity: 1) the dielectric quasi-transverse electromagnetic (quasi-TEM) mode where the signal travels through both the dielectric and the metal; 2) the slow wave where the substrate resistance adds substantially to the signal loss and retards the signal propagation; and 3) skin effect. The operating frequency range of each of these modes depends on several factors, including the resistivity of the silicon substrate, the thickness of SiO isolation layers, as well as the TSV dimensions [17]. When the

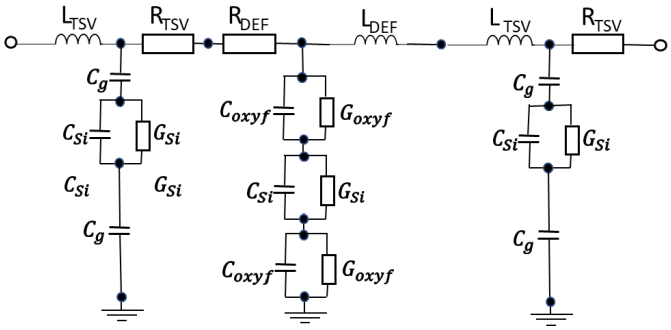

Fig. 3. Equivalent circuit model used to define parameters (R_{DEF}, L_{DEF}, C_{oxyf}, and G_{oxyf}).

microwave frequency is not very high, such as in this study, and the resistivity of the silicon substrate is moderate, such as those used in monolith-IC circuit technology, the substrate acts as a semiconductor, and a slow-surface wave propagates along the TSV-Si interface [18]. Thus, in this work, the slow wave propagation mode is expected to be the dominant mechanism of insertion loss ($|S_{21}|$). Furthermore, we expect strong interfacial polarization at the SiO–Si interface to perturb the microwave signal propagation [17]. Hence, $|S_{21}|$ is expected to be frequency dependent and sensitive to any dangling bonds and the changing chemistry of the isolation oxide due to thermal cycling.

The equivalent circuit model parameters, inductor with inductance L_{TSV}, silicon substrate with conductance G_{Si}, capacitors with capacitance C_{Si} and C_g, resistors with resistance R_{Si}, and a frequency-dependent resistance R_{TSV} are defined by physical models described elsewhere in the literature [19], [20], [21], [22], [23]. These parameters are not adjustable and are set to nominal values based on LETI and SEMATECH test structures. In Fig. 3, R_{DEF} and L_{DEF} represent the dc resistance and the inductance of the defects such as voids, cracks from the copper fill electroplating, and crack or impurities in the dielectric, through the defect resistivity and inductance, and the capacity, respectively, and C_{oxyf} and G_{oxyf} represent the capacitance and conductivity change due to thermal cycling of the isolation oxide, respectively. We define effective R_{DEF} as

$$R_{\mathrm{DEF}} = R^* \left(\frac{f}{f_0}\right)^{\gamma} \tag{1}$$

where $((f/f_0)^{\gamma})$ is a resistance scaling factor, R^* and γ are nonnegative model parameters, f is the frequency of the microwave signal, and $f_0 = 1$ Hz.

Based on a transform of the equivalent circuit into a two-port network (i.e., T-pad circuit), we predict the frequency-dependent theoretical scattering parameters that characterize the TSV module. We determine our model parameters by a stochastic optimization procedure that seeks the global minimum of the mean-squared deviation between broadband measurements of $|S_{21}|$ and their associated predicted values based on an equivalent circuit model. In our empirical model, we set nonadjustable model parameters to nominal values. Adjustable model parameters are determined by a stochastic optimization method. For other applications where the TSVs differ from than those considered in our study, one would require a method to determine the nominal values of the nonadjustable model parameters based on the TSV attributes (e.g., geometry, materials of construction, and fabrication process).

A. Estimation of Model Parameters

For the ith frequency, we define the theoretical equivalent circuit model prediction of $|S_{21}|(i)$ and an empirical model prediction of the measured value $|S_{21}|_{\mathrm{mean}}\ (i)$ as $|S_{21}|\ (i)$

$$\widehat{|S_{21}|}(i) = \alpha + \beta * \widetilde{|S_{21}|}(i) \tag{2}$$

where α and β are adjustable offset and scale parameters, respectively. The seven adjustable model parameters form a model parameter vector θ where $\theta = f\ (L_{\mathrm{DEF}}, R^*, R_{\mathrm{oxyf}}, C_{\mathrm{oxyf}}, \beta, \alpha, \gamma)$. We determine θ with the three-stage stochastic optimization method similar to the approach we have described elsewhere [24]. For given estimates of the adjustable parameters R^* and γ and the frequency, we can directly determine the frequency-dependent R_{DEF}. It must be emphasized that this is not an analytical model with an explicit relationship between $|S_{21}|$, gamma, and R^*. The full model is outside the scope of this report.

B. Stochastic Optimization

Here, we describe how we estimate our model parameters, which we denote as a vector θ. We seek to minimize the mean square deviation between predicted and observed $|S_{21}|$ with a modified Levenberg–Marquard [26] method where we specify a lower and upper bound for each model parameter. In stage 1, we simulate N_{sim} random realizations of θ. Each random initial parameter value is sampled from a Gaussian distribution centered on a preliminary estimate of θ. For each component of θ, the standard deviation of the sampling distribution equals p times the difference of its upper and lower bounds where $p < 1$. (Generally, $p = 0.01$ for the data studied here.) If a simulated value of a model parameter falls outside its allowed interval, we set it to the closest of the two boundary values. For each simulated initial value of θ, we determine a final estimate (and the associated value of the cost function) with the Levenberg–Marquardt method. In stage 2, we simulate N_{sim} random realizations of θ from a uniform distribution based on the lower and upper bounds assumed in stage 1 (see Table I). We select the estimate that yields the lowest value of the cost function from stages 1 and 2. In stage 3, we simulate N_{sim}random realizations of θ centered on the best estimate determined from stages 1 and 2. However, the standard deviation of the sampling distribution is ten times less than in stage 1. The final estimate of θ is the one with the lowest associated cost function. In the first-pass analysis, initial values of components of θ are set to the associated mean of the upper and lower bounds for those components. In subsequent optimizations, initial values are equated to first-pass analysis results. We determine the results at larger values of N_{sim} to confirm that model parameter estimates are numerically stable. For the cases studied here, the results are reported for N_{sim} values ranging from 2000 to 8000.

TABLE I
CEA-LETI DATA

	Number of thermal cycles	L_{DEF} (H)	R* (Ω)	R_{oxyf} (Ω)	C_{oxyf} (F)	β	α	ɣ	RMS
Die 1	0	3.06E-09	220.18	94.911	3.01E-15	2.0236	0.87337	0.14657	0.001298
	55	2.97E-09	221.31	128.21	3.53E-15	2.3082	0.85861	0.14703	0.001344
	215	3.16E-09	455.78	82.237	1.38E-29	2.5759	0.8379	0.10618	0.001461
Die 2	0	3.31E-09	212.11	80.921	5.35E-15	2.075	0.86477	0.14288	0.001408
	55	3.01E-09	165.91	128.71	5.61E-15	2.1841	0.86422	0.15737	0.001464
	125	3.05E-09	236.31	87.201	6.39E-15	2.2356	0.85578	0.13748	0.001381
	215	2.98E-09	196.19	104.45	6.52E-15	2.2229	0.85803	0.14745	0.001477
	343	3.36E-09	344.17	102.52	3.93E-27	2.5384	0.8397	0.11842	0.004369

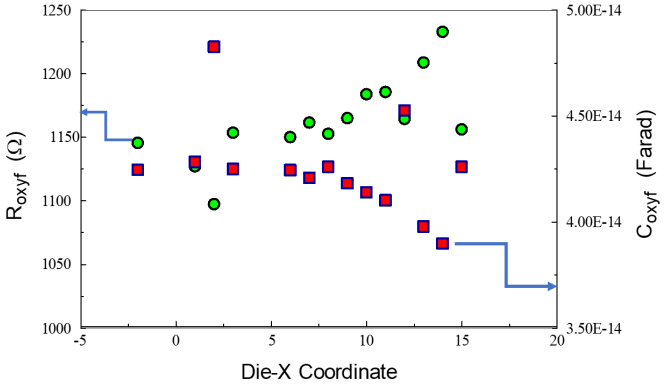

Fig. 4. Spatial variation of estimated isolation oxide resistance (R_{oxyf} in green circles) and estimated oxide capacitance (C_{cxyf} in red squares) of "as-received" dies produced by CEA-LETI.

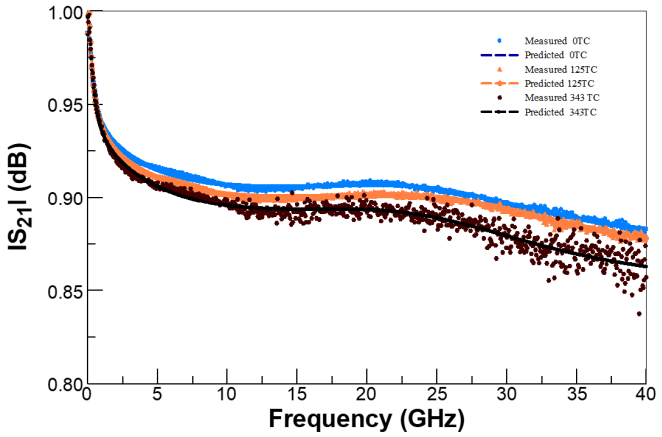

Fig. 5. Comparison of the evolution of measured $|S_{21}|$ and predicted $|S_{21}|$ as a function of thermal cycle for a representative CEA-LETI die.

Our stochastic optimization method is an example of a multi-start method for avoiding getting stuck in a local minimum of the cost function [26]. The upper and lower bounds of each modeling parameter are summarized in Table I.

C. Modeling Results

While we studied devices from both SEMATECH and CEA-LETI, for brevity, we will illustrate this report with only figures from the latter. In our analysis, some circuit model parameters are set to nominal values. For example, we set $L_{TSV} = 1.197 \times 10^{-10}$ H, $C_{Si} = 1.172 \times 10^{-14}$ F, $R_{Si} = 1588\ \Omega$, $C_g = 4.789 \times 10^{-13}$ F, and $R_{TSV} = 1.342 \times 10^{-4}(f)^{1/2}/f_0\ \Omega$, where $f_0 = 1$ Hz for the LETI test structures.

Fig. 4 shows the estimated spatial variation of estimated isolation oxide resistance (R_{oxyf} in green circles) and estimated oxide capacitance (C_{oxyf} in red squares) isolation silicon oxide (SiO) resistance and capacitance, respectively, of the "as-received" dies from a single 300-mm wafer from CEA-LETI. Clearly, there is a location dependence of the estimated electrical properties: the effective model oxide resistance increased, while the effective model oxide capacitance decreased, from the center toward the edge of the wafer inspection of the figure revealing that while the two estimated quantities agree in the center of the wafer, they tend to diverge in devices located toward the outer edge of the 300-mm wafer. The spatial distribution of the estimated electrical properties is reminiscent of the spatial variation of SiOH concentration on a 300-mm wafer [13] and the thermal profile of the wafer susceptor during isolation SiO deposition [27]. Table I shows how estimated model parameters for CEA-LETI data vary with thermal cycles (from 0 to 343) and die locations, while Table II shows how estimated model parameters for SEMATECH data vary with thermal cycles (from 0 to 5000) and die locations. In the tables, rms is the root-mean-square deviation between observed and predicted values of $|S_{21}|$. The number of thermal cycles is shown in the second column.

Fig. 5 compares the measured and predicted insertion loss spectra $|S_{21}|$ for a representative LETI die. Inspection of the figure shows that the measured and predicted $|S_{21}|$ are nearly the same for all cases (except the noisy measured data for the 340 thermal cycles).

D. Empirical Model for R* and Gamma (ϒ)

For each provider and devices at the ith location, we model the estimated value of R^* as

$$\widehat{R_i^*} = a_0 + a_1 c_i + \epsilon_{R,i} \tag{3}$$

TABLE II
SEMATECH DATA

	Thermal cycles	L_{DEF} (H)	R* (Ω)	R_{oxyf} (Ω)	C_{oxyf} (F)	β	α	ɣ	RMS
Die 1	0	1.13E-08	13448	539.94	0	64.495	0	0.004471	0.013791
	1000	5.35E-08	13211	4982.6	1.45E-15	119.03	0.03633	0.033024	0.005428
	2000	5.00E-08	11088	4584.8	1.55E-15	111.5	0.039766	0.039624	0.005912
	5000	9.80E-09	4631.3	2326.6	0	56.495	0.27213	0.07063	0.003429
Die 2	0	7.07E-08	851.5	11424	2.86E-16	104.2	0.26592	0.1735	0.001687
	1000	4.22E-08	5956.9	3817.6	1.61E-15	95.251	0	0.066364	0.008296
	2000	3.56E-08	3965.2	2946.5	1.91E-15	85.048	5.50E-10	0.080818	0.008919

TABLE III
ESTIMATED SLOPES AND INTERCEPTS r^* AND γ AS A FUNCTION OF THERMAL CYCLES FOR TWO REPRESENTATIVE DIES FROM EACH SAUCE

Fab	(x,y)	a_0 (Ω)	a_1 (Ω/cycle)	b_0	b_1 (1/cycle)
CEA-LETI	(4,2)	193(38)	1.18(0.29)	0.152(0.007)	-2.03(0.54) x 10^{-4}
CEA-LETI	(4,10)	174(36)	0.039(0.19)	0.152(0.008)	-7.7(4.2) x 10^{-5}
SEMATECH	(-6,11)	1.43(0.07) x10^4	-1.87(0.25)	0.013(0.006)	1.21(0.23) x 10^{-5}
SEMATECH	(-1,9)	2.0(2.6) x 10^3	1.6(2.1))	0.153(0.045)	-4.6(3.5) x 10^{-5}

where c_i is the number of thermal cycles, $\epsilon\_(R_i)$ is the unobserved measurement error, and a_0 and a_i are model parameters to be determined. Similarly, we model the observed value of γ, (γ_i)^, as

$$\widehat{\gamma_i} = b_0 + b_1 c_i + \epsilon_{\gamma,i} \tag{4}$$

where $\epsilon_{\gamma i}$ is the unobserved measurement error and b_0 and b_i are model parameters to be determined by ordinary least squares (OLS).

Fig. 6 shows the variation of estimated R^* and estimated γ. Estimated R_{DEF} [see (1)] depends on both the number of thermal cycles and the location of the die on the source wafer. In Table III, we list the model parameters and their standard uncertainties in parenthesis for (3) and (4) models, which predict R^* and γ as a function of number of cycles for both device types (taken from the center (green circles) and toward the edge (red squares) of the 300-mm wafer, respectively). For instance, 193(38) conveys that parameter estimate and its associated standard uncertainty are 193 and 38, respectively. Inspection of the table shows the impact of local chemistry on the electrical properties of the die.

III. DISCUSSION

We attribute the spatial variation of R_{oxf} and C_{oxyf} shown in Fig. 4 to the spatial variation of $|S_{21}|$. In general, as the number of thermal cycles increases, insertion loss increases and hence $|S_{21}|$ decreases, due in part to changes in the physicochemical properties of the materials used for the construction of the devices studied. We have shown elsewhere that these changes could be in either the isolation dielectric and/or in the coaxial conducting metal (i.e., Cu) fill in the TSV [28]. Typical stress in SACVD O_3-TEOS film is about 85-MPa compressive [29] but becomes tensile at higher temperatures, as the film condenses and loses water.

As discussed in Section I, the electrical isolation dielectric of the core metal conductor in the "via-last" TSVs process is typically deposited at low temperatures [5], in a single wafer processor where the wafer may be held and heated on a ceramic susceptor. The temperature uniformity control across large susceptors is challenging. The exact thermal profile depends on the configuration of the heater within the susceptor body; the center-to-edge temperature range increases with increasing target temperature (i.e., power of the ceramic heater). Furthermore, the substrate is held onto the susceptor by either mechanical or electrostatic clamps, and the clamping mechanism contributes to the thermal profile of the susceptor [27], [30]. The local physicochemical properties of the deposited material are closely related to the local substrate temperature during deposition and its thermal history [9]. For an optimized deposition process, the temperature range across a 300-mm wafer should be less than 5%.

In both device types studied in this work, the quality and chemistry of SiO materials differ across the wafer, due to the atomistic-level structure of the silicon oxide, which depends on the local substrate temperature and or the composition of the reactant gases over the local area. As we have shown previously, the spatial distribution of acoustic impedance and other physicochemical properties of the SACVD silicon oxide films (e.g., Young's modulus) depends on the local silanol concentration [13]. In addition, "as-deposited" SiO dielectric also contains substantial amounts of water-related species [31], which affects the mechanical stress hysteresis in the material during thermal cycling [32], [33].

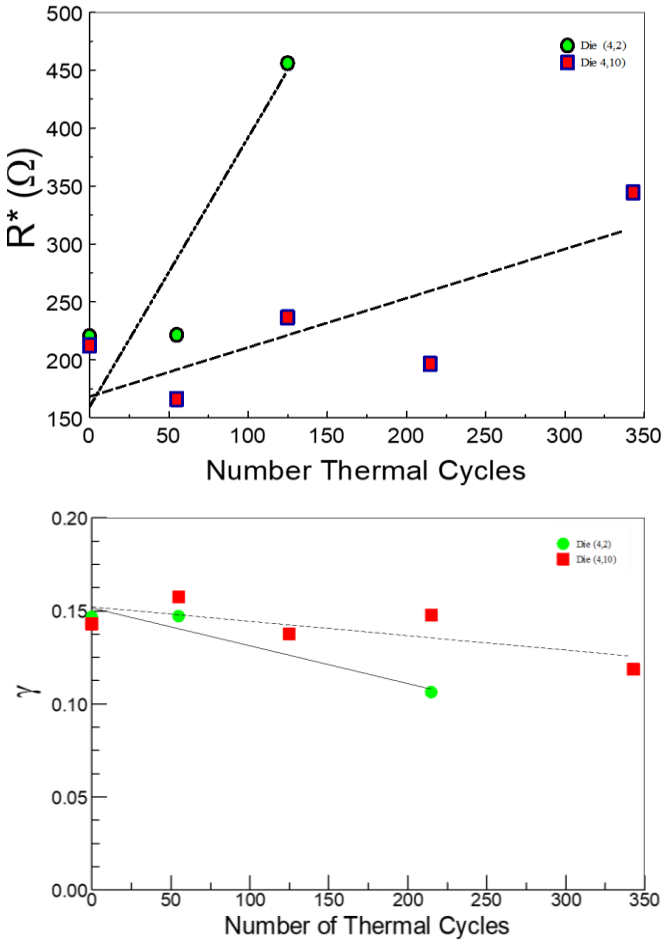

Fig. 6. Variation of estimates of $R*$ and γ as a function of thermal cycles for two representative CEA-LETI dies (edge die and center die 2). The data clearly show the impact of local chemistry on the electrical properties of the die.

We believe that the changes we describe here are more related to changes in the dielectric than to the metal fill. However, while we cannot totally discount contributions from the metal fill toward the improved device performance with thermal cycling, the data and analyses presented in this work are more consistent with dielectric material transformation with thermal cycling as the main contributor to the microwave insertion loss. Specifically, the RF insertion losses we observe in this work are attributed to the reorientation of electrically active defects, e.g., SiOH dangling bonds and water molecules. These perturbations result in energy being sorted and dissipated because the complex dielectric permittivity $\varepsilon^* = \varepsilon' - i\varepsilon''$ components become frequency-dependent when dipoles can no longer stay in-phase with the applied field.

IV. Conclusion

Microwave insertion loss ($|S_{21}|$) spectra were used to study defect evolution in prototype TSV-enabled two-level stacked dies fabricated by two different organizations, SEMATECH and CEA-LETI. We developed a statistical empirical model for measured frequency-dependent insertion loss ($|S_{21}|$) that accounts for thermal annealing effects. The model parameters were determined with a stochastic optimization implementation of the Levenberg–Marquard method. The frequency-dependent changes in the electrical characteristics of the interconnect were attributed to the polarization of defects such as silanol (Si-OH) and other dangling bonds at the Si–SiO interface between the silicon substrate and the lateral isolation silicon oxide, while the changes in the polarizations are traceable to thermal-induced chemical changes in the isolation dielectric. The data also suggest that the evolution of the "chemical defects" inherent in the "as-manufactured" products may be responsible for some of the signal integrity degradation issues and other early reliability failures observed in TSV-enabled 3-D interconnected devices.

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