Heterojunction tunnel triodes based on two-dimensional metal selenide and three-dimensional silicon

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Abstract. Low power consumption in the static and dynamic modes of operation is a key requirement in the development of modern electronics. Tunnel field-effect transistors with direct band-to-band charge tunnelling and steep-subthreshold-slope transfer characteristics offer one potential solution. However, silicon and III–V heterojunction-based tunnel field-effect transistors suffer from low on-current densities and on/off current ratios at sub-60 mV decade^{-1} operation. Tunnel field-effect transistors based on two-dimensional materials can offer improved electrostatic control and potentially higher on-current densities and on/off ratios. Here we report gate-tunable heterojunction tunnel triodes that are based on van der Waals heterostructures formed from two-dimensional metal selenide and three-dimensional silicon. These triodes exhibit subthreshold slopes as low as 6.4 mV decade^{-1} and average subthreshold slopes of 34.0 mV decade^{-1} over four decades of drain current. The devices have a current on/off ratio of approximately 10^6 and an on-state current density of 0.3 μA μm^{-1} at a drain bias of –1 V.

Power dissipation is a central problem in modern, highly scaled nanoelectronics [1–3]. The fundamental limit on the subthreshold slope (SS) in thermionic devices involving single-band transport – such as in metal–oxide–semiconductor field-effect transistors (MOSFETs) – restricts further scaling in power consumption and supply voltage, as well as increases the power density and dissipation in MOSFET-based

circuits [4–6]. The limitation on SS is set at $m \times \ln(10) \times kBT/q$ – around 60 mV decade^{-1} at room temperature for an ideal MOSFET [7] – where k_B is the Boltzmann constant, m is the body factor (equal to 1 for an ideal transistor), q is the elementary charge and T is the temperature. This is due to the thermal nature of carrier injection at the metal–semiconductor contact, which puts a lower limit on the power consumed per switching cycle. Tunnel field-effect transistors (TFETs) – whose operation relies on band-to-band tunnelling (BTBT) rather than thermionic emission – can potentially overcome this limit [8–10]. However, TFETs are limited by low on-current densities and on/off ratios at the sub-60 mV decade^{-1} operation [3,8].

Two-dimensional (2D) semiconductors offer new opportunities in TFET device design because their atomically thin structure permits strong electrostatic control [9,11–14]. This electrostatic control allows smaller SS values in TFETs and may also permit higher on/off ratios by maximizing the on-current density. In addition, 2D van der Waals materials are naturally self-passivated, which allows them to be easily embedded between metal gates and thin dielectrics, leading to strong electrostatic modulation [15,16]. But unlike three-dimensional (3D) bulk materials that have well-established doping schemes, stable and complementary doping in 2D materials remains a challenge [17,18]. TFET device structures normally comprise p–i–n homo- or heterojunctions where the intrinsic layer sees strong electrostatic modulation and the shrinkage in lateral dimensions permit direct BTBT transport. Therefore, combining 2D materials with 3D bulk semiconductors offers a potentially valuable approach [19–21] for developing TFET architectures. In this Article, we report gate-tunable heterojunction tunnel triodes (HJ-TTs) that are based on van der Waals heterostructures formed from n-type 2D InSe and heavily p-doped (p^{++}) 3D silicon. The devices overcome the thermionic limitation of conventional MOSFETs and offer a minimum SS of 6.4 mV decade^{-1} and an average SS of 34 mV decade^{-1} over four decades of drain current. They also exhibit a large on-current density of $I_{p\text{-}Si} = 0.3$ μA μm^{-1} at a drain bias of $V_{p\text{-}Si} = -1$ V. Our work is a demonstration of all-solid-state low-power logic devices based on 3D silicon and 2D InSe [22].

Device fabrication and architecture

We begin by etching square windows on the surface of SiO2/p^{++}Si substrates to expose the lower p^{++}Si layer. We then transfer mechanically exfoliated 2D InSe flakes of a few-layer thickness onto the exposed surface (Fig. 1a). The γ-phase crystalline structure is sketched in Fig. 1a (cross-sectional view). Microfabrication processes (Methods) are used to make the Ti/Au metal electrodes and AlO_x gate dielectric. An optical micrograph of the InSe/p^{++}Si 2D/3D HJ-TTs along with control of the top-gated MOSFETs is shown in Fig. 1b. The cross-sectional architecture of the device is characterized by scanning transmission electron microscopy (STEM) (Fig. 1c–e). A 2-nm-thick native silicon oxide (SiO_x), which was formed during the InSe transfer process, is revealed between 2D InSe and 3D Si (Fig. 1d, Supplementary Fig. 1 and Supplementary Section 1). The polytype structure of the InSe layer is identified as the phase with selected area electron diffraction (Supplementary Fig. 2) and atomic-resolution high-angle annular dark-field (HAADF) STEM analyses (Fig. 1f). Although ultrathin amorphous SiO_x exists between the InSe and p^{++}Si, it is highly conductive with resistance of only ~25 Ω for the lateral dimensions of our devices (Supplementary Fig. 3). Furthermore, the native silicon oxides can be reduced with surface dangling bonds passivated by forming Si–H bonds via a hydrogen termination treatment. There are various other strategies for Si passivation with deuterium instead of the regular isotope of hydrogen or with various other small organic groups such as methyl or other alkyl groups [23–26], which may be adopted in future works. To understand the details of the electronic structure of InSe crystals, we have performed photoemission and Hall measurements (Supplementary Fig. 4, Supplementary Table 1 and Supplementary Section 2) to determine the carrier density and band alignment. Using these values combined with the known gap value of γ-InSe, we have simulated band diagrams of unintentionally n-doped InSe/p^{++}-Si HJ-TTs, as shown below.

Performance characteristics

We perform room-temperature electrical characterizations of the InSe/Si 2D/3D HJ-TTs in a three-terminal transistor configuration with the n-InSe terminal grounded and p^{++}Si as the drain. The device exhibits a minimum SS value of 6.4 mV decade^{-1} with a current on/off ratio of 10^6, as well as a large on-state current

density of $I_{p\text{-}Si}$ = 0.3 μA μm^{-1} at an applied $V_{p\text{-}Si}$ = −1 V (Fig. 2a). We note that this phenomenon is not observed in a one-off device and has been reproducible in other 2D/3D devices (Supplementary Fig. 5). Figure 2b shows the zoomed-in transfer characteristics with VG changing from −6.00 to −5.82 V, showing the steepness in the context of a magnified x axis. It is worth noting that a gate-voltage change of mere 180 mV modulates the output current by over five orders of magnitude. Further, compared with the drain current, the gate-leakage current shows negligible magnitude. Therefore, I_{gate} leakage only leads to very minor fluctuations in the off-state current (Fig. 2b, dashed square) and has almost no influence on the signal current in the subthreshold or above-threshold region. A detailed TCAD simulation analysis on the transfer/output characteristics with gate-leakage current is shown in Supplementary Fig. 6 (Supplementary Section 3). Figure 2c shows the statistical SS versus output $I_{p\text{-}Si}$ for six representative InSe/Si HJ-TTs. Note that all these InSe/Si devices show SS below 60 mV $decade^{-1}$. To further illustrate the carrier transport in 2D/3D HJ-TTs, we provide Sentaurus technology computer-aided design (TCAD) simulations here, with detailed parameters and physics model additionally provided in Supplementary Table 2. The ultrathin SiO_x layer is not considered in the TCAD simulation for simplicity because it has limited influence on the electrical performance with a minor shift in the threshold voltage (Supplementary Fig. 7). The simulated $I_{p\text{-}Si}$–V_G characteristics show qualitative resemblance to the experimental plots with an average SS of less than 10 mV $decade^{-1}$ and a current on/off ratio of up to 10^9 (Fig. 2d,e). Despite the strong qualitative agreement, the simulated InSe/Si HJ-TTs show quantitatively superior electrical performance in terms of the current compared with our physically made experimental devices. This is reasonable since no trap charges at either interface have been considered in the TCAD simulations.

To further understand the electrostatics of the InSe/Si HJ-TTs, the TCAD-simulated electric-field contour and electron-density plots are shown in Fig. 2f. In the on state (V_G = 0.8 V and $V_{p\text{-}Si}$ = −0.5 V), the top-gated electric field combined with the drain-induced electric field are mainly in the 2D InSe region, with a total electric field of 1–2 MV cm^{-1} (Fig. 2f–i). The strong electric field bends the energy band of the InSe/Si heterojunction, leading to overlapping between the valence band of Si and conduction band of InSe for BTBT transport. The electron-density contour (Fig. 2f(iii)) shows a high electron density of 10^{20} cm^{-3} in

the InSe channel in the on state. In the off state (V_G = −0.8 V and $V_{p\text{-}Si}$ = −0.5 V), the total electric field is small (Fig. 2f(ii)) with a low electron density across the InSe channel due to the blocked BTBT transport (Fig. 2f(iv)). The device polarity and threshold voltage can be further modulated by doping concentration and type ($p^{++}/n^{-}/n^{+}$ or $n^{++}/p^{-}/p^{+}$), channel material and even device geometry (vertically stacked van der Waals structures) [27].

Charge transport mechanism

The equilibrium band diagrams with known electron affinities (2D InSe, 4.60 eV; 3D Si, 4.01 eV) and carrier concentrations indicate that the InSe/Si form a type-II junction with 0.59 eV valence-band offset that is closely matched with the photoemission results (Supplementary Fig. 4). To further evaluate the electrical characteristics of InSe/Si HJ-TTs, we compare with control MOSFETs made on the same InSe crystal as the junction shown in Fig. 1b. The detailed TCAD simulation and analysis of the control InSe MOSFETs are shown in Supplementary Fig. 8. We observe clear and stark differences between the two devices made from the same flake (crystal), further suggesting that our heterojunction device indeed has a different charge transport mechanism, namely, BTBT. There are three clear differences observed between the control InSe MOSFETs and InSe/Si 2D/3D HJ-TTs: the current density of InSe MOSFETs is higher than the InSe/Si HJ-TTs; the average SS in the transfer characteristics of InSe MOSFETs is more than three times larger for the same oxide thickness (Fig. 3a,b); and InSe MOSFETs have linear output characteristics, whereas InSe/Si HJ-TTs clearly show rectifying output with gate-tunable rectification ratios (Fig. 3c,d).

First, the transfer characteristics when compared over the same scale (Fig. 3a) show that the InSe MOSFETs (blue) are less steep in the subthreshold region compared with the InSe/Si HJ-TTs (red). Further, it is also clear from the same plot that the InSe MOSFETs have higher current density in the on state as opposed to InSe/Si HJ-TTs. Interestingly, both devices show very flat on-state characteristics in the semi-log scale, which further suggests that the InSe/Si heterojunction can provide large swings in current with small swings in voltage and is suitable for low-voltage operation. Furthermore, we find that the InSe MOSFETs have an SS value that hits a minimum at ~100 mV decade^{-1} and rapidly rises with both increase or decrease in

current. In contrast, the InSe/Si HJ-TTs show consistently small SS value ranging from 6.4 to 60.0 mV decade^{-1} – a change of over four orders of magnitude in drain current with an average of 34.0 mV decade^{-1}. These average SS values have been derived using the data points of drain current in the 10^{-12} to 10^{-8} A μm^{-1} range. This is because the 2D InSe used in our devices is unintentionally n doped and near intrinsic and therefore likely to show p-type conduction on a further increase in VG in the negative direction (Fig. 3a, blue curve (from −4 to −6 V)). We also note that a similar behaviour has been obtained in intrinsic WSe2/p^{++}Si HJ-TTs (Supplementary Fig. 9). Therefore, although the device is qualitatively similar to the one described in another work [28], there are important differences between these prior works and the present report. For instance, BTBT requires not only clean interfaces but 'electronically' clean band edges. For sulfide systems, this is difficult to achieve and hence MoS_2 devices are n doped in most cases. This is notably reduced in selenide systems, which are easier to grow with near-intrinsic quality or minimal unintentional doping.

Another notable difference between InSe MOSFETs and InSe/Si HJ-TTs is in the output characteristics. InSe MOSFETs with ohmic contacts show highly symmetric current–voltage (I–V) characteristics above the origin with early signs of saturation (Fig. 3c). These characteristics are representative of an n-MOSFET with increasing conductance (slope) and hence current as a function of gate voltage from −6 to 6 V, in agreement with the transfer characteristics shown in Fig. 3a. Even when magnified to small values of voltage (Fig. 3c, inset), these I–V curves remain linear, suggesting the ohmic nature of the contacts. In contrast, the InSe/Si HJ-TTs clearly demonstrate rectifying output characteristics (Fig. 3d and Supplementary Fig. 10). Furthermore, with increased $-V_{p\text{-}Si}$, the output current $I_{p\text{-}Si}$ shows Zener breakdown because of the reverse-bias-induced overlap between the valence band of Si and conduction band of InSe (Fig. 3d,e). This observation is like that of several prior reports of gate-tunable p–n diodes based on 2D materials [28–30]. To further understand the rectifying $I_{p\text{-}Si} - V_{p\text{-}Si}$ characteristics in InSe/Si HJ-TTs, Sentaurus TCAD is once again used to systematically investigate the output characteristics (Fig. 3e), energy-band diagrams (Fig. 3f) and the corresponding transfer characteristics (Fig. 3g). More details on InSe/Si HJ-TTs simulation are provided in Supplementary Figs. 11–13.

The 2D/3D HJ-TTs are p–n junctions with p^{++}Si/n-InSe heterostructures. In this scenario, the gate and drain voltages can both effectively modulate the energy bands. Since the p^{++}Si part is highly conductive, the applied drain voltage from the p^{++}Si or n-InSe part mainly introduces a voltage drop (that is, band bending) on the n-InSe. Note that the drain bias is always competing with the gate bias. Thus, the combined potential difference in the channel modulates the energy bands. (1) In the reverse-bias region ($V_{p\text{-}Si}$, 0 to −0.5 V), the drain bias of $V_{p\text{-}Si}$ = −0.5 V can push the conduction-band minimum (CBM) of n-InSe below the valence-band maximum (VBM) of p^{++}Si, resulting in BTBT; however, the negative gate voltage (V_G = −0.8 V) pushes the E_f (Fermi-level) value of n-InSe to the mid-gap region. Therefore, the CBM of n-InSe is still above the VBM of p^{++}Si (Fig. 3f–i, black line), and an overlap in the energy window cannot be created for electrons to tunnel from the filled valence-band states of p++Si into the empty conduction-band states in n-InSe. As shown in Fig. 3e,g–i, the current ($I_{p\text{-}Si}$) is low for $V_{p\text{-}Si}$ = −0.5 V and V_G = −0.8 V. However, for $V_{p\text{-}Si}$ = −0.5 V and V_G = 0.8 V, the positive gate voltage (V_G = 0.8 V) further pulls up the E_f value of n-InSe close to its CBM. Therefore, the CBM of n-InSe is below the VBM of p^{++}Si (Fig. 3f–i, red line) in this case, and an energy window can be created for electrons to tunnel from the filled valence-band states of p^{++}Si into the empty conduction-band states in n-InSe, leading to high Ip-Si.

Note that the Zener breakdown occurs with increasing $-V_{p\text{-}Si}$, which has been observed in both TCAD-simulated and physical (experimentally made) InSe/Si HJ-TTs (Fig. 3d–e). This further demonstrates the overlap between the valence band of Si and conduction band of InSe in the band alignment. The same analysis can also be applied to the case of $V_{p\text{-}Si}$ = −0.1 V (Fig. 3f(ii),g(ii)). (2) In the forward-bias region ($V_{p\text{-}Si}$, 0–0.5 V), the negative gate voltage (V_G = −0.8 V) pushes the E_f value of n-InSe to its mid-gap value. The increased forward bias of $V_{p\text{-}Si}$ further pulls up the CBM of n-InSe. Therefore, the potential barriers for holes in p^{++}Si thermally injected into n-InSe and electrons in n-InSe thermally injected into the p^{++}-Si are low with $V_{p\text{-}Si}$ = 0.5 V and V_G = −0.8 V (Fig. 3f(iv), red line). For a positive gate voltage (V_G = 0.8 V), the CBM of n-InSe is pushed below the VBM of p^{++}-Si. However, the positive drain bias of $V_{p\text{-}Si}$ pulls up the CBM of n-InSe slightly above the VBM of p^{++}-Si. Therefore, the potential barriers for holes in p^{++}Si thermally injected into n-InSe and electrons in n-InSe thermally injected into p^{++}Si are both high for $V_{p\text{-}Si}$

= 0.5 V and V_G = 0.8 V (Fig. 3f(iv), black line). In conclusion, the drain current $I_{p\text{-}Si}$ for $V_{p\text{-}Si}$ = 0.5 V and V_G = −0.8 V is slightly higher than that for $V_{p\text{-}Si}$ = 0.5 V and V_G = 0.8 V (Fig. 3g(iv), green line).

Furthermore, for gate voltages of V_G = 0.8 and 0.6 V, the negative differential resistance was observed with a small forward bias, for example, $V_{p\text{-}Si}$ = 0.1 V, further indicating the overlap between the valence band of Si and conduction band of InSe (Fig. 3f(iii),g(iii)). Our study and other reports [31], however, did not observe an obvious negative differential resistance in the forward region, which is probably due to Fermi-level pinning or high thermal-injection probability at room temperature. Furthermore, due to the asymmetric 2D/3D heterostructure, the I–V characteristics highly depend on the direction of the applied drain biases. By switching the drain regions (3D p^{++}Si as the drain or 2D n-InSe as the drain), the output characteristics are not exactly mirrored and flipped along the y axis, which has been systematically discussed in Supplementary Figs. 11–13 and Supplementary Section 3. We note that the gate oxide thickness was fixed at 5 nm for speeding up the simulations and gate dielectric permittivity was fixed at $9\varepsilon_0$ (where ε_0 is the permittivity of vacuum). In addition, no trap charges were assumed in the simulations. This results in different gate-voltage ranges for the simulated versus experimentally measured plots.

To further prove the differences between the charge transport mechanism of InSe MOSFETs and InSe/Si HJ-TTs, we perform temperature-dependent electrical characterizations (Fig. 4). Figure 4a shows the $I_{p\text{-}Si}$–V_G characteristics of the heterojunction device at various temperatures for $V_{p\text{-}Si}$ = −2 V. The threshold voltage for BTBT appears to clearly shift right with reducing temperature. In addition, the magnitude of the on-current plateau also appears to reduce with reducing temperatures. This suggests that the transport in these devices is complex and varies as a function of gate voltage/position of the Fermi level in 2D InSe. A decrease in the on current as a function of temperature suggests some thermal barrier in the device. This thermal barrier could arise from multiple reasons ranging from imperfect metal/InSe contacts to hopping transport in the non-junction part of 2D InSe (refs. 32,33). Another possible mechanism to explain this is trap-assisted tunnelling, where electrons first tunnel into a trap within the bandgap close to the conduction band, from which they are thermally excited into the conduction band. The Bridgman-grown InSe crystals [34,35] possess interstitial atoms, vacancies and unintentional impurities. To understand this temperature-

activated transport in more detail, we present an Arrhenius plot analysis (Fig. 4b) that shows plots made for different gate voltages. We observe an activation energy of 0.2 eV extracted for the subthreshold region. Further, this activation energy changes from 0.20 to 0.05 eV as the gate voltage changes from −5.36 to −4.00 V, suggesting that the transport is weakly dependent on temperature for high doping density (V_G = −4.00 V). Given the steep drop in current and lack of ability to obtain currents below 10^{-11} A, it is difficult to ascertain the nature of temperature dependence in the subthreshold region. However, for thermionic transport in conventional MOSFETs, it is well known that the SS linearly depends on the temperature. On plotting the SS slope as a function of temperature, we find that the slope is nearly independent of temperature, in stark contrast with InSe MOSFETs that show a clear dependence on temperature with an m factor of ~2 (Fig. 4c and Supplementary Fig. 14). The m factor is further confirmed by capacitance–voltage characterizations (Supplementary Fig. 15 and Supplementary Section 4). This provides strong evidence that the observed transport – at least in the steep-SS range of our InSe/Si HJ-TTs – is dominated by BTBT. However, given that the on current is also reducing with temperature, further theoretical and experimental studies are necessary to confirm the exact mechanism of transport away from the SS region.

Benchmark of device performances

Finally, given the steep SS of our devices combined with the large on/off ratio, we perform the benchmark of our devices with earlier studies on select steep-SS devices operating at room temperature. We compare our devices on three important metrics: SS versus drain current density; drain current at SS = 60 mV decade^{-1} versus average SS; and current at SS = 60 mV decade^{-1} versus off current in the sub-60 mV decade^{-1} region. Figure 5a shows the SS values as a function of drain current for various steep-SS TFET devices and negative-capacitance (NC) FETs [31,36–39]. The SS versus IDS for our device is extracted from the transfer curves (Fig. 2a). The comparison data clearly indicate that InSe/Si HJ-TTs have simultaneously small SS, high I_{60} (current where SS becomes 60 mV decade^{-1}) and current density more than two orders of magnitude larger than that obtained in MoS_2/Ge TFETs. The I_{60} value is the chosen metric since the current saturates soon after that and would be the point of operation of the on state of the device. Though

some homo- and heterojunction devices show slightly higher $SS_{average}$ values (Fig. 5b) or I_{60}/I_{off} ratios (Fig. 5c), the InSe/Si heterostructures still exhibit dramatic advantages in terms of easy integration with silicon technology and a suitable bandgap in all-solid-state device architecture. Furthermore, we propose that this current density could be raised even further by removing the interfacial silicon oxide layer, as a higher on-state current could improve the gate-to-source capacitance. Likewise, shrinking device dimensions and use of a graphene top contact can also help improve the I_{60} value.

Conclusions

We have reported BTBT HJ-TTs that are based on the van der Waals integration of 2D metal selenide on 3D silicon. Due to the atomically thin nature of InSe and fixed doping profile in bulk silicon, energy bands can be effectively modulated by a capacitively coupled gate, enabling the strong modulation of band alignment resulting in direct BTBT. The resulting HJ-TTs exhibit a minimum SS of 6.4 mV decade^{-1} with an average SS of 34.0 mV decade^{-1} over four decades of drain current at room temperature. The devices also exhibit a high current on/off ratio of up to 10^6 and on-state current density of 0.3 μA μm^{-1} at $V_{p\text{-}Si} = -1$ V. Our results suggest that 2D/3D integration is a viable path for the development of ultralow-power and highly scaled logic switches. Furthermore, considering that indium has a low solubility in silicon40 and InSe is lattice matched to silicon[111] (refs. 41,42), our approach potentially offers a route to large area growth and scaling of InSe/Si HJ-TTs for next-generation digital logic.

Methods

Device fabrication

All the devices were fabricated using electron-beam lithography (EBL) using a three-step process. Electron-beam resist (polymethyl methacrylate) was first spin coated onto the SiO2/p^{++}Si substrate (WaferPro, B doping with resistivity of 0.005 Ω cm) capped with a 50-nm-thick SiO_2 layer grown using a dry oxidation process. Then, a square pattern (size, 10×10 μm^2) was defined by EBL (step 1), followed by a development

process. After that, the SiO2/p^{++}Si substrate was immersed into a buffered oxide etch solution for about 1 min to etch the SiO_2 layer, exposing the lower p^{++}Si layer. Finally, the rest of the resist was removed by acetone, and the as-prepared substrate was immediately transferred to a glove box to avoid the reoxidation of the exposed p^{++}Si window. In the glove box, a few-layer 2D InSe flake was physically transferred onto the exposed p^{++}Si window. The flake was exfoliated using a tape from the bulk crystal and then stuck onto a polydimethoxysilane stamp (GelPak, A4). The metal electrode patterns of the devices were then defined by EBL (step 2), followed by metal deposition and lift-off processes. After that, we use the atomic layer deposition method to deposit a 10-nm-thick AlO_x top-gated dielectric on 2D InSe. The top-gated electrode was finally defined by EBL (step 3), metal deposition and lift-off processes.

Growth and characterization of InSe crystals

InSe single crystals were grown by the vertical Bridgman method using a non-stoichiometric polycrystalline $In_{1.04}Se_{0.96}$ charge. The n- and p-type doping was achieved by adding Sn (2 at.%) and Zn (as ZnSe at 0.3 at.%), respectively, during InSe charge synthesis. The InSe melt was equilibrated at 720 °C for several hours and then the ampoule was translated across a temperature gradient at a rate of 0.5 mm h^{-1}.

Electrical characterization

The electrical measurements for all the devices were performed by a Lake Shore probe station combined with a Keithley 4200 semiconductor analyser. All the measurements were carried out at room temperature, unless noted otherwise in the figures.

Simulations

The TCAD device simulations were performed using Synopsys Sentaurus TCAD device package. Additional details for the simulations are provided in the Supplementary Information.

Electron microscopy characterization

The electron-transparent cross-section sample was prepared with an FEI Nova NanoLab 600 DualBeam (scanning electron microscope/focused ion beam) system. An FEI Titan 80-300 probe-corrected scanning

transmission electron microscope/transmission electron microscope operating at 300 keV was employed to acquire the selected area electron diffraction patterns, scanning transmission electron microscope images and scanning transmission electron microscope images and scanning transmission electron microscope energy-dispersive X-ray spectroscopy linescans.

Data availability

The data that support the conclusions of this study are available from the corresponding authors upon reasonable request. Source data are provided with this paper.

Code availability

Any codes used in this study are available from the corresponding authors upon request.

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Author contributions
D.J. and J.M. conceived the idea/concept. D.J. directed the collaboration and execution. J.M. fabricated all the devices with assistance from B.S. and measured them with the assistance of X.L. Simulations were done by C.L., J.W., Y.G. and W.H. Electron microscopy and cross-sectional cutting of the devices was performed by H.Z. InSe crystals were grown by S.K. A.V.D. supervised the crystal synthesis, Hall measurements and electron microscopy. N.G. and T.B. performed the photoemission spectroscopy measurements. J.M., C.L. and D.J. co-wrote the manuscript with contributions from all the authors.

Competing interests
D.J. and J.M. have filed an invention disclosure based on this work. The other authors declare no competing interests.

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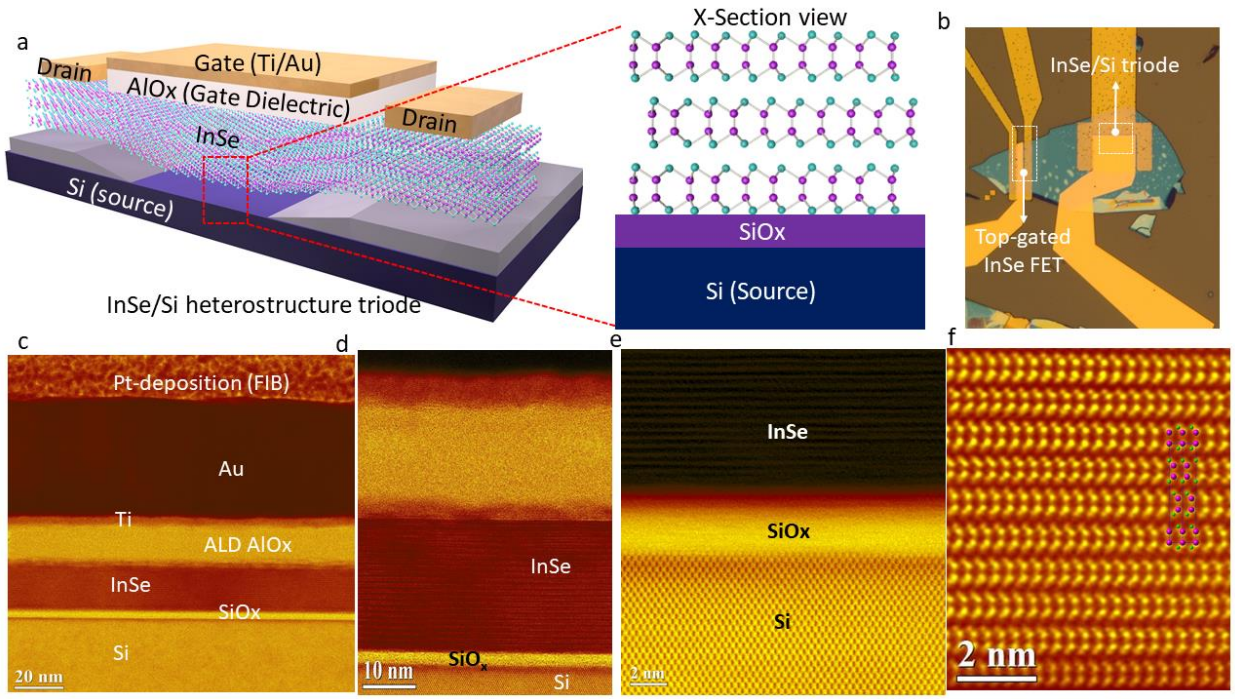

Fig. 1. Structure and characterization of 2D/3D heterojunction tunnel triode. a, Schematic of an n-InSe/p^{++}Si 2D/3D HJ-TT with 3D p^{++}Si, 2D n-InSe, AlO_x gate dielectric and Ti/Au metallic electrode vertically stacked together. **b**, Optical micrograph of a representative 2D/3D HJ-TT and top-gated n-InSe MOSFET. Scale bar, 10 μm. **c**, Bright-field STEM image showing the cross-sectional architecture of the n-InSe/p++Si HJ-TTs. Scale bar, 10 nm. **d,e**, Zoomed-in images showing the layered crystalline structure of 2D InSe **(d)** and a 2-nm-thick amorphous native SiO_x between 2D InSe and single-crystalline 3D p^{++}Si (e). Scale bars, 5 nm (d), 2 nm **(e)**. **f**, Atomic-resolution HAADF-STEM image overlapped with a projected atomic model, showing a good match with the γ-InSe polytype. Scale bar, 1 nm.

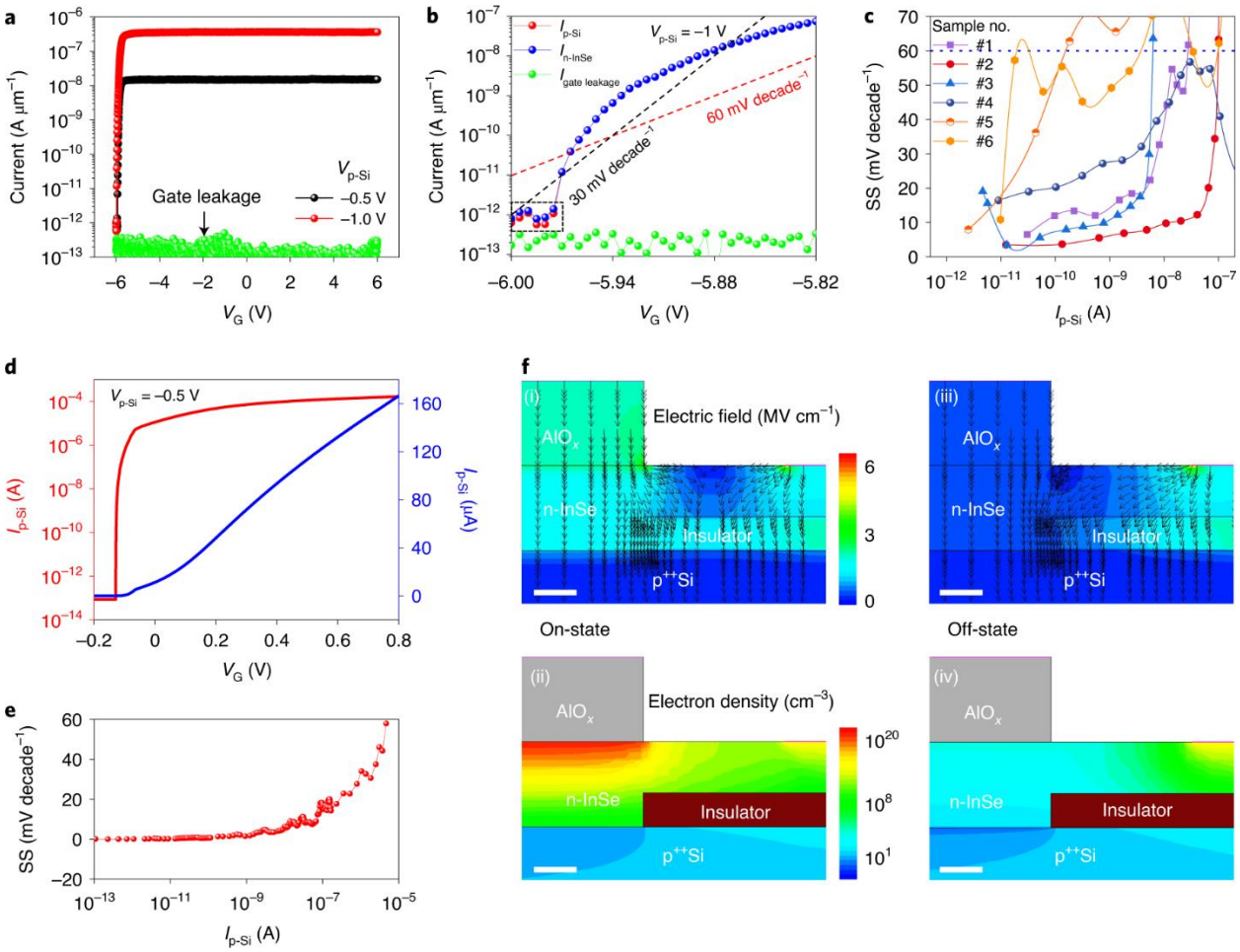

Fig. 2: Room-temperature electrical characteristics of InSe/Si 2D/3D HJ-TTs. a, Logarithmic-scale $I_{p\text{-}Si}$–V_G transfer characteristics of InSe/p^{++}Si HJ-TTs measured at room temperature with applied $V_{p\text{-}Si} = -0.5$ V (black) and $V_{p\text{-}Si} = -1.0$ V (red) plots. The minimum subthreshold swing is 6.4 mV decade^{-1}. The green line represents a gate-leakage current of ~10^{-13} A μm^{-1}. b, Zoomed-in transfer characteristics from the data in a ($V_{p\text{-}Si} = -1$ V), showing the magnitude of $I_{n\text{-}InSe}$ (red spheres), $I_{p\text{-}Si}$ (blue spheres) and $I_{gate\ leakage}$ (gate-leakage current) in green spheres in V_G range from −6.0 to −5.8 V. The red and black dashed lines are references for indicating the 60 and 30 mV decade^{-1} for the SS. The dashed black box indicates a very minor variation between $I_{p\text{-}Si}$ and $I_{n\text{-}InSe}$ because of $I_{gate\ leakage}$ in the off state. c, SS versus output current $I_{p\text{-}Si}$ of six representative InSe/Si HJ-TTs showing reproducibility of the effect. d, Predicted logarithmic-scale (red) and linear-scale (blue) transfer characteristics of InSe/Si HJ-TTs using the Sentaurus TCAD simulator. e, SS versus output current $I_{p\text{-}Si}$ for the TCAD-simulated InSe/Si HJ-TTs from d. f, TCAD-simulated electric-field contour across the InSe/Si HJ-TTs in the on (i) and off (iii) state. The electron-density profile for the simulated InSe/Si HJ-TTs in the on (ii) and off (iv) state. Scale bar, 2.5 nm.

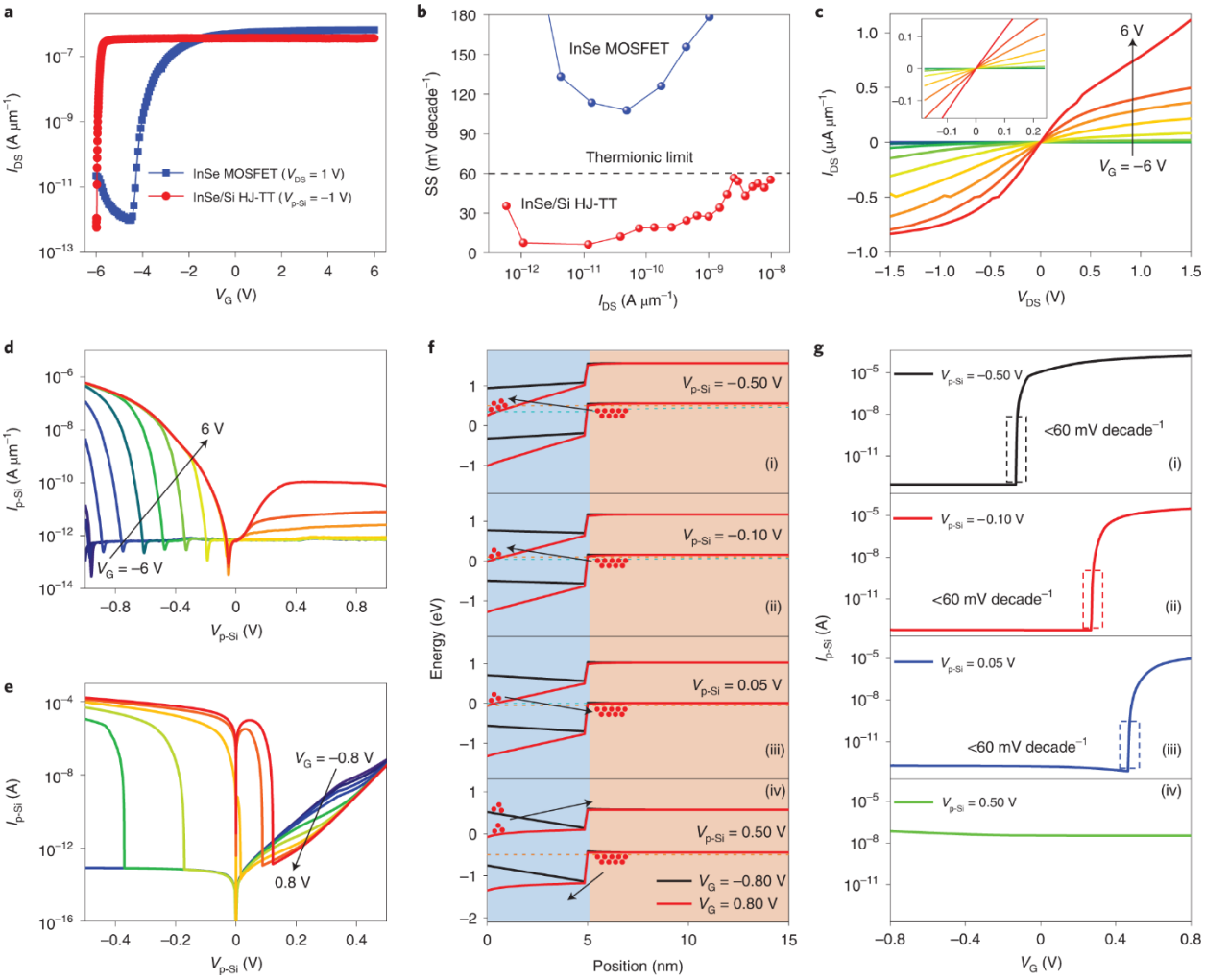

Fig. 3: Room-temperature electrical characteristics of InSe/Si 2D/3D HJ-TTs, control 2D InSe MOSFETs and TCAD-simulated devices. **a**, Comparison of logarithmic-scale I_{DS}–V_G transfer characteristics of InSe MOSFETs and InSe/Si HJ-TTs. **b**, Subthreshold swing comparison of InSe/Si HJ-TTs with control InSe MOSFETs. The minimum SS value of the control InSe MOSFETs is ~100 mV decade^{-1}. The InSe/Si HJ-TTs show sub-60 mV decade^{-1} over four decades of drain current. The black dashed line represents the thermionic limit of 60 mV decade^{-1}. **c**, Linear-scale I_{DS}–V_{DS} output characteristics of the control InSe MOSFETs with V_G varying from −6 to 6 V in 1 V steps. The inset shows a zoomed-in view on the same plot closer to the origin, showing the linearity of the characteristics. **d**, Logarithmic-scale $I_{p\text{-}Si}$–$V_{p\text{-}Si}$ output characteristics of InSe/Si HJ-TTs with V_G sweeping from −6 to 6 V with 1 V step. **e**, TCAD-simulated $I_{p\text{-}Si}$–$V_{p\text{-}Si}$ output characteristics of InSe/Si HJ-TTs with V_G sweeping from −0.8 to 0.8 V in 0.2 V steps. **f**,**g**, TCAD-simulated InSe/Si band structures and corresponding $I_{p\text{-}Si}$–V_G transfer characteristics for various $V_{p\text{-}Si}$ and V_G values. $V_{p\text{-}Si}$ = –0.5 V (i); $V_{p\text{-}Si}$ = –0.1 V (ii); $V_{p\text{-}Si}$ = 0.1 V (iii); $V_{p\text{-}Si}$ = 0.5 V (iv); red line, V_G = 0.8 V; black line, V_G = −0.8 V.

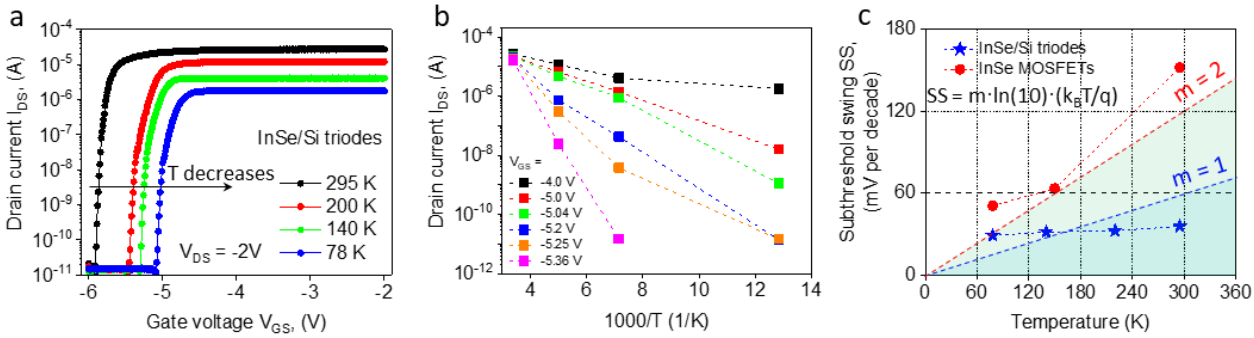

Figure 4. Temperature-dependent electrical characteristics of InSe/Si 2D/3D triodes. (a) Temperature-dependent I_{DS}-V_{GS} transfer characteristics measured at V_{DS} = -2.0 V. (b) Arrhenius plot of drain current as a function of 1000/T for various gate voltages. (c) Subthreshold swing as a function of temperature for InSe/Si 2D/3D heterojunction tunneling triodes and InSe control MOSFETs.

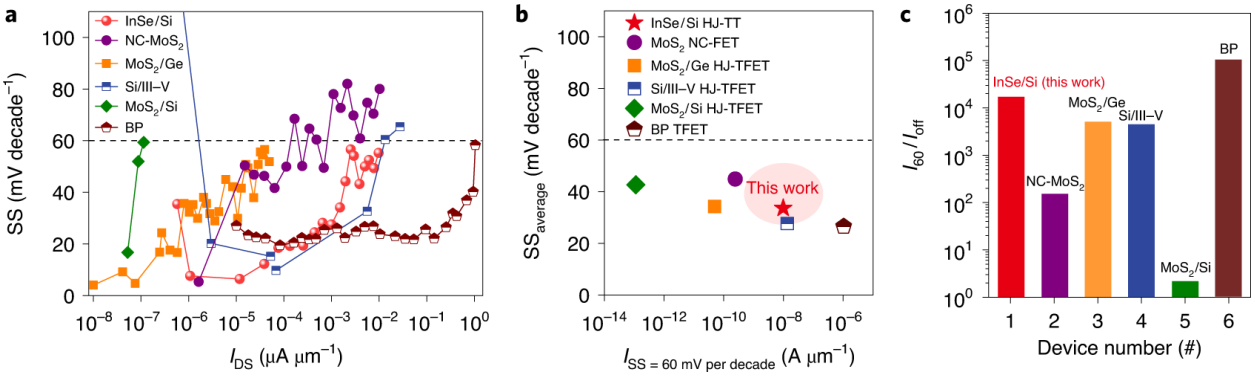

Figure 5. Performance comparison of the InSe/Si 2D/3D HJ-TFETs with reported subthermionic HJ-TFETs and NC-FETs. a, Subthreshold swing as a function of drain current for various types of sub-thermionic FET. The black dashed line represents the SS = 60 mV decade^{-1} limit. The red spheres represent the SS values of InSe/Si HJ-TTs in this work. The InSe/Si HJ-TTs show SS below 60.0 mV decade^{-1} for 4–5 orders of magnitude of drain current, with a minimum of 6.4 mV decade^{-1}. **b**, Average SS versus drain current where SS becomes lower than 60 mV decade^{-1}. Here $SS_{average}$ of InSe/Si covers more than four decades of I_{DS} (red), $SS_{average}$ of MoS_2/Ge covers more than four decades (orange), $SS_{average}$ of InAs/Si covers less than four decades (navy blue), $SS_{average}$ of MoS_2/Si covers less than one decade (green), $SS_{average}$ of NC-MoS_2 covers approximately three decades (purple) and $SS_{average}$ of black phosphorus (BP) homojunction TFET covers more than five decades (brown). **c**, I_{60}/I_{off} for various sub-thermionic devices. The I_{60}/I_{off} ratio of InSe/Si HJ-TTs is >10^4.