Gateless *p-n* Junction Sharpness in Centimeter-Scale Epitaxial Graphene

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(Received xx October 2021;)

PACS numbers: 42.30.Ms, 72.80.Vp, 73.40.-c

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We have demonstrated the centimeter-scale fabrication of monolayer epitaxial graphene *p-n* junction devices using simple ultraviolet photolithography, thereby significantly reducing device processing time compared to that of electron beam lithography typically used for obtaining sharp junctions. This work presents measurements yielding nonconventional, fractional multiples of the typical quantized Hall resistance at $\nu = 2$ ($R_H \approx 12906\ \Omega$) that take the form: $a/b * R_H$. Here, a and b have been observed to take on values such 1, 2, 3, and 5 to form various coefficients of R_H. Additionally, we provide a framework for exploring future device configurations using the LTspice circuit simulator as a guide to understand the abundance of available fractions one may be able to measure. These results support the potential for simplifying device processing time and may possibly be used for other two-dimensional materials.

I. Introduction

We demonstrate how standard ultraviolet photolithography (UVP) and the photoresist ZEP520A were used to build *p-n* junctions (*pnJ*s) that have junction widths smaller than 200 nm on devices made from centimeter-scale epitaxial graphene (EG) growths [1-4]. Quantum Hall transport measurements were performed and simulated for various *p-n-p* devices to verify expected behaviors of the longitudinal resistances in a two-junction device despite junction roughness [5]. Furthermore, we use the LTspice current simulator [see notes] to examine the various rearrangements of the electric potential in the device when injecting current at up to three independent sites. We find that nonconventional fractions of the typical quantized Hall resistance, R_H, can be measured, thus validating the simulations. These results have strong importance in the field of resistance standards and general fabrication techniques for other two-dimensional materials [6-8].

II. Device Fabrication

The growth of high-quality epitaxial graphene can be found in Refs. [9-11]. EG is formed when Si atoms sublimate from the silicon face of SiC. Samples were grown on square SiC chips diced from on-axis 4*H*-SiC(0001) semi-insulating wafers (CREE) [see notes]. SiC chips were submerged in a 5:1 diluted solution of hydrofluoric acid and deionized water prior to the growth process. Chips were placed, silicon face down, on a polished graphite substrate (SPI Glas 22) [see notes] and processed with another photoresist (AZ5214E) to utilize polymer-assisted sublimation growth techniques. The face-down configuration promotes homogeneous growth, and the annealing process was performed with a graphite-lined resistive-element furnace (Materials Research Furnaces Inc.) [see notes]. The heating and cooling rates were about 1.5 °C/s, with the growth performed in an ambient argon environment at 1900 °C.

The grown EG was evaluated with confocal laser scanning and optical microscopy as an efficient way to identify large areas of successful growth [13]. Protective layers of Pd and Au are deposited on the EG to prevent organic contamination. While protected, the EG is etched into the desired device shape, with the final step being the removal of the protective layers from the Hall bar using a solution of 1:1 aqua regia to deionized water. Some variants of this device included electrical contact pads made from NbTiN for lower contact resistances [14-15]. To fabricate the *pnJ*s, completed Hall bars were functionalized with $Cr(CO)_3$ to reduce the electron density to a value close to the Dirac point and on the order of 10^{10} cm^{-2} [16]. A S1813 photoresist spacer layer was then deposited on a region intended to be preserved as an *n* region. Finally, a 100 nm layer of polymethyl methacrylate (PMMA/MMA) and an approximately 350 nm layer of ZEP520A were deposited. The 100 nm layer was intended to be a mild protectant for EG since ZEP520A is very photoactive and known to reduce the mobility of EG when in direct contact with it (see Figure 1).

III. Characterization

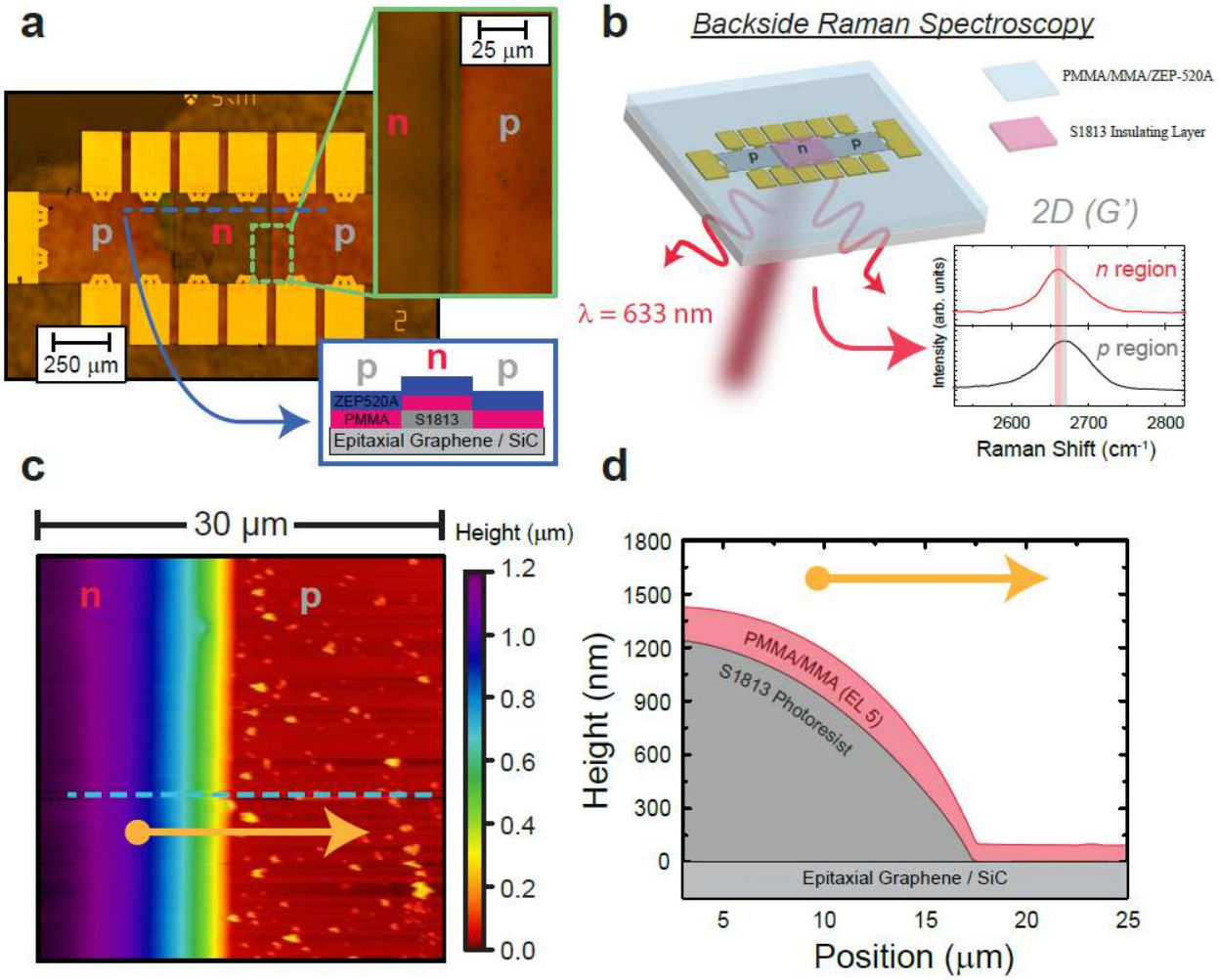

FIG. 1. (Color online) (a) The optical image of the device after processing is shown with labels indicating the intended charge polarity. A cross section of the device is also depicted for clarity. (b) An illustration of the Raman acquisition and a map-averaged 2D (G') spectrum are shown for the *n* (red) and *p* (gray) regions. The transparent red and gray bands indicate the range (for the corresponding polarity) of 2D (G') peak positions to within 1σ of the average. (c) An atomic force microscope image was acquired to gain some insight into how the boundary between the intended p and n regions formed. (d) An extracted profile prior to ZEP520A deposition is shown.

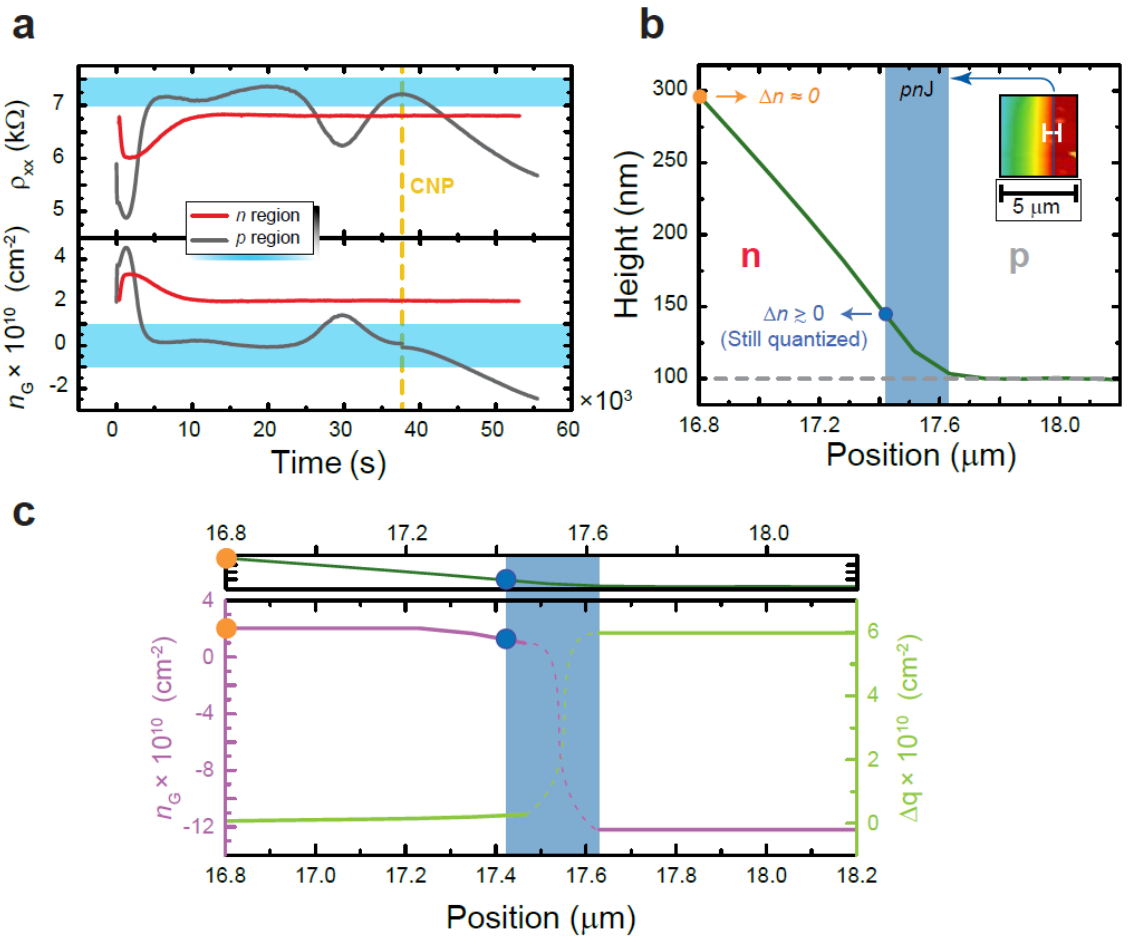

FIG. 2. (Color online) ((a) The longitudinal resistivity ρ_{xx} and electron density in EG n_G are monitored as a function of time in the upper and lower panel, respectively, while the region is being exposed to 254 nm UV light. The $Cr(CO)_3$ helps the carrier density transition from *n*-type to *p*-type despite an extensive time of transient lingering close to the Dirac point. The charge neutrality point (CNP) is marked by a gold dashed line. The cyan shading approximates a range where the electrical properties of the EG would not yield quantized plateaus. (b) The AFM profile and magnified image of the *pnJ* are shown after PMMA/MMA copolymer deposition (totaling 100 nm). The green curve is taken along the white line in the inset. To validate the junction width, multiple devices with various thicknesses of S1813 were measured, as indicated by the orange and blue dot along the profile representing the two example thicknesses of 300 nm and 42.4 nm, respectively. The shaded blue region indicates the bounds within which the carrier density is expected to switch polarity. (c) The same profile and shaded region is projected onto the calculated charge transfer Δq to the ZEP520A layer and profile of n_G.

To assess device quality, the charge configuration of the device needed to be known and the width of the *pnJ*s needed to be estimated. It is also important to approximate how the carrier densities in the regions change with exposure to 254 nm, 17 000 μWcm^{-2} UV light (distinct from the UV light used in photolithography), and this is primarily done by monitoring the longitudinal resistivity in all three regions of a *p*-*n*-*p* device during a room temperature exposure, with two polarities shown in the upper panel of Figure 2 (a). For the *p* region, the expected *p*-type doping mechanism resulting from the deposition of a ZEP520A layer on the whole device persists to the point where the carrier density crosses the Dirac point. This crossing is most evident during the room temperature UV exposure when the longitudinal resistivity of the device exhibits a similar value to when the exposure was started, but instead with a negative time derivative. The S1813 successfully prevents the *n* region from becoming a *p* region, as exhibited by the flat resistivity (and electron density). Though the idea of using ZEP520A as a dopant for EG has been demonstrated [17], accessing the *p* region with that mechanism is challenging due to the intrinsic EG Fermi level pinning from the buffer layer below. However, the reduction of the electron density from the order of 10^{13} cm^{-2} to the order of 10^{10} cm^{-2} by the presence of $Cr(CO)_3$ considerably assists the *p* region to undergo its transition.

NOTES

Commercial equipment, instruments, and materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology or the United States government, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

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