Research Article

Pradeep Namboodiri*, Jonathan Wyrick, Gheorghe Stan, Xiqiao Wang, Fan Fei, Ranjit Vilas Kashid, Scott W. Schmucker, Richard Kasica, Bryan M. Barnes, Michael D. Stewart Jr, and Richard M. Silver

Multi-scale alignment to buried atom-scale devices using Kelvin probe force microscopy

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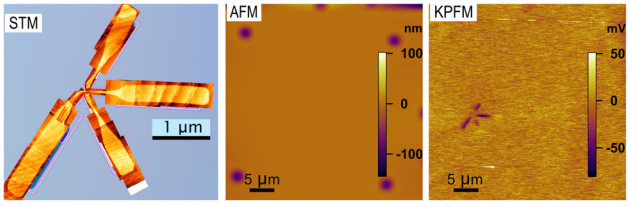
Abstract: Fabrication of quantum devices by atomic-scale patterning with scanning tunneling microscopy (STM) has led to the development of single/few atom transistors, few-donor/quantum dot devices for spin manipulation, and arrayed few-donor devices for analog quantum simulation. We have developed atomic precision lithography, dopant incorporation, device encapsulation, *ex situ* device re-location, and contact processes to enable high-yield device fabrication. In this work, we describe a multiscale alignment strategy using Kelvin probe force microscopy to enable the alignment of buried device components to electronic support structures such as source/drain leads, in-plane and top gates, and waveguides while preserving flexibility in the placement of fabricated STM patterns. The required spatial accuracy to bridge the sub-micrometer scale central region of the device to millimeter scale large wire-bond pads is achieved through a multi-step alignment process at various stages of fabrication, including atom-scale device fabrication using STM, re-location and registration, and electron beam lithography for contact leads and pads. This alignment strategy allows imaging small device regions as well as large-scale fiducial marks, thereby bridging the gap from nanometer STM patterns to the millimeter-scale electrical contact fabrication with a 95% yield on more than 150 devices fabricated to date.



Graphical abstract

Keywords: atomic-scale devices, scanning tunneling microscopy, STM, dopant device, Kelvin probe force microscopy

1 Introduction

Scanning tunneling microscopy (STM)-based lithography on silicon surfaces has been used to fabricate devices with near single-atom positioning accuracy [1–11]. Such devices are excellent test vehicles to observe quantum phenomena at the atomic scale and further advance technological applications in the realm of quantum information science [12–16], and analog quantum simulation [17–20]. For example, it has been proposed that this method can be used to create large-scale qubit systems implementing a surface code quantum computer [21]. The core technology behind the fabrication of these devices is hydrogen depassivation lithography [22–24]. An STM tip is used to selectively desorb hydrogen atoms from a hydrogen-terminated Si (100) surface while the exposed dangling silicon bonds foster the precise placement of phosphorous dopants [25]. The atom-scale fabrication processes take place in an ultra-high vacuum (UHV) environment and the devices are encapsulated in epitaxial silicon. The result is a fully encapsulated and protected two-dimensional dopant device buried under epitaxial silicon that often leaves little to no topographic signature at the surface. A variety of such dopant-based devices have been fabricated by this method in the last decade, demonstrating a viable path for the realization of multi-qubit devices [12,13,26]. One of the

* **Corresponding author: Pradeep Namboodiri,** Physical Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899, United States of America, e-mail: pradeep.namboodiri@nist.gov
Jonathan Wyrick, Ranjit Vilas Kashid, Scott W. Schmucker, Richard Kasica, Bryan M. Barnes, Michael D. Stewart Jr, Richard M. Silver: Physical Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899, United States of America
Gheorghe Stan: Material Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899, United States of America
Xiqiao Wang, Fan Fei: Physical Measurement Laboratory, National Institute of Standards and Technology, Gaithersburg, MD 20899, United States of America; Joint Quantum Institute, Joint Quantum Institute, University of Maryland, College Park, MD 20742, United States of America

key fabrication challenges for these devices is achieving sub-micron positioning accuracy of electrical contacts to the buried STM-fabricated structures [27]. The accurate alignment of contacts is a key requirement in enabling high-yield STM-based device fabrication. This also has important applications with regard to mating buried devices to other types of on-chip electronic/quantum devices such as local top gates, high-frequency lines for nuclear magnetic resonance/electron spin resonance, complementary metal-oxide-semiconductor (CMOS) structures, and microwave resonators. The methods used for fabrication in this article, hydrogen passivation, lithography, phosphine dosing, phosphorous incorporation, and silicon overgrowth, are essentially the same as those used by the Simmons group [28] with the exception of the alignment strategy described here which is the primary focus of this work.

Various methods have been proposed for the positioning and connectivity of atomic-scale STM patterns to micrometer scale contacts and leads. Methods based on having a pre-defined location of STM pattern [27–29] on the chip have advantages in terms of contact alignment, but on the other hand, this imposed patterning location might not have the best surface quality for device fabrication. Ruess *et al.* [28] demonstrated a method to pattern a device aligned to a pre-etched registration mark allowing direct patterning of contacts using electron-beam lithography (EBL) since the device is already registered during fabrication. However, this method limits the flexibility in the choice of device location and requires performing large area survey scans to locate registration marks. Another approach is to use pre-deposited metal marks [29] or pre-implanted contacts [30], which has the advantage that once the device has been patterned, the sub-micron to millimeter-scale contact is already formed and may prove useful to fabricate devices that can be operated *in situ* STM. This approach, however, restricts the standard high-temperature treatments required to obtain pristine silicon surfaces and similarly suffers from the requirement for large survey scans before patterning. It is likely that high yield and reproducible atomic-precision fabrication using STM demands the selection of surface regions that are clean and have a minimum of defects. Once such a high-quality surface region is selected and the STM patterns defined, we need to be able to re-locate these patterns and align the contacts to them. In addition, the patterned STM devices and pad sizes are kept to only a few micrometers in size because of the time constraint associated with exposure of the device layer to potential contamination. It is therefore necessary to have a precise and robust alignment strategy for making electrical contacts to relatively small STM pads that have little if any variation in post-encapsulation topography compared to their surroundings. Since devices are located relatively close to the surface (~30 nm below), it is also necessary to utilize non-invasive post-fabrication processes to preserve the device quality during re-location. Here, we define “re-location” to mean determination of the location of an encapsulated device after it has been removed from UHV. It should be noted that the re-location adds one day to the overall process. This replaces a required initial *in situ* step of performing large area survey scans and positioning the STM tip with respect to the pre-etched fiducial marks which itself can take several hours. The overall process for making a single fully functional device from *in situ* STM patterning to aligned contact fabrication takes roughly 2 weeks.

There are a few options in the imaging techniques used to re-locate the STM fabricated patterns, each of them with its own advantages and disadvantages. Based on its differential conductance contrast, the STM itself is sensitive enough to image shallow subsurface doped regions like the ones in phosphine-doped silicon devices [15,19]. However, the limited vertical and lateral operational range of the STM makes it difficult to measure the taller microscale etched fiducial marks that are used for device registration. Second, common atomic force microscopy (AFM) topographical modes like contact or tapping modes might be used to locate surface features within the necessary nanometer-to-micrometer scanning range, but they have no contrast for buried devices that show little to no topographic perturbations on the top surface. Finally, some specialized AFM modes like scanning capacitance microscopy and scanning microwave microscopy featuring long-range electronic contrast have proven capable of imaging buried patterned dopant devices within scans comprising micrometer-scale areas [29,31,32]. Both techniques produce high-contrast images of buried devices, but they operate in contact mode while applying voltage across the tip-sample contact and have the potential of causing surface oxidation and modification of the silicon surface [33].

To address most of the issues discussed above, we employed a minimally invasive scanning probe technique, namely Kelvin probe force microscopy (KPFM) [34,35], to re-locate and register patterned STM devices with respect to a pre-etched 50 µm grid of reference fiducial marks. With KPFM operating in a dual-pass mode, it is possible to scan relatively large areas encompassing the fabricated devices and have both the surface topography from a mechanical intermittent contact mode like tapping or PeakForce tapping performed in the first pass of the scan and the surface potential map from an electrical modulation carried out in the second pass at 50–70 nm lift height above the scanned surface. The topography and

the potential map are commensurate to one another and hence can be overlaid using a semi-automated algorithm to identify the location of the device with respect to the nearest fiducial marks. In the last several years, we successfully developed a precise and accurate method to fabricate and align STM-patterned quantum devices [3,04,17], and here, we present in detail the alignment methodology behind this process.

2 Methods

2.1 Device fabrication

The alignment method presented in this work spans over all device fabrication stages, including the re-location done by KPFM. First, we start with silicon chips that have a coordinate system defined by two sets of fiducial marks that are pre-etched on each chip (Figure 1a and b). These two sets of pre-etched patterns consist of: (1) STM-compatible fiducial marks that are an array of 50 μm × 50 μm features over the central region of the chip within which any STM-patterned device will be located and (2) EBL alignment marks that are an array including chip alignment marks near the peripheral parts of the chip for high precision alignment of EBL. Both sets of fiducial marks are fabricated by optical lithography with an ASML Stepper PAS 5500/275D[1] (ASML, Veldhoven, The Netherlands) having a specified overlay accuracy of 40 nm across the wafer. The wafers that we use are boron-doped float zone silicon wafers with a resistivity of 1–10 Ω cm manufactured by Virginia Semiconductors (see footnote 1). The STM fiducial marks are etched to nominally 100 nm deep and the EBL alignment marks are nominally 2 μm deep. This allows scanning probe imaging of the fiducials near devices without damaging the probe tip and provides a means to determine scan locations relative to the EBL alignment marks. Second, the pre-etched chips are loaded into a UHV-STM system, flash annealed at 1,200°C to obtain a clean silicon (100) surface, and then hydrogen passivated. We have previously observed and used the presence of these pre-etched features to help modify the step-terrace features leaving relatively large terraces [36]. Third, STM patterning of a device is then carried out at a location with few defects within one of the pre-etched squares. This is followed by phosphorous deposition and incorporation, and then epitaxial silicon is overgrown at 250°C [37] to activate and encapsulate the device. To optimize and baseline the fabrication process, the presence and the vertical confinement of the phosphorous δ-layer fabricated by this process is confirmed by other techniques [38]. Figure 1d shows the image of an STM patterned device, a single electron transistor (SET) during hydrogen lithography prior to phosphorus dosing and silicon encapsulation. The featured SET island tunnel couples to two leads serving as source (S) and drain (D), respectively, and two gates (Gate 1 and Gate 2), so the electron occupancy of the quantum dot can be controlled through the capacitive coupling between the gates and the doped island. These electrodes extend to contact pads from which larger electrical leads for outside connectivity are further defined by subsequent EBL patterning and metallization (Figure 1e and f). To have a precise alignment of the contacts over the STM patterned device pads, the location of this active area must be registered first within the reference coordinate system of the STM fiducial marks (Figure 1b), and, in our method, this registration is provided by KPFM scans over the region of interest.

2.2 KPFM

The KPFM that we used was in the form of PeakForce™ frequency-modulation KPFM (PeakForce FM-KPFM) (Multimode AFM, Bruker [see footnote 1] Santa Barbara), which is an AFM dual scanning mode with a topography scan acquired first in PeakForce tapping mode followed by a second scan line with KPFM data acquired at a given tip height above the surface [35]. The use of the PeakForce FM-KPFM scanning mode provides three main advantages: (1) reduced mechanical damage [39] of the surface during the topographical scanning since the PeakForce is an intermittent contact mode operating with feedback control based on the maximum applied contact force, (2) the bias voltage applied during the KPFM scanning portion is done at a constant height (typically 50 nm) above the surface, so no oxidation damage is produced on the surface; this is in contrast to possible unintentional oxidation induced by the bias changes occurring with other AFM modes [33,40–43]; (3) the FM-KPFM variant provides an enhanced spatial resolution compared to AM-

1 Certain commercial equipment, instruments, or materials are identified in this article to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by NIST, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

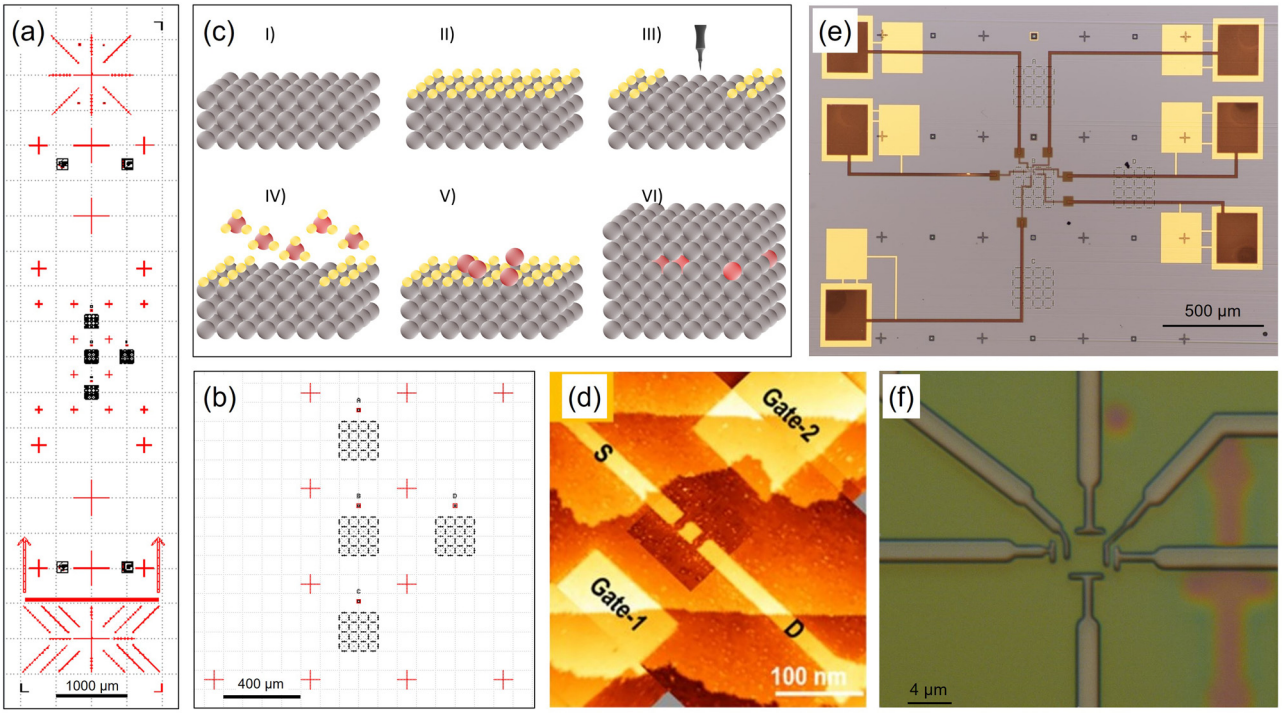


Figure 1: (a) Layout of registration marks on a chip showing the two sets of pre-patterned fiducial marks, namely the STM fiducial marks (the four black arrays of squares in the middle of the chip) and the global and local alignment marks for EBL (red marks). (b) Enlarged view of the array of squares used as STM fiducial marks on the center of the chip. (c) The main steps of hydrogen depassivation lithography for device fabrication: (I) clean silicon surface, (II) hydrogen passivation, (III) tip-induced lithography to selectively remove hydrogen atoms, phosphine (IV) dosing and (V) incorporation, and (VI) intrinsic silicon overgrowth. (d) STM images of a quantum dot connected to source and drain as well as two gate electrodes. (e) Large-scale optical image showing a finished chip with electrical leads from the device electrodes extending to bond pads. (f) Optical image of metal contacts over an encapsulated device.

KPFM due to reduced capacitive coupling between the cantilever and the sample being imaged. The AFM tips used for these scans were Platinum-Iridium coated, electrically conductive tips (SCM PIT_V2, Bruker [see footnote 1] AFM Probes), with the first resonant frequency nominally 60 kHz and cantilever stiffness around 3 N/m. The scan rate was equal to or less than 0.5 Hz because of the large scan area involving etched fiducial marks. As such, the total time required for one single scan varied between 45 and 60 min depending on the desired pixel resolution.

3 Results and discussion

3.1 KPFM imaging for device relocation

The imaging contrast of the KPFM is due to the variation in contact potential difference (CPD), $V_{CPD} = -(\phi_{tip} - \phi_{sample})/e$, between a metallic AFM probe and the sample (refer to Figure 2a), with ϕ_{tip} and ϕ_{sample} being the tip and sample surface potential respectively, and e the electron charge [34]. The electrostatic interaction between the tip and sample can be understood in terms of the dc voltage V_{dc} required to minimize/cancel either the electrostatic force (as in amplitude modulation KPFM) or electrostatic force gradient (as in frequency modulation KPFM) [35] sensed by the tip at every location in the scan, so the characteristic KPFM map, $V_{CPD} = -V_{dc}$, is given by the nullifying condition of the operational feedback control. In the case of the PeakForce FM-KPFM mode that we used, the KPFM feedback control operates on the sideband components at $\omega_1 \pm \omega_E$ that are induced around the first resonance frequency of the cantilever ω_1 by the applied ac bias $V_{ac}\sin(\omega_E t)$ (see Figure 2a). Since ϕ_{tip} is constant during a scan, the KPFM map across a sample with heterogeneous surface potential will directly show the variation in the surface potential between different regions of the sample (see Figure 2b). For a metallic sample, ϕ_{sample} simply equates to the work function. In a semiconductor material, ϕ_{sample} also includes contributions

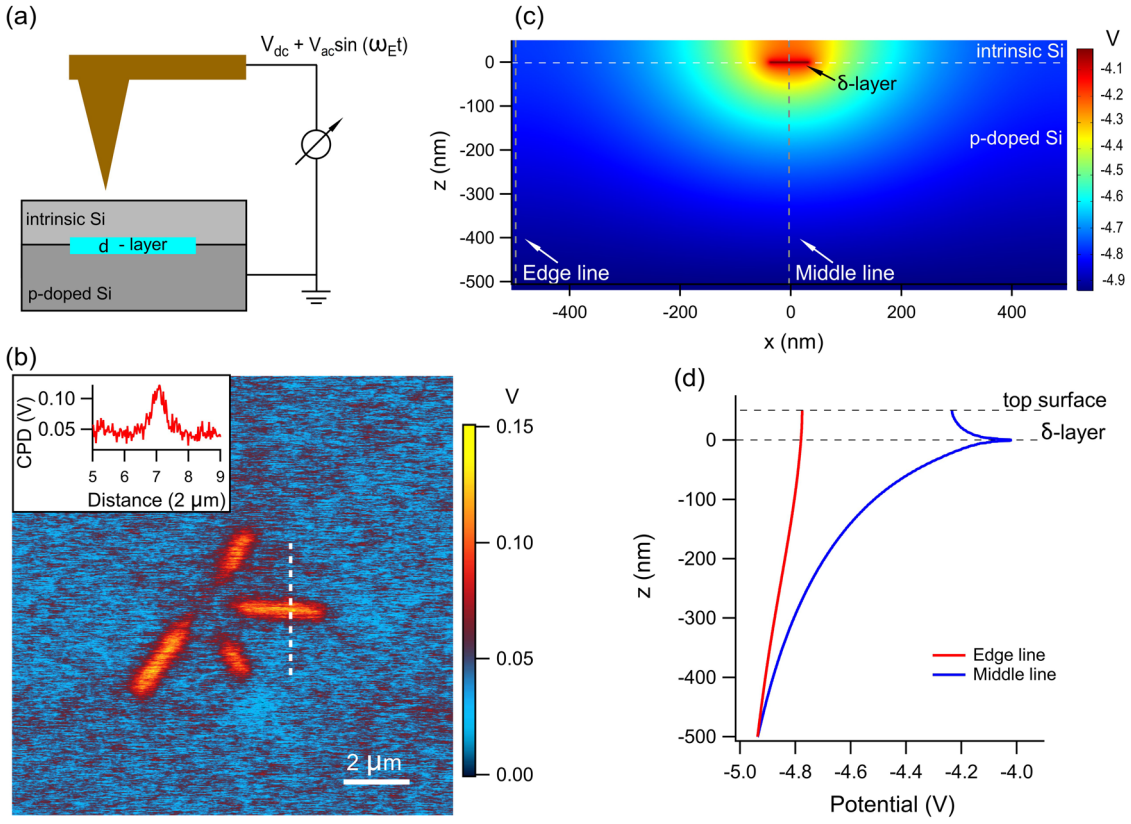


Figure 2: (a) KPFM setup over a Si-based heterostructure that incorporates a δ-layer (blue) between the p-doped substrate (dark gray) and the nominally intrinsic top encapsulation (light gray). (b) KPFM contrast measured over an area consisting of a phosphorous-doped device. The inset shows tip-sample CPD along the dotted line. (c) The calculated 2D electrical potential map of a Si-based heterostructure that mimics the cross-section of the actual layer structure of a doped buried device. (d) Vertical cross-sections from (c) across regions with (middle line) and without (edge line) δ-layer doping.

from surface charge states, doping, surface band bending, *etc.* The buried dopant devices are encapsulated by a 30 nm thick silicon layer in UHV, and we expect that a uniform layer of native oxide (~2 nm) is also formed after the sample is removed from UHV. Therefore, with no additional surface treatments on the sample, the KPFM image contrast is dominated by the changes in the subsurface electric potential induced by doping, so that an image of the patterned device is obtained. From the measurements, the convolution introduced by the electrostatic tip sample interaction is within 50 nm around the imaged structures, which is within the KPFM spatial resolution.

To illustrate the variation in the surface CPD due to a buried δ-layer we simulate the surface potential of a δ-layer region using the semiconductor module of the COMSOL Multiphysics platform (COMSOL Inc., Burlington, MA, USA [see footnote 1]). The Poisson–Boltzmann equation for the space charge distributions of carriers and ionized dopants across a 2D section of a doped heterostructure was solved. The model allows carrier movement using drift equations to satisfy the equilibration of the Fermi level across interfaces and at boundaries. The simulated subsurface electric potential across a silicon heterostructure is shown in Figure 2c, where the layer structure and electron doping profile implemented in the simulation are similar to those used in our devices, namely $n = 10^{12}\,\mathrm{cm}^{-3}$ over 30 nm (for the encapsulating top layer), $n = 10^{20}\,\mathrm{cm}^{-3}$ over 3 nm (for the highly doped δ-layer), and $p = 10^{15}\,\mathrm{cm}^{-3}$ over 500 nm (for the substrate) where n is the doping concentration. Within the classical Poisson–Boltzmann approximation for doping confinement, the simulation shows a change in the electrical potential across the subsurface region in the presence of the highly doped region below a 30 nm thick encapsulation that qualitatively reproduces the contrast seen in KPFM. A more accurate model of the surface potential introduced by the δ-layer would require taking into account: atomistic details, probe geometry, and surface conditions of the sample and the probe, such as surface dipoles, surface states, oxide layer, and humidity which are beyond the

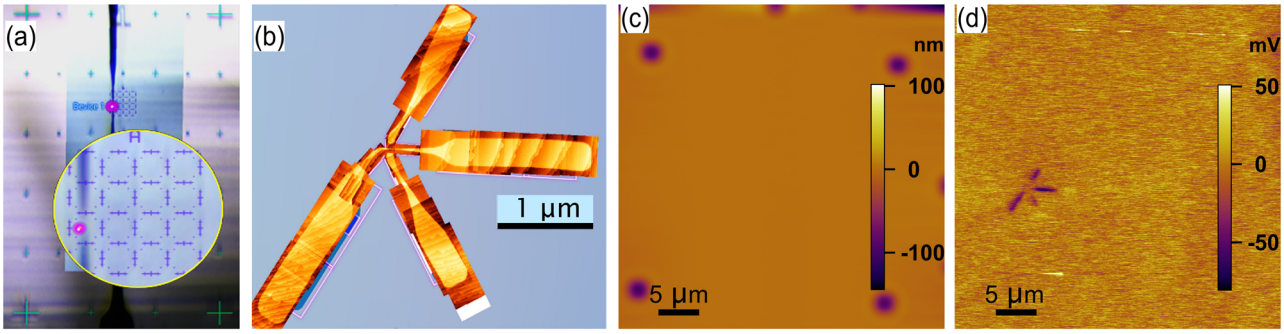


Figure 3: (a) Optical images acquired with a long working distance camera (two different camera angles are used to triangulate the sample position) of the STM tip and the sample; round inset is a zoom showing the STM tip and its reflection indicating an approximate location of the patterned device with respect to the STM fiducial marks. (b) STM image of a device after patterning showing device components leading to larger device pads. (c) AFM topography and (d) KPFM surface potential maps used to locate the device from (b) within four nearby STM fiducial marks.

scope of this work. The presence of the δ-layer and high carrier concentration modulates the electric field resulting in band bending that extends to the surface; this effect is measurable as a local variation in surface potential above δ-doped regions when compared to undoped regions (refer to the profiles shown in Figure 2d). As explained above, KPFM is sensitive to this local change in surface potential and is used to image the buried devices.

The scan region to relocate a device using KPFM mapping is chosen based on an optical image of the tip-sample reflection point captured in the UHV system, as shown in Figure 3a. The STM scan of a device with extended contact pads is shown in Figure 3b. Since KPFM has a large scan range capability, we can quickly locate buried devices. An example of a KPFM scan is shown in Figure 3c (topography) and d (surface potential) over a 40 μm × 40 μm scan area with the STM fiducial marks visible in both topography and surface potential images and the extended contact pads of the device clearly visible only in the surface potential image.

3.2 Overlay and alignment procedure

From KPFM images the relative position of an STM-patterned device with respect to the STM-compatible fiducial marks is extracted and then used to register the device with respect to EBL alignment marks. We have developed a multiscale alignment scheme, where images ranging from atomic-scale STM images to micrometer-scale AFM scans and optical microscopy images can be overlaid on a chip layout defined by the CAD file used to generate fiducial marks (a GDS-2 file[2]). In most cases, we find that alignment can be achieved by using a combined minimal subset of images consisting of AFM topography, KPFM map, and STM fiducial layout of the GDS-2 file. As shown in Figure 3, we acquire AFM scans large enough to include both the encapsulated device and several distinct shallow etched STM fiducial marks. Distortion is common in large scanning probe images as a result of creep, drift, and hysteresis of the piezo-electric scanner, resulting in an inaccurate device location relative to the fiducial marks. We account for these distortions by enforcing agreement of four "control" points in the AFM topography image with the four equivalent points in the GDS-2 file, as illustrated in Figure 4.

Without imposing additional constraints, there is no unique mapping from four points on a given 2D image to four points on another image, particularly in the case where we know one image was generated with piezo distortion in which straight lines can become curved. As for our mapping we choose a simple linear mapping, where for a given point $\vec{p}$ in the original AFM image, we write $\vec{p}$ as a linear combination of the coordinate vectors $\vec{c}_i$ defined to be the four corners of the image:

$$\vec{p} = \sum_{i=1}^{4} g_i \vec{c}_i, \tag{1}$$

and we impose a similar relationship for the transformed point, $\vec{p}'$, of the re-mapped image with respect to a set of transformed corners, $\vec{c}_i'$:

$$\vec{p}' = \sum_{i=1}^{4} g_i \vec{c}_i', \tag{2}$$

2 GDS stands for graphic design system and is a database file format used for data exchange in a variety of cases such as creating layout for nanoscale fabrication using lithography.

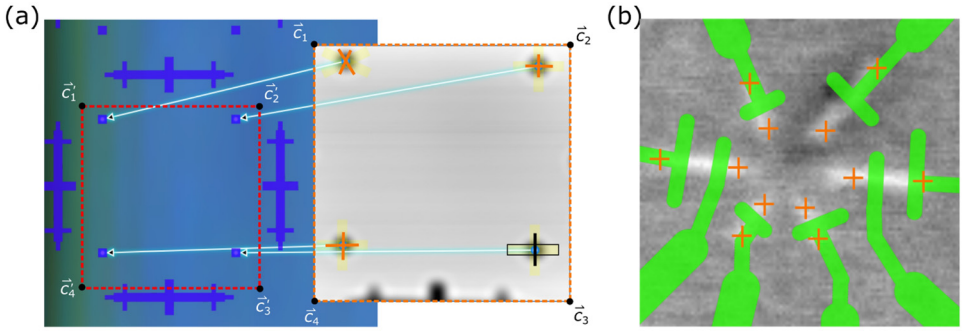


Figure 4: (a) Mapping an AFM topography (orange dashed outlined square in the middle of the figure) to the GDS-2 fiducial design coordinates (red dashed outlined square in the left part of the figure). The regions around the STM fiducial marks on the AFM topography (yellow rectangles) are analyzed to determine the centers of the fiducial marks (orange and black cross lines). Overlayed perpendicular (or near perpendicular) sampling regions (yellow rectangles) are chosen from the topography image to generate two center lines (orange solid lines) whose intersection defines the center of the circular etched feature; one bottom right sampling region is highlighted (black outline) and its corresponding center line is marked in black for clarity. The locations of these centers are then mapped (blue arrows) to the corresponding points on the GDS-2 file. (b) The final planned EBL contacts (green leads) are overlaid on the KPFM image (contact pads in white with ends marked by orange crosses).

where we assume that the coefficients g_i will be the same for both equations (1) and (2). We find that this mapping has consistently generated coordinates that, when used to direct metallization for contacts, result in ohmic contact to each device lead.

The four control points are chosen based on the available STM fiducial marks in the vicinity of the device. According to our design, the device will be found between some set of four circular STM fiducial marks that can be imaged simultaneously (see Figure 4a). Given the finite lateral width (~100 nm) of the etched fiducials after anneal, their precise locations in the AFM topography image are not well-defined so we have adopted a semi-automated edge detection approach to determine the centers of the circular marks: as shown in Figure 4a, rectangular regions (yellow rectangles) from the AFM topography image were chosen to calculate the center lines of the STM fiducial marks (the source code of this procedure is available at reference [44].

The algorithm for determining the center lines of the STM fiducials treats them as topographic trenches having parabolic minima. A given rectangular region of the image is separated into a series of horizontal lines (*i.e.*, horizontal "scan lines") or profiles. A least-squares parabolic fit is then applied to each profile in a neighborhood about its absolute minimum to determine the x-coordinate of the minimum (here x is the horizontal position of the local coordinate system defined by the chosen rectangular region). Each of these x-coordinates (one per profile) is then least-squares fit with a line that represents the algorithm's best estimate of the center line of the STM fiducial mark. Two non-parallel regions overlaid on a circular mark can be used to find the center point as the intersection of their two respective center lines (refer to the black rectangle and line for the lower-right fiducial on the AFM image of Figure 4a); this intersection acts as a well-defined control point that can be mapped to the equivalent position in the GDS-2 file.

Once the AFM topography image has been properly overlaid with the planar geometry of the GDS-2 file, the same mapping can be used to overlay the KPFM image since it is commensurate (notably the four-point mapping should be done separately for the trace (forward scan) and retrace (reverse scan) AFM images to account for the reverse scan image that might not be fully commensurate with the forward scan image. Having generated transformed images that show the locations of the STM-fabricated contact pads properly overlaid relative to fiducials, we then mark (crosses in Figure 4b) relevant positions given by the GDS-2 file to guide the alignment of the EBL contact pattern. The code developed by Wyrick [44] for STM patterning, data acquisition, and analysis with overlay utilities to accurately determine device coordinates is available for download in the Github repository for public use.

3.3 Overall uncertainty estimation

The uncertainty of the alignment method has contributions from each of the three stages of the fabrication process. The first is fabrication of etched STM fiducial marks and EBL registration marks before STM patterning. Lithography overlay for this is accomplished using an ASML Stepper PAS 5500/275D (see footnote 1) which has a specified overlay accuracy of 40 nm. The second process

involves registration of the device to STM fiducials using KPFM and the mapping algorithm to overlay the images to optical and GDS-2 files. We found out that repetitive coordinate re-mapping of the STM fiducials from successive KPFM images can be used to further reduce the associated uncertainty. For a series of devices, we determined that the KPFM positioning uncertainty (1 standard deviation) was 140 nm. The third process is the EBL alignment during patterning for metallization. We routinely use a JEOL JBX 6300-FS (see footnote 1) (Jeol Ltd, Akishima, Tokyo, Japan) direct write EBL which has a specified positioning accuracy of 20 nm. By combining the standard uncertainties from the three different alignment steps mentioned above, the overall uncertainty estimate from all three levels of alignment is about 160 nm. This indicates that the overall uncertainty is dominated by the uncertainty introduced by the registration of the KPFM images to the fiducial grids. The shapes of the EBL patterned contacts (shown as green in Figure 4b) are designed to compensate for this uncertainty. This is evidenced by successful electrical measurements performed on the device in this study and other works [3,4,17].

Electrical measurements were performed on a wide range of device configurations such as van der Pauw devices, single electron devices, and single and multi-dot arrays. Figure 5 shows a summary of measurements of some of the typical device types, from four-point sheet resistances on van der Pauw devices and two-point resistances across single contact pads in SET and tunnel junction devices. The source and drain leads on our devices are typically fabricated with two contacts as shown (green) in Figure 5a; an extended view of the fabricated metal contacts is shown in Figure 5b. Figure 5d shows the I–V plots between two such contact fingers on a set of STM-patterned contact pads. These measured resistance values are not normalized, but they are very small compared to the tunnel junction resistance of our devices (few MΩ), which is critical for the successful operation of our devices [38,45]. Variation in the resistance is attributed to several factors such as the quality of the δ-layer and epitaxy of silicon overgrowth, palladium silicide contacts, and the contribution from alignment. Using this alignment and contacting process, we are able to make very clean electrical transport measurements on atomic-scale devices. An example of the quality of the device fabrication, including the alignment and electrical contact is illustrated in Figure 5c. showing transport measurement through a SET island dominated by single electron tunneling events known as coulomb blockade oscillations [46].

We have implemented and tested the alignment process described in this article on more than 150 multi-

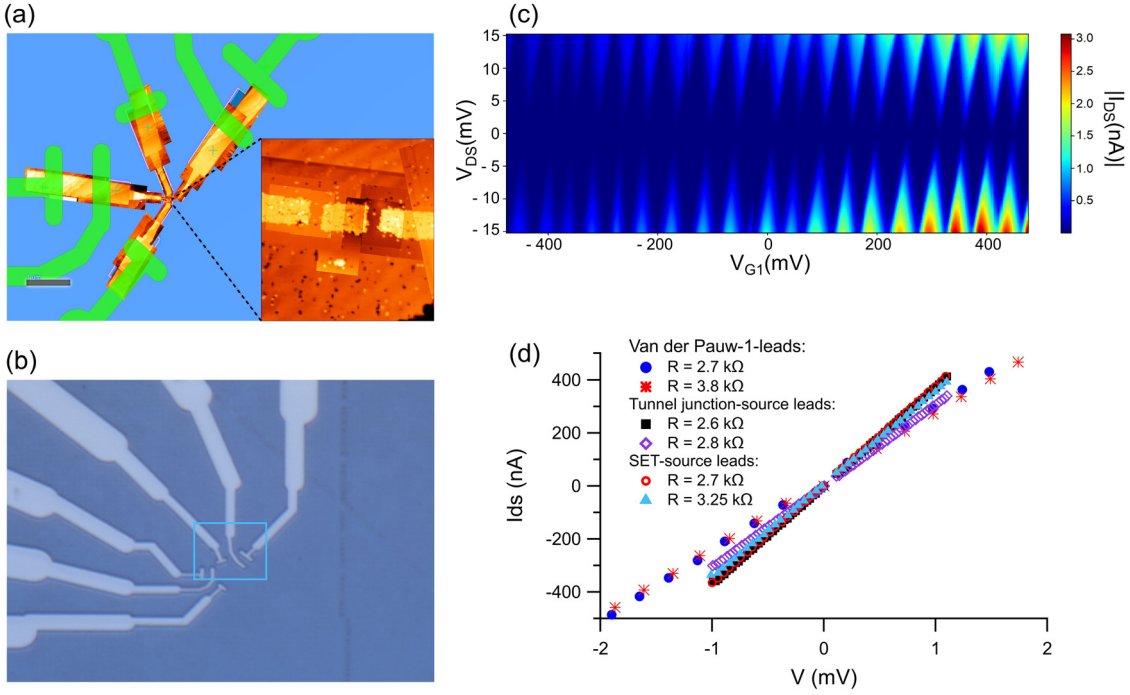


Figure 5: (a) STM image of a patterned SET with designed contacts (green) overlaid on the STM patterned contact pads; inset shows the core device region. (b) Contacts fabricated by EBL and subsequent metallization and anneal; the blue rectangle delimitates the region detailed in (a). (c) Transport measurements on the SET showing coulomb blockade oscillations demonstrating single electron tunneling events. (d) Two-point I–V plots from contact combinations on various devices.

terminal devices such as nanowires, tunnel junctions, SETs, and donor dot structures, resulting in better than 95% contact yield. This contact yield is a combination of errors due to contact processes and the alignment processes. We used palladium silicide to contact the buried δ-layer devices and this process has been demonstrated to work with a near 100% contact yield [45]. This alignment strategy has been routinely used on our devices and its effectiveness is evidenced by the successful measurement of coulomb oscillations in SETs, electron loading and unloading in donor dot devices, and measurement of electron tunneling through arrayed atomic-scale features. The combination of this high-yield contact process and a flexible yet reliable alignment process addresses what has been one of the more substantial challenges to successful atomic-scale STM patterned device fabrication. Of the limited number of devices that have failed, known issues with silicon overgrowth and phosphorous dosing were identified. Therefore, we believe that the apparent reduction from 100% in total yield is limited mostly by the device fabrication in UHV including STM patterning, dosing, and silicon encapsulation processes.

For aligning CMOS structures to STM patterned single atom structures it would be desirable to achieve even greater accuracy (on the order of tens of nanometers). To address this, it will likely be necessary to adopt hybrid strategies where the technique described here would be combined with elements from the work of Fuechsle *et al.* [27] to take advantage of the benefits the two methods offer while mitigating some of the associated disadvantages.

4 Summary and conclusions

We have demonstrated a method to image buried devices with non-contacting electrical mode scanning probe microscopy on surfaces that show no apparent topographical surface perturbations. We developed a multilayer overlaying strategy that provides sufficient accuracy to align complicated contact configurations over buried dopant devices. The method provides reliable re-location of buried devices and determination of coordinates for placement of additional e-beam-defined device components. This methodology allows us to fabricate STM-patterned devices anywhere on a chip without prior registration to any etched fiducial marks during the fabrication stage, with the benefit of saving a significant amount of STM imaging time and yielding flexibility to select suitable areas on the surface free of defects and contaminants. We have achieved an overall contact placement accuracy of 160 nm which we found to be sufficient for integrating various components to the STM fabricated devices such as top gates and coplanar waveguides.

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