Applied Physics Letters

Detection of individual spin species via frequency-modulated charge pumping

Cite as: Appl. Phys. Lett. **120**, 053504 (2022); https://doi.org/10.1063/5.0081172
Submitted: 07 December 2021 • Accepted: 20 January 2022 • Published Online: 02 February 2022

J. P. Ashton, M. A. Anders and J. T. Ryan

Applied Physics Letters ARTICLE scitation.org/journal/apl

Detection of individual spin species via frequency-modulated charge pumping

Cite as: Appl. Phys. Lett. **120**, 053504 (2022); doi: 10.1063/5.0081172
Submitted: 7 December 2021 · Accepted: 20 January 2022 ·
Published Online: 2 February 2022

J. P. Ashton, M. A. Anders, and J. T. Ryan[a]

AFFILIATIONS

Nanoscale Device Characterization Division, National Institute of Standards and Technology, 100 Bureau Drive, Gaithersburg, Maryland 20899, USA

[a]Author to whom correspondence should be addressed: Jason.ryan@nist.gov

ABSTRACT

We utilize a frequency-modulated charge pumping methodology to measure quickly and conveniently single "charge per cycle" in highly scaled Si/SiO_2 metal–oxide–semiconductor field effect transistors. This is indicative of detection and manipulation of a single interface trap spin species located at the boundary between the SiO_2 gate dielectric and Si substrate (almost certainly a P_b type center). This demonstration in sub-micrometer devices in which Dennard scaling of the gate oxide has yielded extremely large gate oxide leakage currents eliminates interference between the charge pumping current and the leakage phenomenon. The result is the ability to measure single trap charge pumping reliably and easily, which would otherwise be completely inaccessible due to oxide leakage. This work provides a unique and readily available avenue for single spin species detection and manipulation, which can be applied as a quantized standard of electrical current as well as to serve as a potentially useful platform for developing quantum engineering technologies. Finally, we discuss potential underlying physical mechanisms that are involved in producing a seemingly contradictory measure of both odd and even integer values for charge per cycle.

Published by AIP Publishing. https://doi.org/10.1063/5.0081172

The ultra-scaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) has paved the way for tremendous improvements in integrated circuit technology. However, with this comes additional complexities and challenges associated with smaller geometry devices and thinner gate dielectrics. A particularly interesting aspect of these ultra-scaled devices is the role of atomic-scale semiconductor/gate dielectric interface spin species (atomic-scale trapping centers), which are well known to drive many performance, yield, and reliability related issues.[1–4]

As device geometries approach fundamental physical limits, the role of a single atomic-scale trapping center (a single broken bond for example) becomes increasingly more important and can have deterministic impacts on device operation.[5] A rather well-known example is random telegraph noise, which, in some cases, results in a complete blockage of drain current.[6–9] A detrimental non-ideality of performing measurements in highly scaled MOSFETs emerges from thin gate dielectrics. Quantum mechanical tunneling currents, known as gate leakage currents, become significant with ultra-thin gate dielectrics.

Countless varieties of measurements have been developed to characterize MOSFET interface trapping centers.[4,10–16] Among these, the so-called charge pumping (CP) methodology has proved to be incredibly popular due to its relative ease of use and adaptability.[10–12] Many different CP measurement configurations have been developed to study various properties of interface traps, including everything from simple trap counting through detailed density of states measurements.[16–20]

In the simplest case, CP yields a current response, I_{CP}, that depends on a gate pulse that acts to cyclically accumulate and invert the semiconductor/dielectric interface. The charge carriers introduced during these cycles can become trapped at interface trap and recombine as electron–hole pairs. I_{CP} is proportional to the frequency of these cycles, f_{CP}, according to $I_{CP} = qA_G f_{CP} D_{it} \Delta E$, where q is electronic charge, A_G is the gate area, D_{it} is the interface trap density per unit energy, and ΔE is the recombination energy window determined by the electrostatics of the accumulation and inversion pulses [determined by the square wave gate pulse high ($V_{G,High}$) and low ($V_{G,Low}$) voltages], which act to fill interface traps with charge carriers and force electron–hole recombination.

Many non-idealities of this simple picture exist, including the so-called geometric effect and thermionic emission loss.[12,18] In ultra-scaled MOSFETs with extremely thin gate dielectrics, quantum mechanical tunneling currents, known as gate leakage currents, are very important to consider. Often, orders of magnitude larger than I_{CP}, gate leakage make conventional CP measurements extremely

difficult and often impossible. Various refinements to overcome this challenge have been developed, with varying degrees of success.[13,21–28] Among these, frequency modulated CP (FMCP) stands out due to its robust nature and ability to easily overcome the fundamental measurement challenges associated with measuring very small signals (I_{CP}) riding on top of a much larger background (leakage currents).[21,22]

CP measurements have also been utilized to study single trap within sub-micron MOSFET devices, again with varying degrees of success and ambiguity.[29–34] In the simplest case of ignoring thermionic emission loss such that the trapping or recombination efficiency is 100%, a single interface trap will yield a CP response that scales linearly with f_{CP} by exactly $1.602\,176\,634 \times 10^{-19}$ C, the SI base unit of elementary charge q.[35] In fact, the nature of this phenomena is under active consideration as a room temperature quantum current source.[34] For clarity, this equates to an I_{CP} of approximately 160 fA per MHz of CP frequency per trap. Based on literature reports, the actual slope of this curve for a single trap could potentially vary between $0 \leq q \leq 2q$.[29–32,34] Beyond the known CP non-idealities mentioned above, other explanations have been proposed in the literature to explain this seemingly odd behavior.[32,34]

In these types of measurements, relatively thick gate dielectrics are desired such that gate leakage currents are minimized with respect to the sub-pA range of expected CP current. However, these measurements also require quite small sub-micrometer resolution channel areas such that only a single interface trap exists. In this work, we overcome the need for thick oxides and leverage FMCP to detect single interface traps within sub-micrometer devices with 1.7 nm gate dielectrics. By modulating the CP gate pulse between two frequencies and demodulating the substrate current via lock-in detection, we robustly resolve fA range CP responses in the presence of orders of magnitude larger leakage currents. This enables relatively easy and routine CP measures of single interface traps in rather common MOS technologies, thereby demonstrating FMCP's utility as a process and development monitoring tool as well as paving the way for use in quantum engineering technologies.

The FMCP apparatus is depicted in Fig. 1(a) and consists of an arbitrary waveform generator (AWG) that is connected to the gate terminal of a MOSFET and monitored with an oscilloscope. This CP waveform consists of a simple trapezoidal wave that is continuously modulated between a high frequency, f_1, and a low frequency f_2, at a modulation frequency f_{mod}. The voltage amplitudes ($V_{G,High}$ and $V_{G,Low}$) of this pulse train are held constant as we modulate back and forth between the two frequencies. The source and drain terminals are grounded in all our measurements. Here, f_{mod} is controlled with a second AWG that is connected to both the gate pulse AWG and the reference input of a lock-in amplifier (LIA). The MOSFET body/substrate current, I_{sub}, is fed into the LIA for demodulation and has the form of a simple square wave of frequency f_{mod} and high and low levels corresponding to I_{CP} at f_1 and f_2, respectively. The modulated gate waveform and resulting substrate signal I_{sub} are illustrated in Fig. 1(b). Here, we also provide the definition for modulation depth, $\frac{f_1-f_2}{2}$, a frequency figure of merit utilized in FMCP measurements.[21,22]

For demodulation of the transmitted I_{sub}, the shape is approximately a square wave for which the fundamental frequency RMS amplitude is given by $\pi/4$ multiplied by the lock-in output voltage.[21,22] The output of the LIA (both in phase V_x and out-of-phase V_y) is then transmitted to a semiconductor parameter analyzer, which multiplies

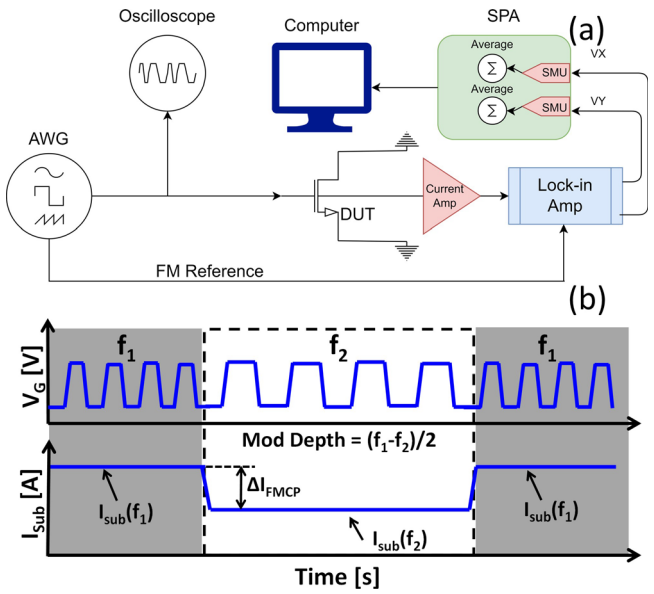

FIG. 1. (a) Schematic illustration of the FMCP apparatus used for single trap detection. (b) Modulated gate pulse shape (top) and resulting two level substrate current I_{sub} (bottom) as a function of time that is fed into the lock-in amplifier. The lock-in output is then directly proportional to the FMCP current, ΔI_{FMCP}.

the RMS amplitude by two to retrieve the peak-to-peak amplitude and is then averaged. Connections to the device under test utilized a standard wafer probing station enclosed within a metal box to eliminate photo generation effects and to minimize noise.

The MOSFET samples utilized here are high quality production grade Si/SiO_2 devices with 1.7 nm thermally grown oxides. Rather large area devices ($1\,\mu m \times 100\,\mu m$) were first measured with conventional CP as well as FMCP, which yield a mean interface trap density of about $3 \times 10^{10}\,cm^{-2}\,eV^{-1}$ corresponding to about 15 000 interface traps in a device of this size. Much smaller devices ($125\,\mu m \times 250$ nm) from the same wafer were utilized for the single trap measurements. Statistical variations due to processing/yield, plus the fact that the number of traps per device must be a whole number (quantized), result in observations of these smaller devices with a range of total traps between zero and about four or five. Note that an increase or decrease in a single trap here has a large impact on what one would calculate for an interface state density (due to the sub-micrometer gate dimensions). While it is not possible to measure zero traps (CP could not occur), the lack of a signal in some devices implies that some devices do not contain any (but other factors cannot be ruled out completely). We regularly (but not always) observe devices with a single interface trap. It should be noted that the uncertainty in our current measurements is no greater than $\pm$ 10 fA.

Figure 2 shows FMCP results from the larger ($1\,\mu m \times 100\,\mu m$) devices from which we obtained a mean interface state density. It is important to note that attempts to perform conventional CP measurements on this device failed to produce any meaningful results due to the large leakage current to CP signal ratio (not shown). Also note the ΔI_{CP} vs modulation depth data are both linear and intersect the vertical axis at zero, indicating both reliable CP measurements and effective suppression of gate leakage current. From

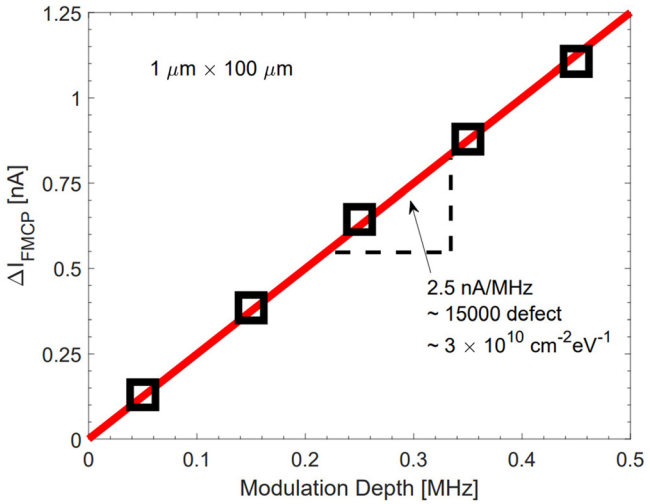

FIG. 2. ΔI_{FMCP} as a function of modulation depth for a larger $1 \times 100\ \mu m^2$ device. Here, we extract a charge per cycle of about 2.5 nA/MHz, corresponding to about 15 000 traps in this large device and a mean interface trap density of $3 \times 10^{10}\ cm^{-2}eV^{-1}$. Note that due to extremely large leakage currents, conventional CP approaches were unable to produce meaningful results (not shown).

this figure, the slope of the line gives the number of traps in this device, about 15 000.

Next, we show results from a much smaller device that likely contains a single interface trap. As mentioned previously, the thin oxide of the MOSFETs yields extremely high gate oxide leakage currents relative to the expected single trap response. This is illustrated in Fig. 3, which shows an attempt to perform conventional CP Elliot curve (fixed amplitude swept base voltage[11]) measurements at 1 MHz. Here, $V_{G,High}$ minus $V_{G,-Low}$ (amplitude) is held constant at 3 V while $V_{G,Low}$ (the base voltage) is swept from −3 to 0 V. The results clearly illustrate that no useful CP data are obtained, and the leakage signal (about 3 pA) is about 20 times greater than the expected CP signal for a single trap at 1 MHz (160 fA).

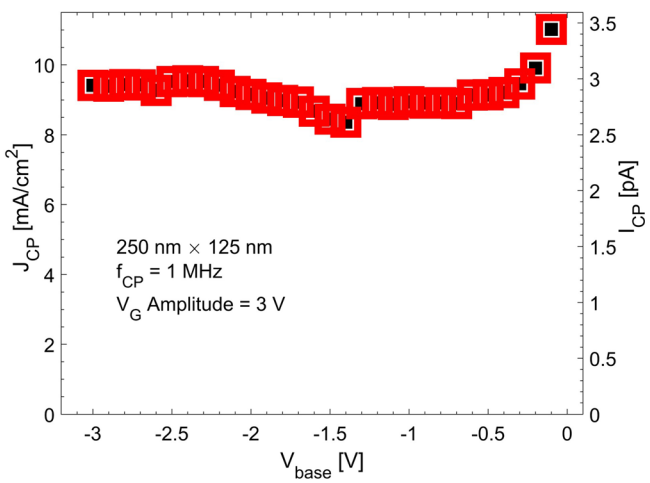

FIG. 3. Conventional CP Elliot curve attempt on the much smaller device. Due to the very large gate leakage current, no meaningful CP data are obtained.

Next, using the same device, the same Elliot curve measurements, performed this time within the FMCP framework described above, were attempted. As shown in Fig. 4, the measured ΔI_{FMCP} is plotted on the left axis and the corresponding charge per cycle, normalized to fundamental electric charge q, is plotted on the right axis. This plot strongly indicates that a single trap is being pumped or "accessed" by the measurement as only a single "bump" in the curve is present with a peak amplitude corresponding to elementary charge, q.

Choosing values of the gate voltage pulse that correspond to the peak of this curve, we next perform variable modulation depth measurements on the $125 \times 250\ nm^2$ devices, shown in Fig. 5. Similar to Fig. 2, which was made on a much larger device, these data are also linear with frequency and intersect the vertical axis at zero, indicating reliable CP measurements and elimination of leakage currents. Specifically, important here is that the slope of this line is about 1.73×10^{-19} C, very close the defined value for a single electronic charge (fundamental constant q).

Thus, we have shown that FMCP may be rather easily utilized for single trap detection and yields a relationship $\Delta I_{FMCP} = q\Delta f_{CP}$. As noted, recent works show that for a single trap, the actual value can vary between $0 \leq q \leq 2q$, possibly due to the amphoteric nature of the likely P_{b0} type traps found at Si (100)/SiO_2 interfaces.[1,36] We have also made measurements (not shown) on devices, which display a slope of $2q$. While possibly due to two traps, statistical variation of the energy levels associated with a particular charge state of a singular trap could give rise to this difference in slope. The classical amphoteric description of P_{b0} type centers yields two energy levels of the trap in the Si bandgap, corresponding to the positive to neutral (+1/0) and neutral to negative (0/−1) transitions.[36,37] This yields two peaks in D_{it} vs energy that lie in the upper and lower parts of the Si bandgap.[32,37]

The range in energy explored by CP measurements, ΔE, can be defined by

$$\Delta E = 2kTln\left(\frac{V_H - V_L}{v_{th}\bar{\sigma}n_i\left(V_{th}^{CP} - V_{FB}^{CP}\right)\sqrt{t_r t_f}}\right).$$

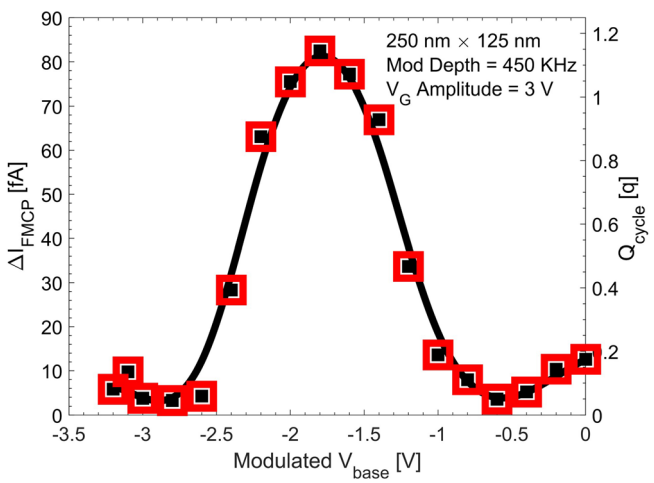

FIG. 4. Utilizing the FMCP framework, meaningful Elliot curves are obtained on a small device that strongly suggest the pumping of a single interface trap.

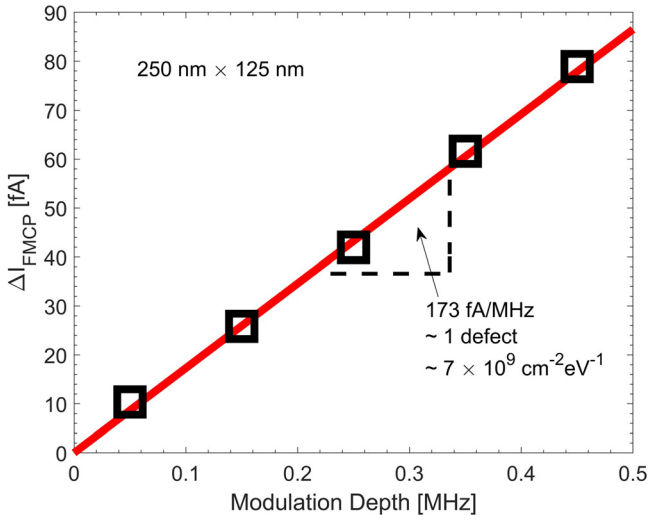

FIG. 5. ΔI_{FMCP} as a function of modulation depth for a much smaller device. Here, a charge per cycle of about 1.73 fA/MHz is extracted, again, strongly indicating the pumping of a single interface trap.

Here, k is Boltzmann's constant, T is the temperature, V_H and V_L are the high and low voltages of the CP waveform, ν_{th}^{-} is the geometric average of the electron and hole thermal velocities, $-\sigma$ is the geometric average of the electron and hole capture cross sections, V_{th}^{CP} is the CP threshold voltage, V_{FB}^{CP} is the CP flatband voltage, and t_r and t_f are the rise and fall transition times of the CP waveform.[10,12] This expression dictates the range in energy explored by CP measurements (recombination window), which at room temperature is about 50% of the Si bandgap. Thus, for a single trap, which cannot be described as a distribution of energy levels, or a "density," but are rather fixed and discrete (quantized), if either the (+1/0) or (0/−1) levels lie outside of the CP window (1), only a single q will be observed. If both lie within the window, $2q$ will be observed. Tsuchiya and Ono recently argued this in single-trap detection with CP in Si MOSFETs.[32]

Another possible explanation of the observation of only a single charge per cycle (rather than two charge per cycle implied by the amphoteric picture) involves the kinetics of the P_{b0} center itself. Recent work by Cheung *et al.* argues that the kinetics involved in fast voltage changes (like those typically utilized in CP measurements) vs relatively slow voltage changes (as typically utilized in conventional capacitance vs voltage measurements) could explain the observation of only a single charge per cycle.[34] Cheung *et al.* argue that the acceptor state, which exhibits sp^3 like character, and the donor state, which exhibits sp^2 like character, are simply different configurations of the same entity and have a rather large reconfiguration energy of about 0.7 eV.[34] This yields a long emission time constant following capture that is too slow to follow the fast voltage pulse trains used in CP but still able to follow the rather slow voltage ramps in conventional capacitance measurements. Thus, in CP measurements, only CP between either the donor or acceptor state is observed (i.e., a single charge per cycle per trap). We have observed both q and $2q$ charge per cycle (or more generally stated, odd and even numbers for charge per cycle) for the devices in this work. However, more investigation is needed to elucidate the underlying mechanisms.

Nevertheless, these FMCP measurements create an avenue for single-trap measurements in ultra-scaled MOS technology and can, thus, be applied to modern and common MOS technologies where conventional approaches are unable to produce meaningful results. Along with the implication of the continued use of CP as a process/yield monitoring tool, single-trap detection with FMCP is an extremely convenient tool for quantum metrology and quantum engineering applications to support and advance efforts on future computing paradigms and quantum technologies; specifically, understanding the nature of single isolated spins, their interactions with other spins, and the ability to manipulate (or initialize) their spin state. This includes the effort needed to transition our understanding of these types of spin states from traditionally statistical based parameters to one that reflects the true quantized nature of single spin sites. Additionally, single trap CP is a very promising candidate as a vehicle toward a true quantized current (ampère) standard to close the so-called quantum metrology triangle (QMT).[34,38] A quantum mechanical description of Ohm's law, the voltage and resistance experiments are very well defined in terms of the Josephson effect and quantum Hall effect, respectively. The third leg, however, electric current, has not found nearly as much success.[38] The work described in this paper takes the next step toward achieving this goal by demonstrating the relative ease at which single spins can be counted with respect to frequency (the basis of a current standard) in a ubiquitous technology (MOSFETs) widely known for its tremendous scalability and manufacturability.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]P. M. Lenahan, Microelectron. Eng. **69**, 173 (2003).
[2]D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, J. Appl. Phys. **73**, 5058 (1993).
[3]E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (John Wiley & Sons, New York, 2002).
[4]D. K. Schroder, *Semiconductor Material and Device Characterization* (John Wiley & Sons, Hoboken, 2015).
[5]J. Franco, B. Kaczer, M. Toledano-Luque, P. J. Roussel, J. Mitard, L. Å. Ragnarsson, L. Witters, T. Chiarella, M. Togo, N. Horiguchi, G. Groeseneken, M. F. Bukhori, T. Grasser, and A. Asenov, in *IEEE International Reliability Physics Symposium Proceedings* (IEEE, 2012), p. 1.
[6]T. Grasser, Microelectron. Reliab. **52**, 39 (2012).
[7]K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, IEEE Electron Device Lett. **11**, 90 (1990).
[8]M. J. Uren, D. J. Day, and M. J. Kirton, Appl. Phys. Lett. **47**, 1195 (1985).
[9]J. P. Campbell, J. Qin, K. P. Cheung, L. C. Yu, J. S. Suehle, A. Oates, and K. Sheng, in *IEEE International Reliability Physics Symposium Proceedings* (IEEE, 2009), p. 382.
[10]G. Groeseneken, H. E. Maes, N. Beltran, and R. F. D. E. Keersmaecker, IEEE Trans. Electron Devices **31**, 42 (1984).
[11]A. B. M. Elliot, Solid State Electron. **19**, 241 (1976).
[12]S. J. Brugler and P. G. Jespers, IEEE Trans. Electron Devices **16**, 297 (1969).
[13]S. S. Chung, S. J. Chen, C. K. Yang, S. M. Cheng, S. H. Lin, Y. C. Sheng, H. S. Lin, K. T. Hung, D. Y. Wu, T. R. Yew, S. C. Chien, F. T. Liou, and F. Wen, in

IEEE Symposium on VLSI Circuits, Digest of Technical Papers (IEEE, 2002), p. 74.
[14]D. J. Fitzgerald and A. S. Grove, Surf. Sci. **9**, 347 (1968).
[15]A. S. Grove, *Physics and Technology of Semiconductor Devices* (John Wiley & Sons, Berkeley, 1967).
[16]J. T. Ryan, J. P. Campbell, J. S. Suehle, and K. P. Cheung, in *Characterization and Metrology for Nanoelectronics and Nanostructures* (Pan Stanford Publishing, Boca Raton, FL, 2016).
[17]J. T. Ryan, L. C. Yu, J. H. Han, J. J. Kopanski, K. P. Cheung, F. Zhang, C. Wang, J. P. Campbell, and J. S. Suehle, Appl. Phys. Lett. **98**, 233502 (2011).
[18]G. van den bosch, G. V. Groeseneken, P. Heremans, and H. E. Maes, IEEE Trans. Electron Devices **38**, 1820 (1991).
[19]N. S. Saks and M. G. Ancona, IEEE Electron Device Lett. **11**, 339 (1990).
[20]J. T. Ryan, A. Matsuda, J. P. Campbell, and K. P. Cheung, Appl. Phys. Lett. **106**, 163503 (2015).
[21]J. T. Ryan, J. Zou, R. Southwick, J. P. Campbell, K. P. Cheung, A. S. Oates, and R. Huang, IEEE Trans. Electron Devices **62**, 769 (2015).
[22]J. T. Ryan, R. Southwick, J. P. Campbell, K. P. Cheung, A. S. Oates, and J. S. Suehle, IEEE Electron Device Lett. **1**, 2251315 (2013).
[23]P. Masson, J. L. Autran, and J. Brini, IEEE Electron Device Lett. **20**, 92 (1999).
[24]L. Lin, Z. Ji, J. F. Zhang, W. D. Zhang, B. Kaczer, S. de Gendt, and G. Groeseneken, IEEE Trans. Electron Devices **58**, 2122263 (2011).
[25]R. Fernández, B. Kaczer, A. Nackaerts, S. Demuynck, R. Rodríguez, M. Nafría, and G. Groeseneken, in Technical Digest-International Electron Devices Meeting, IEDM (2006).
[26]M. Cho, B. Kaczer, M. Aoulaiche, R. Degraeve, P. Roussel, J. Franco, T. Kauerauf, L. Å. Ragnarsson, T. Y. Hoffmann, and G. Groeseneken, IEEE Trans. Electron Devices **58**, 3342 (2011).
[27]G. T. Sasse and J. Schmitz, IEEE Trans. Electron Devices **55**, 3167 (2008).
[28]Y. Wang and K. P. Cheung, Appl. Phys. Lett. **91**, 133504 (2007).
[29]G. V. Groeseneken, I. de Wolf, R. Bellens, and H. E. Maes, IEEE Trans. Electron Devices **43**, 940 (1996).
[30]N. S. Saks, G. Groeseneken, and I. Dewolf, Appl. Phys. Lett. **68**, 1383 (1996).
[31]N. S. Saks, Appl. Phys. Lett. **70**, 3380 (1997).
[32]T. Tsuchiya and Y. Ono, Jpn. J. Appl. Phys., Part 1 **54**, 04DC01 (2015).
[33]L. Militaru, P. Masson, and G. Guegan, IEEE Electron Device Lett. **23**, 94 (2002).
[34]K. P. Cheung, C. Wang, and J. P. Campbell, Micromachines **11**, 364 (2020).
[35]NIST, 2018 CODATA Value: Elementary Charge-The NIST Reference on Constants, Units, and Uncertainty, 2018.
[36]P. M. Lenahan, J. Vac. Sci. Technol. B **16**, 2134 (1998).
[37]P. M. Lenahan and P. V. Dressendorfer, J. Appl. Phys. **55**, 3495 (1984).
[38]M. W. Keller, Metrologia **45**, 102 (2008).