Alternatives to aluminum gates for silicon quantum devices: defects and strain

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Gate-defined quantum dots (QD) benefit from the use of small grain size metals for gate materials because it aids in shrinking the device dimensions. However, it is not clear what differences arise with respect to process-induced defect densities and inhomogeneous strain. Here, we present measurements of fixed charge, Q_f, interface trap density, D_{it}, the intrinsic film stress, σ, and the coefficient of thermal expansion, α as a function of forming gas anneal temperature for Al, Ti/Pd, and Ti/Pt gates. We show D_{it} is minimal at an anneal temperature of 350 °C for all materials but Ti/Pd and Ti/Pt have higher Q_f and D_{it} compared to Al. In addition, σ and α increase with anneal temperature for all three metals with α larger than the bulk value. These results indicate that there is a tradeoff between minimizing defects and minimizing the impact of strain in quantum device fabrication.

I. INTRODUCTION

Quantum dot (QD) devices in GaAs[1,2], Si[3–6], and SiGe[7,8] have been very successfully fabricated with aluminum gate electrodes. This is due to the relative ease with which thin Al gates can be deposited, lifted off, and isolated from overlapping gate layers with a native or nearly native AlO_x. The need to continue shrinking the dot size below ~ 30 nm, however, has prompted workers to investigate alternative gate materials, such as Ti/Pd whose deposited grain size allows smaller gate dimensions[9–11]. However, while much is known about achievable defect densities for Al processing, the impact of alternative metal processing on defects has not been published. For defects in a metal-oxide-semiconductor (MOS) QD, the fixed oxide charge, Q_f, may change during the deposition process which need not be the same for different materials. Additionally, the ability of a forming gas anneal to repair damage and passivate interface traps will vary with the gate material[12].

A possible secondary benefit of Ti/Pd gates is a reduction in the strain-induced modulation of the conduction band, ΔE_c, at the edge of the gates relative to Al. This is based on a comparison of the bulk coefficients of thermal expansion, α, between the gate and a silicon substrate[9,11]. The ratio $\alpha_{Pd}/\alpha_{Si} \approx \frac{1}{2}\alpha_{Al}/\alpha_{Si}$ in the bulk. However, this comparison ignores the processing of thin films for which $\alpha_{film} \neq \alpha_{bulk}$ and which can incorporate large intrinsic film stress, σ[13,14]. Given differences between Pd and Al such as melting point and density, it is unlikely that their as deposited and post-anneal film stresses are similar in magnitude. Previous studies on Si/SiGe devices with Pd gates[15] have shown that the intrinsic stress can lead to significant potential variations in the quantum well[16], which can adversely affect device operations. Given the above considerations, it is unclear how a shift from Al to Ti/Pd gates shifts the defect and strain landscape of a QD device. Additionally, the potential benefits of small grain size and lower α_{bulk} are not unique to Pd. Based purely on bulk properties, there are a wide array of elemental metals or compounds with grain sizes comparable to that achieved with Pd. For instance, Pt films are very similar to Pd films in as-deposited grain size and Pt has an even lower α_{bulk}[17].

In this work, we address these topics by presenting a comparison of Q_f, D_{it}, σ, and α for Ti/Pd, Ti/Pt, and Al as a function of forming gas anneal temperature and hydrogen concentration. We vary the anneal temperature from 200 °C to 425 °C , using both 5 % and 10 % H_2/N_2 mixtures in 30 minute forming gas anneals. We show that Ti/Pd and Ti/Pt have larger D_{it} than Al when optimally annealed and that the magnitude of Q_f is larger for Ti/Pd and Ti/Pt than for Al, with Al showing a net negative charge while Ti/Pd and Ti/Pt display net positive charge. Additionally, we show that both α and σ increase with increasing anneal temperature. Moreover, these results show that due primarily to intrinsic strain, Pd-gated devices have larger strain-induced modulation of the conduction band than their Al-gated counterparts, directly contradicting expectations based on the bulk α alone[18]. Finally, and most importantly, we find no anneal which simultaneously minimizes defects and the effects of strain in any of the materials studied. Thus, a tension arises in designing fabrication processes for MOS QDs where one must choose between setting the anneal such that defects are minimized or the strain-induced modulation of the conduction band is minimized.

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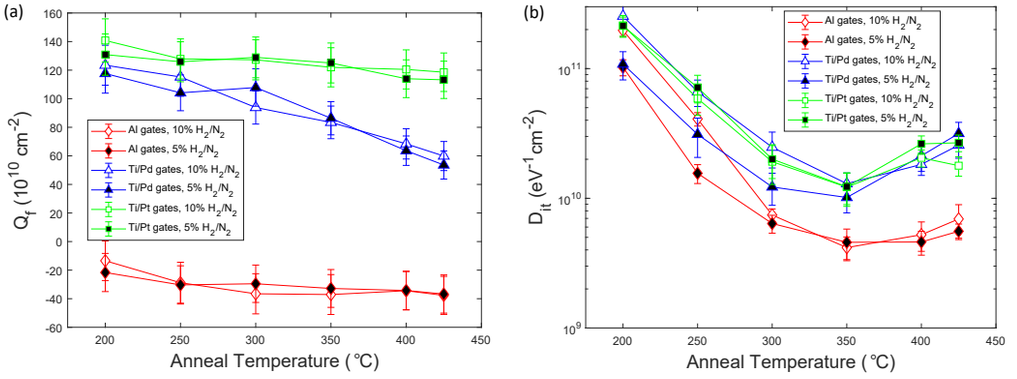

FIG. 1. Plots of the measured oxide defect densities, (a) fixed charge density, Q_f, and (b) interface trap density, D_{it}, vs anneal temperature for Al, Ti/Pd, and Ti/Pt gates in 10 % and 5 % forming gas. Q_f is calculated using the flatband voltage, V_{fb}, extracted from 1 MHz CV curve (not shown). For the V_{fb} data, each point is an average of at least three different MOS capacitors and the standard deviation is propagated into Q_f based on the equation in the main text. The uncertainty in Q_f is dominated by the uncertainty from the UPS measured work functions. D_{it} is measured using the conductance method and the values reported here are the weighted average of D_{it} measured for an energy range in the band gap of $E - E_v = 0.34$ eV to 0.45 eV (see supplemental materials). The minimum D_{it} is reached at 350 °C for all metals. The 10 % and 5 % forming gas anneals shows qualitatively similar behavior with temperature and material. The MOS capacitors fabricated here have gate diameters of 550 μm, 700 μm, and 900 μm, which corresponds to oxide capacitances ranging from roughly 330 pF to 880 pF.

II. DEFECT MEASUREMENTS

To measure the oxide defect densities, we fabricate MOS capacitors with each gate material for capacitance-voltage (CV) and conductance-voltage (GV) measurements. The wafers are boron-doped silicon <100> wafers with a resistivity of 5 Ω·cm to 10 Ω·cm. The wafers are cleaned using standard procedures immediately prior to growing the gate oxide. A roughly 25 ± 1 nm thick gate oxide is grown in a dry oxidation furnace at 1000 °C for 22 minutes with a 10 min post oxidation anneal performed in N_2 at the oxidation temperature. MOS capacitor gates are patterned using negative tone resist (maN-1410) and liftoff in solvent. All of the metals in this work are deposited with e-beam evaporation to mimic common quantum dot device fabrication. For each material, we have used the same deposition rate and pressure: 0.1 nm/s and 4×10^{-4} Pa (3×10^{-6} Torr), respectively. Following deposition and liftoff, isochronal forming gas anneals are performed in an AnnealSys model AS-Master rapid thermal annealer (RTA). The typical ramp-up and ramp-down time ranged from 1 to 3 minutes with both performed in N_2. After annealing, the oxide on the backside of the wafers is removed via a 6:1 buffered oxide etch (BOE) etch and sputtered with Ti/Au to form a low resistance back contact for measurements.

CV and GV measurements are performed using a Keysight E4980A LCR meter in a dark enclosure. We extract the flatband voltage (V_{fb}) from CV curves taken at 1 MHz using the $1/C^2$ fitting method[19]. The fixed charge density is calculated using: $Q_f = \frac{C_{ox}}{eA}(\phi_{MS} - V_{fb})$, where ϕ_{MS} is the metal-semiconductor work function difference. The semiconductor work function is calculated using physical constants, such as the electron affinity and band gap energy for silicon, and the measured substrate doping implied from the slope of the $1/C^2$ plot. Since the thin film metal work function will vary with the processing conditions and properties of the film, we have measured the work function of our films separately using ultraviolet photoelectron spectroscopy (UPS) rather than assuming bulk values[20]. Here, we have performed UPS measurements on representative samples and averaged the resulting work functions from measurements of three different spots for each metal (see supplemental). The interface trap density, D_{it}, is calculated from the peak in the conductance vs frequency data using the statistical model from ref[21] (see supplemental).

Fig. 1(a) and (b) show the results for the fixed charge density and interface trap density respectively as a function of anneal temperature for Al, Ti/Pd, and Ti/Pt gates. There are three important observations to be made from the Q_f data in Fig. 1(a). First, there is an order of magnitude difference in Q_f between the three different gate materials, with Pt the largest overall. This is likely due to differences in the e-beam evaporation process between the different metals. For instance, to produce the same deposition rate, Ti/Pt requires a significantly higher applied power than both Pd and Al, which can increase damage to the oxide[22]. We note that the choice of deposition rate and power may be leading to differences in D_{it} and Q_f presented here rather than specifically just the choice of material. Second, Al shows an overall negative net charge value for all anneals while Ti/Pd and Ti/Pt show net positive charge values. Importantly, the magnitude of Q_f is smaller in Al than Ti/Pt and Ti/Pd. Third, Q_f decreases at different rates with increasing anneal temperature between the three materials. We note that this behavior suggests that there are

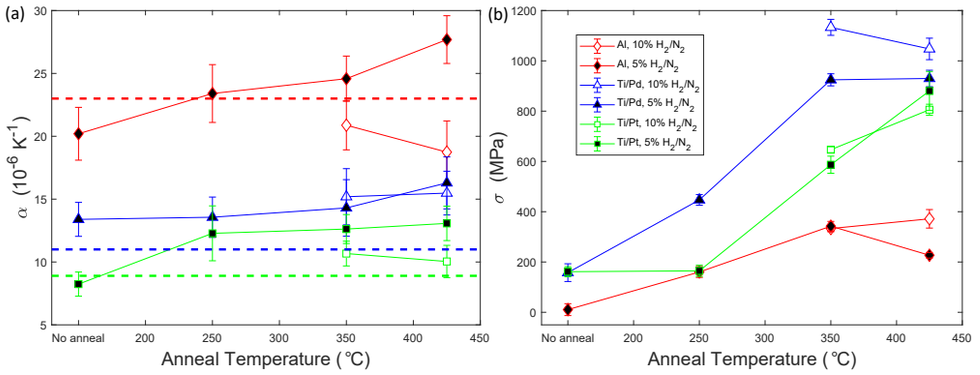

FIG. 2. (a) Measured coefficient of thermal expansion (α) vs anneal temperature for Al, Ti/Pd, and Ti/Pt films. α is measured from the linear fit of stress vs temperature data from 40 °C to 110 °C . We equate the value obtained over this range to the room temperature value of α in each case. The uncertainty represents the 95 % confidence interval from the linear fit. The dashed lines indicate the expected bulk α[17]. (b) Film stress (σ) vs anneal temperature. The intrinsic film stress represents the average measured stress across a 150 mm wafer in 30° increments and the uncertainty is the standard deviation. All films are 50 nm to 60 nm thick and deposited using e-beam evaporation at a rate of roughly 0.1 nm/s with a chamber pressure of 4×10^{-4} Pa (3×10^{-6} Torr).

differences in defects created in the depositions[23,24], but we are unable to confirm this with the present data.

For all the metals, D_{it} (Fig. 1(b)) reaches a minimum value at 350 °C. Above 350 °C , D_{it} begins to increase with increasing anneal temperature. This "reverse anneal" behavior is a well-known effect activated with long anneals and high temperatures[12]. Most importantly, Al-gated devices reach a lower $D_{it} \approx 3{\times}10^9\ eV^{-1}cm^{-2}$ than both Ti/Pd and Ti/Pt where $D_{it} \approx 9 \times 10^9\ eV^{-1}cm^{-2}$. Here, it is important to note that choosing a different anneal time may affect the value of D_{it} obtained, however, differences between gate materials themselves are expected to persist[12]. For both Q_f and D_{it}, we do not see a large difference between anneals performed in 5 % or 10 % forming gas which agrees well with literature results for metal gates[25].

III. WAFER CURVATURE MEASUREMENTS

To measure σ and α, we use a Flexus 2320 wafer curvature measurement tool. The films used for these measurements are blanket films on 150 mm silicon <100> wafers, evaporated using the same conditions as described for the MOS capacitor fabrication. All films are 50 nm to 60 nm thick. To avoid silicide formation during the annealing process affecting the α measurement, the Ti/Pd and Ti/Pt wafers had 25 nm of thermally grown SiO_2. This oxide does not impact the stress measurement since it is present on both sides of the wafer and we use the oxidized wafer to obtain the initial radius of curvature, R_i. The film stress, σ, is calculated using the Stoney equation[26,27]:

$$\sigma = \frac{E_{sub}}{1-\nu_{sub}} \frac{t_{sub}^2}{6t_{film}} \left(\frac{1}{R_f} - \frac{1}{R_i}\right). \quad (1)$$

Here, E_{sub} and ν_{sub} are the Young's modulus and Poisson ratio of the substrate respectively, t_{sub} and t_{film} are the substrate and film thicknesses, and R_i and R_f are the measured radii of curvature in the initial and final state (e.g before and after film deposition or before and after an anneal). The thickness of the substrate and film are both measured, using a thickness gauge and profilometry respectively, and used as inputs to equation 1, where we have assumed the bulk value of E_{sub} and ν_{sub} for the silicon wafers[28].

To measure α_{film}, we step the substrate temperature from 40 °C to 110 °C to avoid any non-elastic deformation, while measuring σ. We fit the resulting data to a line and extract α_{film} through:

$$\frac{\delta\sigma}{\delta T} = \frac{E_{film}}{1-\nu_{film}}(\alpha_{sub} - \alpha_{film}) \quad (2)$$

where α_{sub} is the coefficient of thermal expansion of the silicon substrate, E_{film} and ν_{film} are the Young's modulus and Poisson ratio of the film respectively. We have used the bulk values[17] for these three quantities in our calculation of α_{film}. In our previous work[29], we have shown that this is sufficient for calculating α_{film}.

Fig. 2(a) shows the change in α_{film} at room temperature in the as-deposited state and following forming gas anneals at various temperatures. Each stress value in Fig. 2(b) is the average of six different scans across the wafer 30° apart. For all metals, σ shows increasing tensile stress with increasing anneal temperature. Ti/Pd and Ti/Pt show similar levels of as-deposited stress, between 160-190 MPa. Both Ti/Pd and Ti/Pt experience a large increase (700MPa to 800 MPa) in stress from their as-deposited values to the highest temperature anneal at 425 °C . This increase is significantly more than the 300 MPa increase observed in Al over the same set of anneals. For comparison, the reported stress-thickness

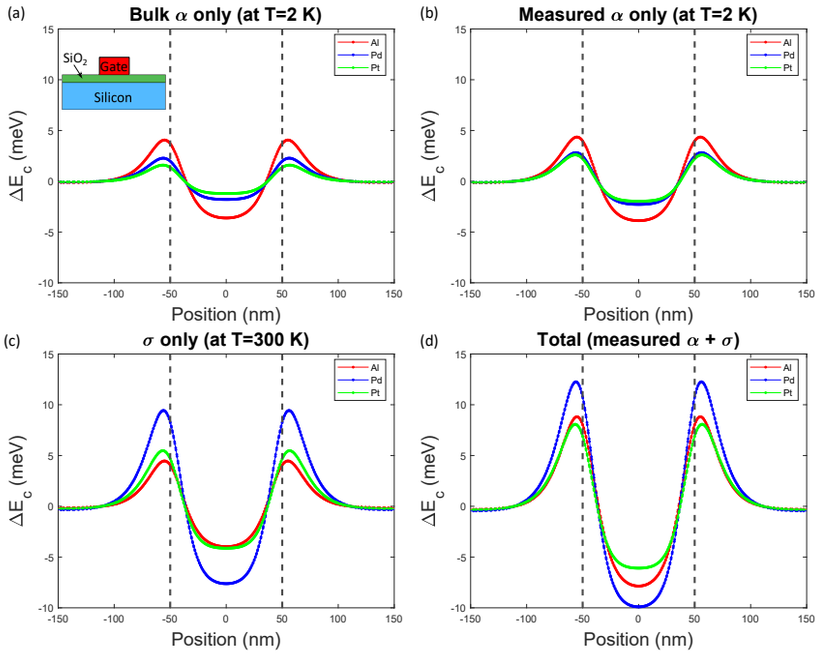

FIG. 3. Simulated conduction band modulation (ΔE_c) due to strain for 100 nm wide metal gate on top of 25 nm SiO_2 on a silicon substrate. (a) ΔE_c due only to the strain generated from the coefficient of thermal expansion, α, mismatch of the gate materials in cooling down from 300 K to 2 K based on the bulk values for each film. The inset shows diagram of the simulated structure. (b) is the same as (a) except we have instead used the measured α values from this manuscript. For each metal, the α used in the simulation is the measured value after a forming gas anneal at 350 °C in 5 % H_2/N_2. (c) ΔE_c due only to intrinsic film stress, σ, for each gate material after a forming gas anneal at 350 °C in 5 % H_2/N_2. (d) Total ΔE_c due to both α and σ. The dashed lines represent the edges of the 100 nm wide metal gate. Due to the significant difference in intrinsic film stress, the Pd films show larger potential modulation than Al and Pt devices.

product for evaporated Pd films used in QD fabrication on SiGe was 80 GPaÅ[16]. For our Pd films, we find a comparable stress-thickness product of 89 GPaÅ ± 13 GPaÅ for the film in the as-deposited state. This suggests that we are producing similar films to those used by other groups fabricating QDs.

Fig. 2(a) shows that α_{film} is generally larger than the bulk value and increases with increasing anneal temperature. Such deviations in elastic properties can be attributed to the micro-structure of the thin film, but we find no clear trend with grain sizes measured in our films via SEM images. For our films, the as-deposited average grain diameters are 43.0 nm ± 1.5 nm, 22.95 nm ± 2.2 nm, and 19.8 nm ± 1.3 nm for Al, Pd, and Pt films respectively. We find that the average grain diameter tends to increase with increasing anneal temperature for the Pd and Pt films, 54.6 nm ± 2.1 nm and 49.6 nm ± 2.1 nm respectively after a 350 C anneal. We find no such trend in the Al films. In the above, the uncertainty is the 95% confidence interval of the mean grain size fit using a log-normal distribution. Since bulk values are typically used to simulate the impact of strain on MOS QD devices[11,30], these α measurements indicate that such simulations do not fully capture the strain in the device[29]. This is especially true given that the most common forming gas anneal temperature is around 400 °C for Ti/Pd gated QD devices[10,11]. We note that we have chosen to use a constant deposition rate of 0.1 nm/s and deposition at room temperature for all materials. This choice impacts the morphology of the film, which may also impact the as-deposited values of the mechanical properties. We are not aware of a consistently reported set of deposition parameters commonly used by groups fabricating MOS QDs.

IV. SIMULATIONS

The large film stresses combined with the deviations of α from bulk values with annealing lead to strain induced modulation of the conduction band that differs significantly from the expectation based on bulk properties. To illustrate the impact of the observed behavior in σ and α_{film}, we perform finite-element modeling of the gate induced strain on the conduction band of silicon using COMSOL[31]. We simulate a single 100 nm wide, 60 nm thick gate on a 25 nm thick SiO_2 layer to mirror the stack for the measurements presented except for the lateral (100 nm) width. For Ti/Pd and Ti/Pt gates, we simulate gates composed of only Pd and Pt respectively as the Ti layer is too thin to measure using wafer curvature methods[32]. Fig. 3 (a) and (b) show the change

in the conduction band, ΔE_c, generated in the silicon substrate 2.5 nm from the SiO_2-Si interface from strain originating from α-mismatch between the metal gate and the silicon when cooled to 2 K. For Fig. 3 (a), we have used the bulk value of α_{film} and in Fig. 3 (b) we use the value of α_{film} measured after the 350 °C anneal in 5 % forming gas. Al shows the largest ΔE_c in agreement with the magnitude of α_{film}. Fig. 3 (c) shows ΔE_c, due only to σ after the same anneal. In this case, Pd gives the largest ΔE_c, reflecting the much larger value of σ. The combined effect of α_{film} and σ is shown in Fig. 3 (d), with Pd showing the largest ΔE_c followed by Al and Pt. Thus, the expectation that moving to Ti/Pd gates from Al gates will reduce the mechanically induced ΔE_c is not supported in this study. From the results of these simulations we can expect that in QD devices, metal films that result in larger total modulations of Ec would have a higher probability of the forming unintentional quantum dots[30] and likely also affect the range of tunnel coupling achievable[4].

V. DISCUSSION

These results show that the fabrication process of silicon MOS QDs must be considered holistically. The choice of gate material, deposition parameters, and anneal parameters impacts lithographic fidelity, threshold voltage, defect densities, strain and perhaps more properties of QD devices. The evolution with anneal temperature we have presented here makes clear that the negative impacts of charge defects and mechanical effects cannot be simultaneously minimized. Given the behavior in Fig. 2 one might be tempted to perform the forming gas anneal prior to any gate metal deposition. This would still allow passivation of the interface traps originating from the oxide growth while avoiding exposing the metal film to any anneals after deposition. Nominally, this procedure minimizes the impact of mechanical effects and charge defects generated as part of the oxide growth. However, it leaves unpassivated any defects created by the metal deposition so that the overall defect density would not truly be minimized. This forces a significant choice in fabrication process design. This choice is displayed most clearly in the observation that, of the gate materials studied, Pt has both the smallest ΔE_c and the largest overall Q_f when annealed to minimize D_{it}. Of the materials studied, Al appears to be best with respect to a minimized D_{it}, a smaller magnitude of Q_f, and nearly ΔE_c from strain. It also affords a convenient inter-gate dielectric. However, the native oxidation of Al gates may itself lead to a negative impact on QD performance with increased noise[8,33] and from the distorted shape of the gate[9] as well as its direct mechanical effects, which are not well studied. Were it not for the larger grain size in the deposition it could still remain the clear choice among the materials studied.

We have shown the impact on defects and strain as a result of moving to Ti/Pd or Ti/Pt gates for MOS QDs with commonly used fabrication methods. The magnitude of charge defects, α-induced and σ-induced stress are highly dependent on the choice of deposition process, anneal temperature, and material. These results indicate three potential paths in MOS QD fabrication processes to move beyond the issues discussed above. First, e-beam deposition parameters should be evaluated with respect to D_{it}, Q_f, α, and σ similarly to the present study. Second, metal deposition techniques other than thermal or e-beam evaporation should be explored. For instance, low energy sputtering techniques, like ion beam deposition, could be used to produce films with different grain structures, which could modify mechanical effects while minimizing deposition-induced defects. Third, the observation above that Pt has the lowest strain modulation contrasted with the highest charge defect density motivates the exploration of gate materials outside of the three we presented here and those typically used in other work. This might include metals like TiN, which has recently been used in QD fabrication[34,35]. It is clear from our work that the choice of material itself is a significant factor in determining the final mechanical and electrostatic properties and that the mechanical impact is not immediately obvious based solely on commonly used bulk mechanical values. The defect measurements presented here were performed at room temperature while all QD devices will operate at cryogenic temperatures. Ultimately, it will be important to tie the results of this study and similar ones to MOSFET measurements of D_{it} performed at cryogenic temperatures as well as aspects of quantum device performance.

SUPPLEMENTARY MATERIAL

See supplementary material for details of the calculations of the average interface trap density, UPS measurement setup, and an example of the raw data used to measure the thin film coeffiecent of thermal expansion.

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DISCLAIMER

Certain commercial equipment, instruments, and materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology,

nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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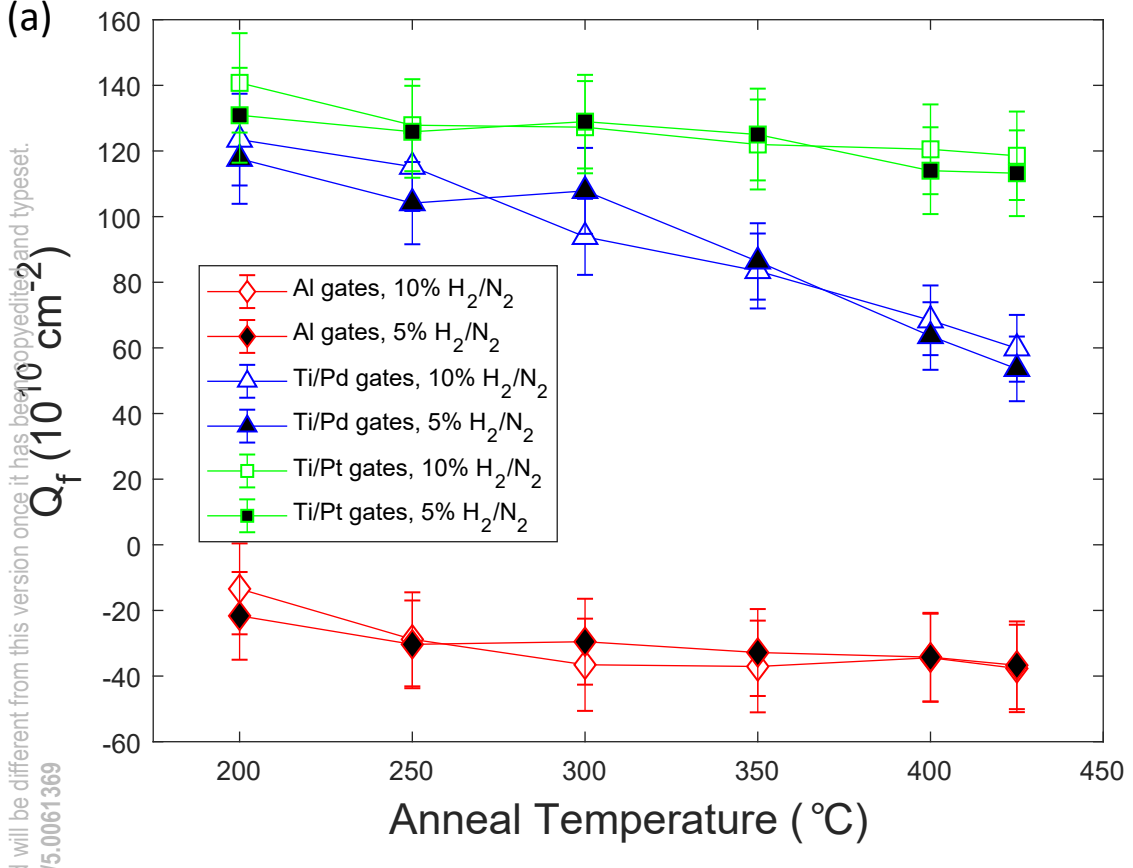

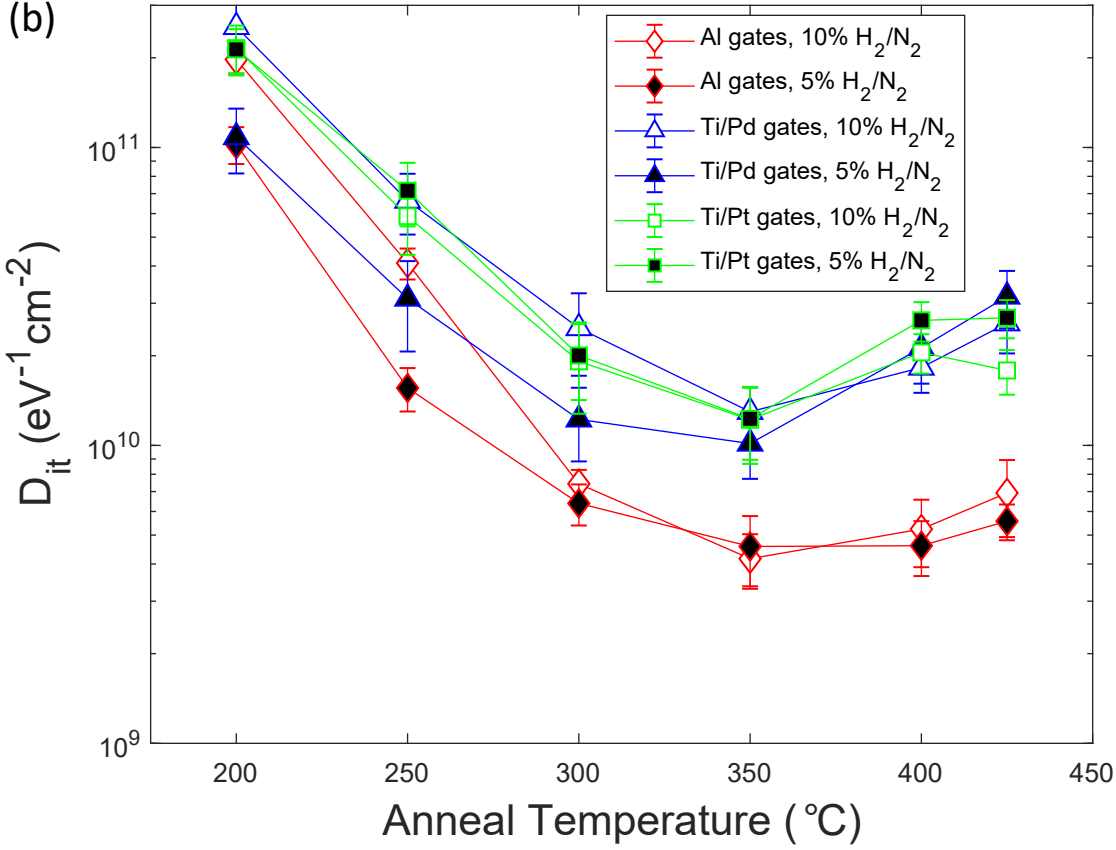

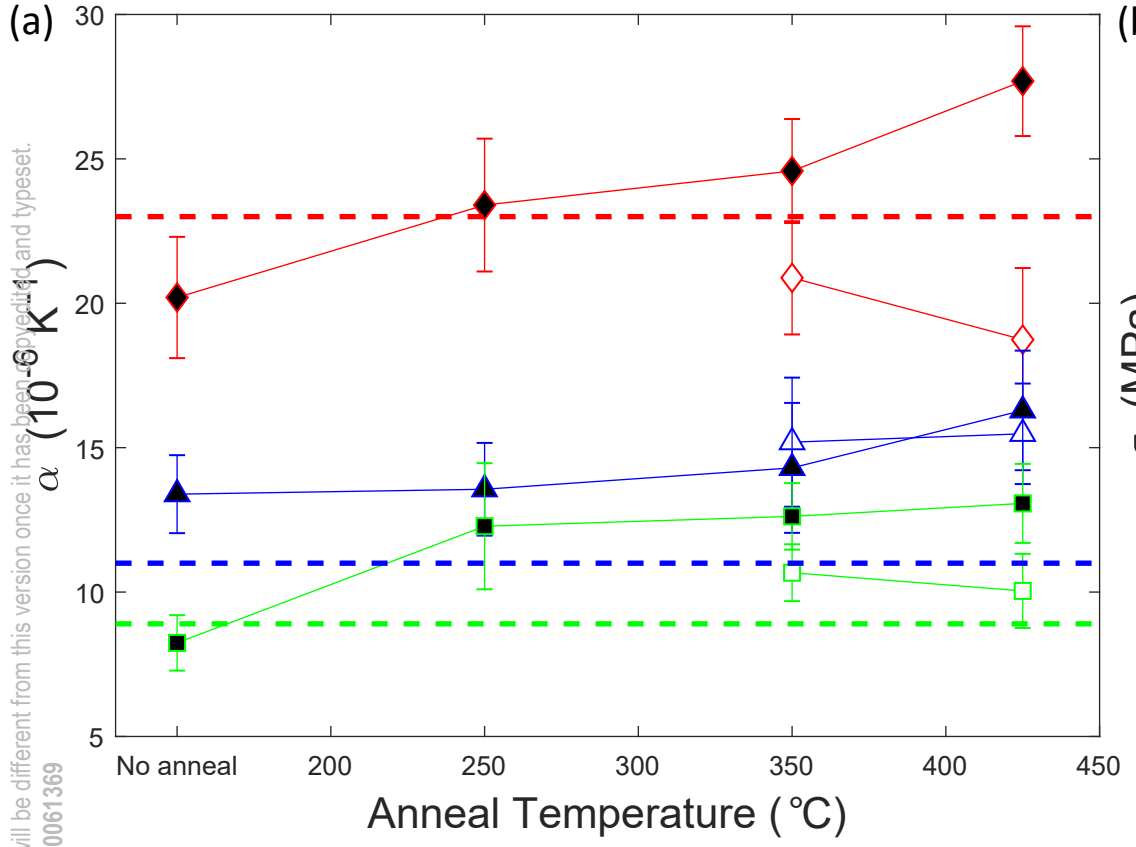

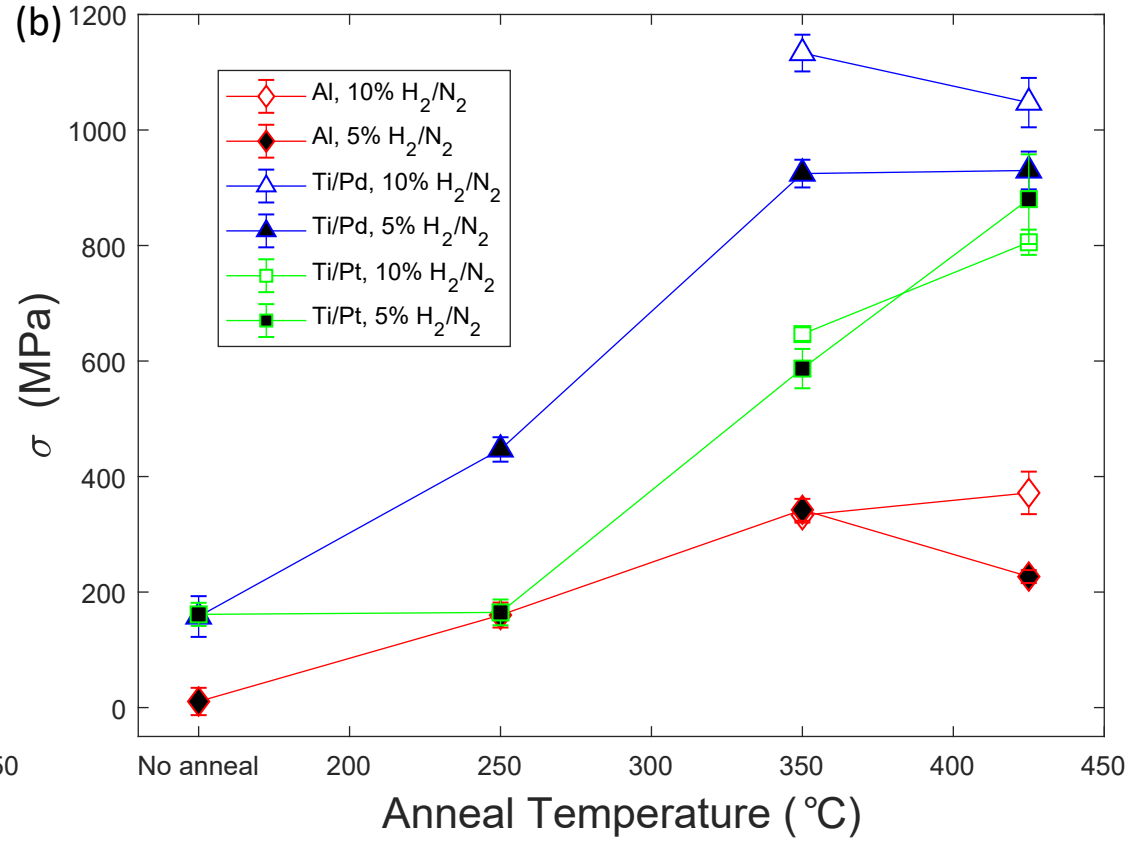

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