

# Programmable System on Chip for controlling an atomic physics experiment

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Most atomic physics experiments are controlled by a digital pattern generator used to synchronize all equipment by providing triggers and clocks. Recently, the availability of well-documented open-source development tools has lifted the barriers to using programmable systems on chip (PSoC), making them a convenient and versatile tool for synthesizing digital patterns. Here, we take advantage of these advancements in the design of a versatile clock and pattern generator using a PSoC. We present our design with the intent of highlighting the new possibilities that PSoCs have to offer in terms of flexibility. We provide a robust hardware carrier and basic firmware implementation that can be expanded and modified for other uses.

## I. INTRODUCTION

Laser-cooled atoms, ions, and molecules are interesting and dynamic systems to study, and are being used to develop many quantum technologies. These technologies include precise atomic clocks<sup>1,2</sup>, quantum computers and simulators<sup>3,4</sup>, and quantum sensors<sup>5,6</sup>. Experiments in atomic, molecular, and optical (AMO) physics are often a combination of a large number of commercial or custom-made instruments from different sources and manufacturers that need to operate synchronously and in a repeatable fashion. Synchronization is achieved by using a specialized software suite to control a primary digital pattern generator or clock device with deterministic timing that sends trigger signals to the other hardware devices. The PulseBlaster by SpinCore<sup>7</sup>, a commercial device based on a field programmable gate array (FPGA), is commonly used as a primary clock in many AMO experiments<sup>8</sup> and is compatible with many different software suites. Many university groups have also designed custom-made devices based around a microcontroller or an FPGA as their primary clock. Microcontrollers combine processing power with many peripherals for interfacing directly with hardware, and have found use in a wide variety of physics experiments<sup>9-12</sup>. On the other hand, FPGAs provide versatility in modifying the overall system architecture to accommodate changes in functionality, although they require more expertise for development. Despite the steeper learning curve, FPGAs have become a common choice as a control device in many physics experiments and work extremely well to accommodate more complex architectures, as well as modular ones<sup>13-17</sup>.

Another approach for controlling experiments is to create a complete infrastructure of software and modular hardware that is designed with built-in timing synchronization. Two commercial examples of this approach are

LabView, a systems engineering software that is compatible with National Instruments hardware, and ARTIQ by M-labs<sup>18</sup>, which is also a complete infrastructure of software and hardware. Some university research groups have also created complete architectures, basing their hardware designs off of FPGAs and designing custom control software<sup>14,16</sup>.

While FPGAs can work well as a primary control device for an experiment, microcontrollers offer a simpler solution for handling complex communications protocols such as USB (Universal Serial Bus) or Ethernet. Often, a microcontroller is used in conjunction with an FPGA, either externally<sup>8</sup> or instantiated within the FPGA<sup>18</sup>. An alternative approach is to use a programmable system on chip (PSoC), which combines an FPGA and a high performance microprocessor on a single chip. This allows implementation of operating systems, advanced communication protocols, and high level language interpreters in the microprocessor, leveraging the FPGA when hardware acceleration or control of dedicated peripherals is needed. Previously, development using PSoCs has been less accessible due to the baseline level of expertise required, but recently, thanks to the diffusion and level of maturity of tools such as PetaLinux<sup>19</sup> or Yocto Project<sup>20</sup> for the generation of GNU/Linux images, PSoCs have become more widely adopted<sup>21,22</sup>.

We chose a PSoC architecture to design our 64-channel pattern generator and primary clock with the goal of expanding the capabilities of our ultracold strontium experiment. Our requirement, to have a large number of channels operating in parallel with fast (100 ns resolution) and deterministic timing, points towards an FPGA as the platform of choice; however, we also had the goal of handling most of the data communication protocols using high level abstraction languages, such as Python, to facilitate testing and future rapid development. To achieve these goals, we take advantage of the PYNQ (Python Productivity for Zynq) infrastructure<sup>23</sup>, a platform for the development of applications with the Xilinx Zynq series of programmable systems on chip based on GNU/Linux and Python. Our lab uses the Labscript Suite of software<sup>8</sup> to control our experiment, which uses

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a text and GUI approach to provide efficient experimental control for atomic physics experiments and is based on the Python programming language. We designed a hardware platform around a Microzed Zynq-7020 module<sup>24</sup> (produced by Avnet) mounted on a custom carrier board with four low-jitter input trigger lines and eight breakout boards with eight channels each to route the 64 output lines. The FPGA gateware is written in Verilog and System Verilog, and we used Xilinx native development tools in order to make use of the many verification features, such as complex testbenches for behavioral simulation. In the next sections, we will describe the system architecture as a whole, as well as describe the hardware and firmware in detail.

## II. SYSTEM OVERVIEW

Fig. 1 illustrates the overall architecture of our design, which can be broken down into three blocks: our host PC (or lab control computer), the Microzed-7020 module, and the carrier and breakout boards. The Microzed module contains the Xilinx PSoC and a series of additional peripherals, of which we show only the most relevant to our project: the I/O connectors to interface with the carrier board, 1 GB of synchronous dynamic random access memory (SDRAM), and an Ethernet physical layer chip (PHY) used for communication with the host PC. The PSoC (Xilinx XC7Z020-1CLG400C<sup>25</sup>) is composed of the processing system (PS) and the programmable logic (PL). The PS is a dual core ARM Cortex-A9, while the PL is an Artix-7 FPGA fabric with approximately 85000 logic cells.

The PYNQ ecosystem allows us to run Linux Ubuntu on the PS and is equipped with a Jupyter notebook server accessible from a remote machine browser as a means to interact with the PL using a Python application programming interface (API). Through the API, the PL can be accessed using extended multiplexed input/output lines (EMIO) or an AXI-lite (Advanced eXtensible Interface) channel that can be used to map configuration registers in the PL to the operating system’s RAM. Additionally, the SDRAM external memory used by the operating system can be accessed using a direct memory access (DMA) controller.

The heart of our design is in the PL, where we implemented a state machine written in System Verilog which reads instructions from RAM instantiated in the FPGA fabric. The RAM is limited to  $2^{15} = 32768$  instructions. To allow for a longer list of instructions, we have implemented a ping-pong memory controller that moves data from the external SDRAM to the PL RAM through the DMA channel. The state machine and ping-pong memory controller will be discussed in further detail in Sections IV B and IV C, respectively.

In the PS, we wrote an application server in Python to receive instructions from the host PC through a socket connection, transferring them to the shared SDRAM

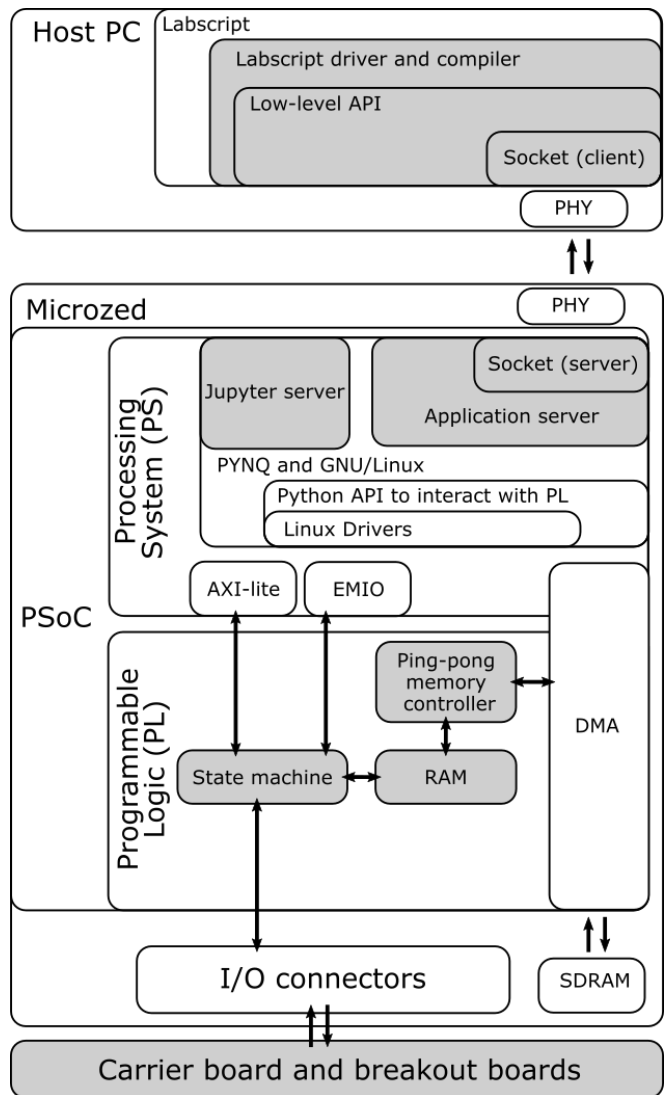


FIG. 1. Overall schematic of the pattern generator. For convenience, we summarize acronyms used in the figure: PC (Personal Computer), API (Application Programming Interface), PHY (PhYsical interface), PSoC (Programmable System on Chip), PS (Processing System), PL (Programmable Logic), AXI (Advanced eXtensible Interface), EMIO (Extended Multiplexed Input/Output), DMA (Direct Memory Access), RAM (Random Access Memory), I/O (Input/Output), SDRAM (Synchronous Dynamic RAM). Elements of the system we designed in detail are shown in gray, while the white blocks are the components and software that are available as commercial modules, open-source libraries, or automatic software generation tools.

and initiating DMA transfers. The application server is paired with a socket client running on the host PC, also written in Python, which acts as a low-level API to interface the Labscript instrument driver with the Microzed module.

The Microzed board plugs into a custom-designed carrier board using MicroHeader connectors. The output signals are then routed through eight breakout boards

and are accessible via BNC (Bayonet Neill–Concelman) connectors. The carrier board and breakout board designs are described in Sec. III.

### III. HARDWARE FEATURES

#### A. Carrier Board

The carrier PCB (Printed Circuit Board) routes the 64 digital output lines from the expansion connectors of the Microzed module (Amphenol ICC 61083-101400LF) to eight 20-pin rectangular connectors, which are used to distribute the signals to the breakout boards using ribbon cables. Placement of the 20-pin rectangular connectors was determined to keep the difference in length between all traces below 12 mm. The resulting maximum difference in propagation time between channels is estimated to be only  $\approx 64$  ps, which is well within the goals of our design. The carrier board also has four BNC connectors for introducing input clock or trigger signals to the Microzed. In order to adapt arbitrary trigger and clock standards to the FPGA input standards, each BNC input is connected to the analog front end circuit shown in Fig. 2(a). Input signals are sent through a high speed comparator chip (ADCMP552BRQZ<sup>26</sup>) with PECL (Positive Emitter-Coupled Logic) outputs. We set a 1 V threshold on the inverting input of the comparator using a voltage divider filtered with a 0.1  $\mu$ F capacitor, and we connect the coaxial input to a network of components (R1, R2, R3, C1, C2) that can be used to adapt a variety of AC (Alternating Current) or DC (Direct Current) input waveforms. R1 is used as jumper to select between DC and AC inputs. In the default DC-coupled configuration, R1 = 0  $\Omega$  and R3 = 50  $\Omega$ , making the input compatible with 3.3 V and 5 V TTL (Transistor Transistor Logic) standards. For an AC-coupled configuration, R1 is not placed, C1 = 0.1  $\mu$ F to block DC signals, and the values, R2 = 294  $\Omega$  and R3 = 60.4  $\Omega$ , set the input impedance to 50  $\Omega$ , maintaining an average voltage of 0.85 V at the input of the comparator. The carrier board also provides a 3.3 V supply for the I/O banks of the PSoC with two high-efficiency micro DC-DC converters (XCL214<sup>27</sup>), and a supervisor chip (STM6779LWB6F<sup>28</sup>) ensures that the required power sequencing for the PSoC is respected<sup>29</sup>.

#### B. Breakout Boards

The eight breakout boards use a Texas Instruments octal buffer (SN74S244DWG4<sup>30</sup>) to drive 5 V TTL signals through 50  $\Omega$  coaxial cables. The electrical schematic for a single channel is shown in Fig. 2(b). The ribbon cable connecting the carrier board with the breakout board has an alternating pattern of GND lines and digital signal lines, which prevents crosstalk and sets a characteristic impedance of 50  $\Omega$ . The ribbon cable also carries a

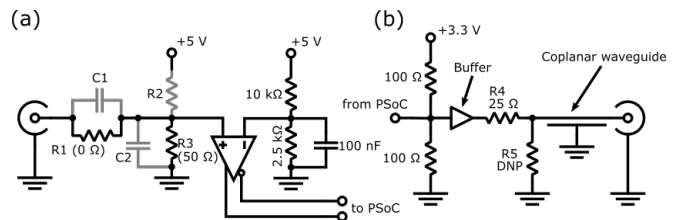


FIG. 2. Termination networks used to interface the FPGA logics with external signals. (a) shows the circuit used for the four digital inputs on the carrier board while (b) shows the circuit used for the 64 digital outputs.

3.3 V supply used for termination and a 5 V supply used to power the octal buffer. The two 100  $\Omega$  resistors in Fig. 2(b) terminate the single-ended line from the PSoC to a Thevenin equivalent of 50  $\Omega$  at half the logic supply. This type of termination is called split termination and is described on page 26 of the Xilinx UG471 user guide<sup>31</sup>. Each output of the octal buffer has an internal impedance of 25  $\Omega$ , and therefore a series resistance of 25  $\Omega$  (R4) is added in order to bring the output impedance to a standard value of 50  $\Omega$ . The additional DNP (do not place) resistor (R5) can be used in conjunction with a different value for R4 to produce an arbitrary Thevenin equivalent output that maintains a 50  $\Omega$  impedance, allowing the user to configure the outputs to different logic standards. For example, the values R4 = 75  $\Omega$  and R5 = 100  $\Omega$

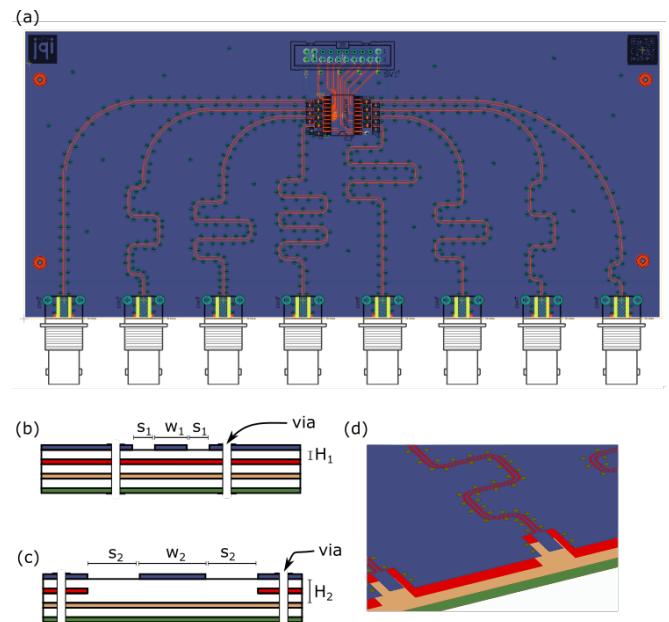


FIG. 3. (a) Breakout board layout. Signals enter the board through the 20-pin connector at the top. Meanders help equalize electrical delays of all traces. (b) Stack-up of the PCB for the coplanar waveguide (c) Stack-up of the PCB for the microstrip below the BNC connector. (d) Close-up perspective view of the circuit board layout. Figure is not to scale.

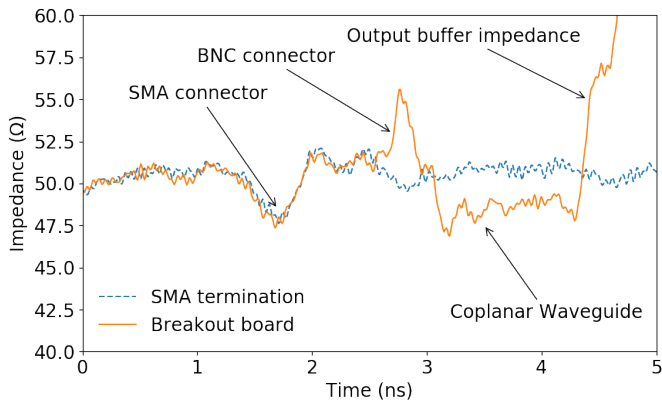


FIG. 4. Time Domain Reflectometry measurement of the breakout board. The characteristic impedance of the BNC connector and coplanar waveguide remain within 10% of the  $50\ \Omega$  target value.

would reduce the output voltage by a factor of 2. The coplanar waveguide in Fig. 2(b) is designed with a target impedance of  $50\ \Omega$  using the Kicad PCB calculator<sup>32</sup> software.

Fig. 3(a) shows how the eight coplanar waveguides are arranged on the breakout board. To prevent variations in the timing delay across different output channels, we have matched the length of all 8 traces using meanders. Based on the information provided by the PCB manufacturer (nominal relative dielectric constant  $\epsilon_r = 4.3$ ), we designed the coplanar waveguide, as illustrated in Fig. 3(b), with a width  $W_1 = 0.46\ \text{mm}$ , spacing between traces and top-layer ground plane  $S_1 = 0.3\ \text{mm}$ , and separation from top-inner-layer ground plane  $H_1 = 0.24\ \text{mm}$ . We chose edge-mount BNC connectors rated up to 4 GHz to minimize the characteristic impedance discontinuity from the PCB to the coaxial cables. For impedance matching, the connectors need to be soldered to a microstrip that ends at the edge of the PCB. However, to ensure an adequate mechanical strength for the connector’s central pin soldering joint, the width of the microstrip must be much larger than the width  $W_1 = 0.46\ \text{mm}$  of the coplanar waveguide in Fig. 3(b). To allow for a wider section of the transmission line, we therefore remove the inner-top ground layer from under the central pin’s soldering pad, as shown in Fig. 3(c). Using the inner-bottom layer as the new ground plane, the distance from the transmission line is increased to  $H_2 = 1.26\ \text{mm}$ . A nominal  $50\ \Omega$  impedance is now obtained with  $W_2 = 2.29\ \text{mm}$  and  $S_2 = 1.27\ \text{mm}$ . A perspective view of the PCB layers is shown in Fig. 3(d).

We verified the performance of the transmission lines and BNC launch by performing a time domain reflectometry (TDR<sup>33</sup>) measurement on the PCB. The result of the measurement is shown in Fig. 4, where we use the technique described in Ref.<sup>33</sup> to measure the amplitude of a reflected step signal to calculate the characteristic impedance along a transmission line as a function of electrical delay. We first measure the response of a coaxial

cable with an SMA (SubMiniature version A) connector attached to a SMA  $50\ \Omega$  termination. We then connect the coaxial cable to our PCB board, while not powered, using a SMA to BNC adapter and compare the two TDR responses. Four different sections can be distinguished in the traces in Fig. 4: the SMA connector, the BNC adapter, the coplanar waveguide on the PCB, and the output buffer passive impedance. Apart from the output buffer, which shows a change of impedance compatible with a capacitive load, the maximum impedance variation for the BNC connector and coplanar waveguide design is below  $\approx 10\%$ , limiting reflections below  $\approx 5\%$ .

## IV. FIRMWARE DEVELOPMENT

### A. Communication

To communicate instructions to the PSoC, we open a socket server on the PS. We then wait for the TCP/IP client on the lab computer to connect. Once the connection is established, data is sent through the socket stored in a numpy array<sup>34</sup>, which is mapped on a contiguous section of SDRAM shared with the PL through a DMA controller. The data is then accessed by the PL and processed by the state machine as instructions in a 128 bit format extension of the 80 bit long instruction format used in the PulseBlaster<sup>35</sup>. In case the connection is unexpectedly broken, we have implemented an algorithm for the server to automatically refresh the same socket connection, instead of creating a new one. This makes the system robust against the interruption of the connection without having to manually reset it.

### B. State Machine

To control the 64 TTL output channels, we have written a Mealy<sup>36</sup> state machine in the programmable logic of the FPGA. In contrast with Moore<sup>37</sup> state machines, Mealy state machines’ inputs directly affect the outputs, allowing for a lower-latency design. We wrote our state machine in System Verilog to take advantage of specialized features of the language, such as enumeration logic and the passing of structured data through design modules. The state machine first fetches 128 bit instructions from a  $128 \times 32768$  RAM, mapped as shown in Fig. 5. There are five fields that make up the 128 bit instruction to the state machine: time delay (32 bits), data (20 bits) opcode (4 bits), flags (64 bits) and finally the remaining 8 bits are reserved for future use. The state machine reads the memory bank row by row. The opcode tells the state machine which state to enter next, and the flags field designates which output channels will be changed or affected with each instruction. The data contains any special information specific to the current opcode. For example, if the state machine is being instructed to enter a loop, the

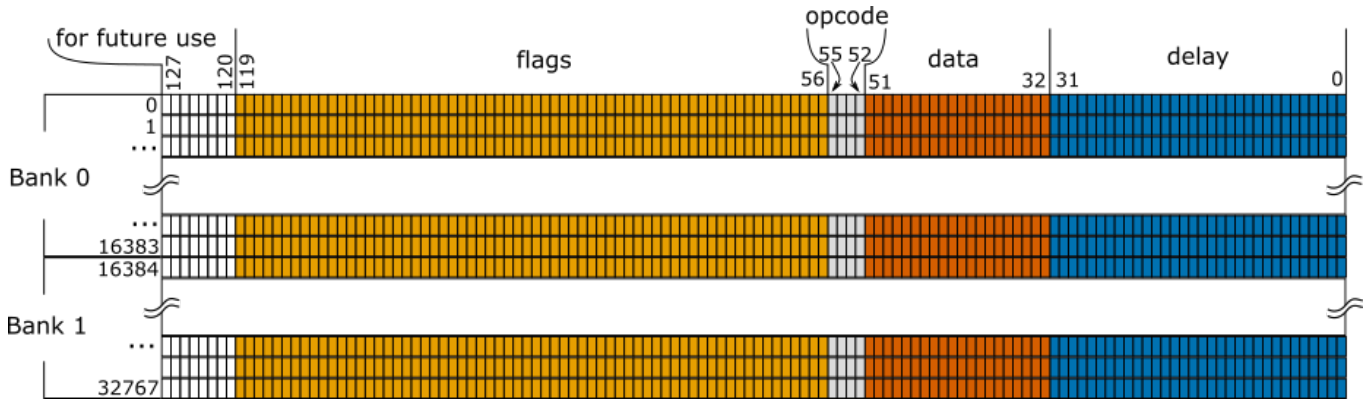


FIG. 5. Illustration of the memory in the FPGA. The memory is split into Bank 0 and Bank 1, each with 16834 instructions. The memory has a width of 128 bits. Each instruction contains 64 bits for the state of each of the flags, 4 bits for the opcode, 20 bits for the data argument, and 32 bits for the time delay argument. The last 8 bits are left unused, but can be allocated in the future.

data would contain the number of loop iterations. Finally, the ‘delay’ argument indicates how long the state machine should wait before loading the next instruction. The states that we have programmed in our state machine are shown in Table I, along with the accompanying ‘data’ field. To facilitate integration with Labscript, we choose an instruction set that is mostly compatible with the one of the Pulseblaster, which is extensively used

within the Labscript codebase (we did not implement nested loops, as they are not used in Labscript).

### C. Ping-Pong Memory

The state machine described in the previous section is designed to read instructions from a 32768-instruction static memory. To increase the available memory, we use the 32768-instruction space as a cache memory and divide it into two banks with  $2^{14} = 16384$  instructions each: Bank 0 and Bank 1, as shown in Fig. 5. We then implement a ping-pong memory controller to automatically update the content of the memory by requesting direct memory access (DMA) to a large shared contiguous portion of the SDRAM, which has space for up to 8192000 instructions. The algorithm for the ping-pong memory controller is shown in Fig. 6(a). The controller begins by transferring 16384 instructions from SDRAM into Bank 0 of the PL RAM and setting a register called “last\_bank” equal to 1. The main state machine then begins executing instructions from RAM, starting from Bank 0, while the ping-pong memory controller constantly monitors the memory address. Each time the memory address is not in the bank identified by the register “last\_bank”, the previously accessed bank is refreshed with new data from the SDRAM and the value of “last\_bank” is updated with the identifier of the currently accessed bank. Setting “last\_bank” equal to 1 when the state machine starts causes Bank 1 to be updated immediately after Bank 0 as soon as the state machine accesses the memory. The PL RAM is a dual port memory that can be independently addressed from two different clock domains. Thus, the state machine controlling the 64 TTL outputs does not need to be synchronous with the rest of the PL and with the PS. The ping-pong memory controller and DMA engine are clocked by the PS, while the state machine can be optionally clocked from one of the PLLs (Phase Locked Loop) available in the PL fabric that can be locked to an

State	Instruction	Data	Function
0	CONTINUE	None	Continues to next instruction
1	STOP	None	Stops execution of program
2	LOOP	Number of desired loops, great than or equal to 1	Specifies beginning of loop
3	END LOOP	Address of beginning of loop	Specifies end of loop
4	JSR	Address of first subroutine instruction	Jumps to a subroutine
5	RTS	None	Program execution returns to instruction after JSR was called at the end of subroutine
6	BRANCH	Address in memory to branch to	Program execution branches to an address specified by data
7	LONG DELAY	Delay multiplier	Executes the length of instruction given in the time field multiplied by delay multiplier
8	WAIT	None	Waits for a hardware trigger to continue program execution

TABLE I. List of states that was programmed in the state machine with associated data field and description of the function performed. The state numbering corresponds to the associated opcode.

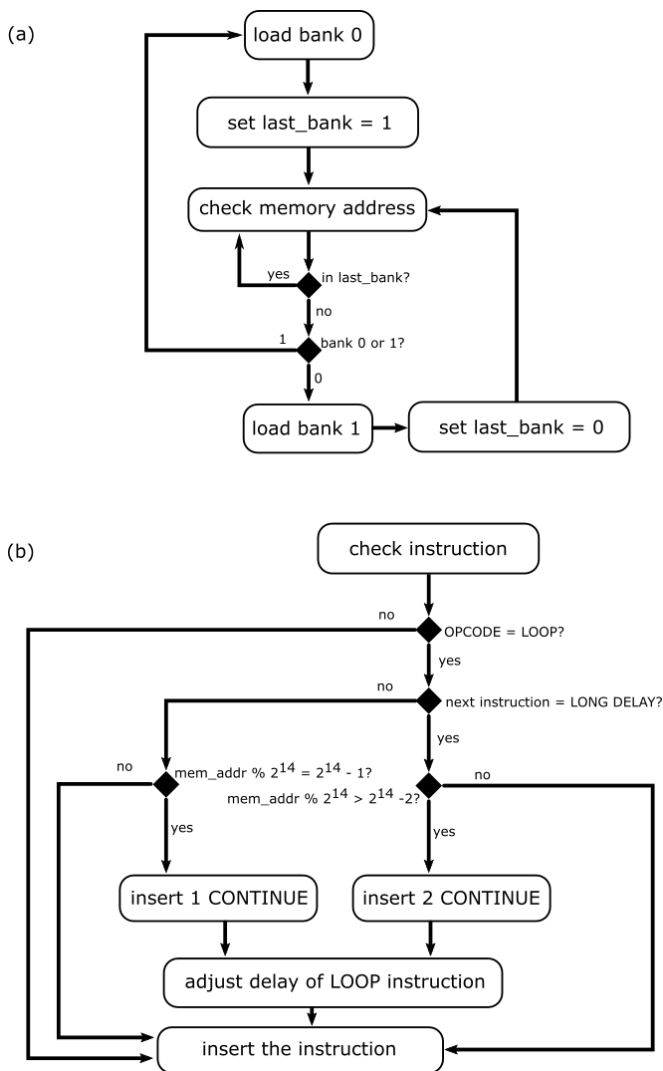


FIG. 6. Bank switching and compiler check algorithms for the ping-pong memory controller. (a) The system begins by loading bank zero and setting the “last\_bank” to Bank 1. From there, the system consistently checks the memory address of the state machine to determine whether it has switched banks in the memory. If it has switched banks, it changes “last\_bank” and loads the other bank of memory with new instructions. (b) Checks performed during compilation to avoid memory underflow. The logic expressions  $\text{mem\_addr} \% 2^{14} > 2^{14} - 2$  and  $\text{mem\_addr} \% 2^{14} = 2^{14} - 1$  check, respectively, if  $\text{mem\_addr}$  is mapped to the last two slots or the last slot in the memory bank (% is the MOD operator).

external reference connected to one of the four available BNC inputs.

The automatic RAM refresh implemented by the ping-pong memory controller can pose a problem if certain instructions span over two banks, such as LOOP/END LOOP, BRANCH, JSR/RTS. For example, if a loop is started in the first bank, but ends in the second bank, since the first bank is updated with new instructions while the second

bank is running, the system will no longer have the initial loop instruction to refer back to. The compiler must be aware of this type of memory underflow or overflow and be able to resolve them by altering the order and number of instructions, without changing the final behavior at run time. In the current Labscrip driver, there is only one instance where underflow can happen: when the complex instruction called “reps” is translated into either a LOOP immediately followed by an END LOOP instruction or a series of LOOP, LONG DELAY, END LOOP. To prevent memory underflow, we have implemented checks in the code while the program is compiling. The algorithm is illustrated in Fig. 6(b). When a LOOP opcode is found, the system checks if either the instruction is mapped on the last instruction of a bank or if it is mapped on the second to last and is immediately followed by a LONG DELAY instruction. In these cases, it inserts additional CONTINUE instructions to ensure that the LOOP instruction is moved to the beginning of the next bank. To ensure that the insertion does not modify the original timing, the field ‘delay’ in the LOOP instruction is reduced by the duration of the inserted CONTINUE instructions.

## V. DISCUSSION

The PSoC-based primary clock device, that we have created for controlling AMO physics experiments, is easily integrated with the Labscrip Suite. The hardware provides 64 buffered digital outputs for controlling other hardware devices and also 4 input trigger channels. The printed circuit board design ensures signal integrity and minimal crosstalk between channels. Our firmware design implements a state machine written in System Verilog and a ping-pong memory controller that allows the execution of a large number of instructions (exceeding 8192000). The system is currently being used to run the entire experiment in our lab, providing triggers for digital to analog converters (DAC), digital direct synthesizers (DDS), mechanical shutters, and many other instruments.

According to the Synthesis tools timing reports the maximum frequency the state machine can operate at is 104 MHz, and it is currently clocked at 100 MHz. Therefore, the current timing resolution is 10 ns, although using serializers in the PL fabric would allow timing resolutions down to 1 ns. The versatility of the platform also allows for other modifications, such as the possibility to add additional instructions to the state machine. For example, an additional instruction could initiate a train of a specific number of pulses with an adjustable duty cycle and period using a single instruction, rather than using loops. Other extensions of the instruction set could allow for conditional branching, which has already been shown to be useful in ion trapping experiments<sup>38</sup>. Further modifications to the design might include network security protocols and encryption for data transmission, which we have not included since our setup is running

on an isolated network. A possible use of the system we have considered, and have extensively taken advantage of during testing, is its capability to run scripts directly from the local Jupyter notebook server. With the Jupyter web interface, a remote computer is not necessary for the generation of patterns, and the device can be used as a stand-alone testbench digital pattern generator.

Our PSoC-based primary clock device has the capability to be integrated with many experimental setups with minimal modification, and the whole design is available online<sup>39</sup>.

## ACKNOWLEDGEMENTS

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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