Gate resistance thermometry: An electrical thermal characterization technique

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9.1 Introduction

Gate resistance thermometry (GRT) is a characterization technique to determine the average temperature of the gate metal in GaN transistors. Implied in the name itself, the electrical method is based up on measuring the change in resistance of the gate metal during heating [1,2]. Since many electrical characteristics are temperature dependent [3], several different electrical methods have been reported in literature [4–8]. Upon review, each method represents a spatially averaged temperature across a different area of the transistor [9]. For example, Kuzmik's method [5] represents the average temperature of the source-gate region, while McAllister's method [6] represents the average source-drain temperature. Due to the complex joule heating profile generated in GaN HEMTs, however, the temperature gradient across a single device can be as large as 60°C [10]. Therefore, both the location and the area over which an electrical technique averages a temperature can result in significantly different values. Noting that the highest temperature in the device is typically found near the gate footprint, GRT is found to be one of the more suitable electrical methods to estimate the peak temperature in the GaN HEMTs. In addition to its location, GRT is also less susceptible to trapping effects or current collapse, which may develop at high voltages and affect the temperature measurement's accuracy [8,11].

Another advantage of employing GRT over other electrical methods is its ability to perform in situ measurements. For electrical DC methods, such as *I-V* sweeps, the device must be switched briefly off to perform the measurement [7]. In contrast, GRT can be applied during operation to monitor the in situ temperature. To reduce the acquisition time of these other DC methods, pulsed IV measurements have been employed to shorten the measurement time to sub-microseconds [7]. These methods, however, still incur and error associated with fast switching and leakage currents.

Extending beyond electrical methods, a wide range of optical thermometry techniques have been developed for measuring the temperature in GaN electronics including IR thermal imaging [12–15], Raman thermometry [16–19], and transient thermoreflectance imaging [20–23]. While these optical techniques offer better spatial

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resolution to capture the lateral temperature gradient, optical barriers such as a field plate can limit these techniques' capabilities to measure the temperature near the hotspot and require the use of nanoparticle sensors [24,25]. GRT also does not require any modification on the package level, whereas most optical techniques require removing the cap to access the device's active area. Additionally, optical techniques can be restricted by the wavelength used to measure the channel temperature. In the case of IR thermal imaging, the GaN layer is transparent to IR wavelengths thus leading to the underprediction of the channel temperature [26,27]. For thermoreflectance imaging, the implementation of a subband gap excitation source can significantly underestimate the GaN channel temperature [28].

Overall, GRT has shown the potential to estimate the channel temperature rise in HEMTs by monitoring the gate end-to-end resistance [29]. Using a 4-point set-up, the resistance of the gate metal has shown to be strongly linearly dependent with temperature [1]. Previous work using gate resistance thermometry (GRT) under DC biasing has been applied to single finger AlGaN/GaN-on-Si HEMTs [30] as well as GaAs pHEMTs [31,32]. It has been suggested that GRT tends to underpredict the junction temperature when a large temperature gradient exists across the channel [33]. Additionally, previous work has shown the effects of bias conditions and device geometry on the accuracy of estimating the channel peak temperature. Altering the drain bias can impact the electric field distribution and consequently change the area of localized Joule heating. Elongating the gate width may develop larger temperature gradient along the device [34,35].

This chapter reviews the different approaches and configurations possible to implement GRT under varying biasing conditions. The accuracy of GRT is thoroughly investigated, and the origin of the temperature rise it captures is clearly demonstrated. In addition to being able to conduct this technique without having to switch off the device, the technique also has the potential to transiently monitor the channel temperature [36], which could then be used to characterize the device's transient thermal dynamics. The versatility of being able to use GRT under DC and pulsed biasing enables the accurate thermal characterization of the device under both steady state and transient conditions. Particular focus is given on verifying the technique's accuracy technique via other experimental methods (Raman) and numerical simulations. Furthermore, the errors associated with performing these measurements under different modes of operation are quantified. The importance of extracting accurate transient thermal parameters is also highlighted in this chapter using transient GRT measurements in the time or frequency domain.

9.2 Steady-state analysis

When initially developed, the GRT method captured the steady-state temperature of the gate metal in transistors [1]. The measurement is based on four-point sensing where separate electrode pairs are used to accurately record the voltage and current (shown in Fig. 9.1A). One key distinction in the design layout of GRT devices is the addition of a metal line on the other end of the gate to make the gate a doubled

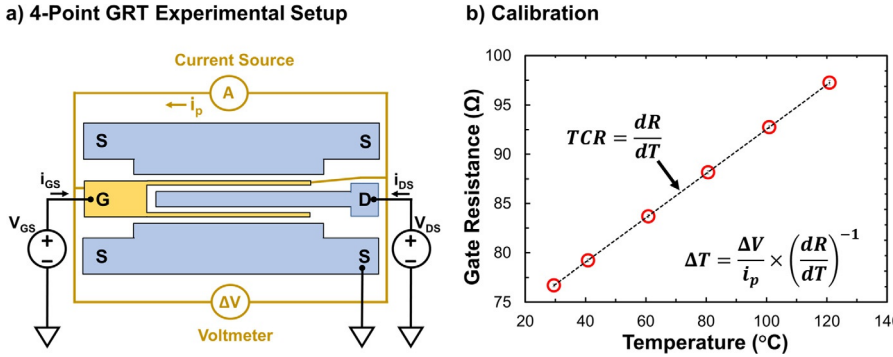

Fig. 9.1 (A) General experimental setup for conducting gate resistance thermometry (GRT) measurements. The setup utilizes four terminal sensing to measure the gate resistance over a single gate finger. The resistance is converted to temperature based on the temperature coefficient of resistance (TCR). (B) The TCR is extracted by linearly fitting the resistance vs. temperature data obtained via calibration with a temperature-controlled stage. The error bars represent the standard error of the gate resistance using 95% confidence intervals.

ended test structure. Under this configuration, the resistance can be measured in two configurations: current driven (supply a probe current and measure the voltage difference across the gate metal) or voltage driven (maintain constant voltage across the gate width while measuring the current). Most studies have used a passive oscilloscope to monitor the voltage drop across the gate; however, some studies have achieved higher sensitivity with an active differential probe [37]. Other studies have shown the implementation of depositing additional metal pads near the gate as temperature sensors [38–40].

Similar to previously developed electrical techniques, GRT is composed of two distinct stages: calibration and measurement. The calibration process (Fig. 9.1B) is typically completed with a temperature-controlled stage and is used to extract a temperature coefficient of resistance (TCR). The TCR can then be used during the measurement stage to convert the electrical measurement to a temperature value. The following section summarizes the efforts of both current and voltage configurations and discusses the potential uncertainties associated with the measurement.

9.2.1 Current driven

Under this configuration, a high precision current source is typically used to supply a probe current, i_p, across the gate metal. The voltage drop across the gate metal can then be measured at any time to extract the gate metal resistance. The magnitude of the probe current has shown to influence GRT's accuracy by potentially interfering with the gate leakage current due to impact ionization [31]. Impact ionization occurs when hot electrons collide with atoms in the channel to produce holes (positive charge to trap sites) [41]. This phenomenon is typically caused by a combination of a high gate-drain electric field and a high two-dimensional electron gas (2-DEG)

concentration. If the probe current, i_p, for the GRT measurement is injected in the same direction as the leakage current, the measured voltage drop across the gate (ΔV) will be overpredicted and thus result in falsely measured channel temperature. The probability of overlooking this effect is very high when measuring the gate temperature at varying power dissipations. Instead of attributing the sudden increase in temperature to the gate leakage (example shown in Fig. 9.2), the rise in channel temperature could be mistakenly attributed to a temperature-dependent thermal conductivity or significant localized heating. To minimize the error associated with impact ionization, the probe current can be increased (1–8.5 mA) to lower the percentage of the gate leakage current to the overall current.

The implementation of a high probe current, however, has also been shown to possibly alter the current distribution across the gate width [42]. Operating at a significant probe current will result in a large potential difference across the gate width. During operation, this additional voltage drop across the gate affects the electric field distribution across the channel by causing one end of the gate to be more negative than the other (Fig. 9.3A). The uneven current distribution will result in altering the path of heat dissipation. To confirm that a high probe current will alter the joule heating profile, an IR thermal imaging study was performed to monitor the temperature distribution across a GaN/SiC HEMT [42]. The study showed that the temperature profile is altered significantly when increasing the probe current. As depicted in Fig. 9.3B, the hot spot is shifted from the center signifying that the channel is more open on one end in comparison to the other end.

Alternatively, the effect of gate leakage current can also be minimized by the implementation of differential probes to monitor the gate end-to-end voltage drop. In contrast to passive probes, the active differential probe can amplify the detected signal and reduce the capacitive loading to achieve greater signal fidelity. To reduce

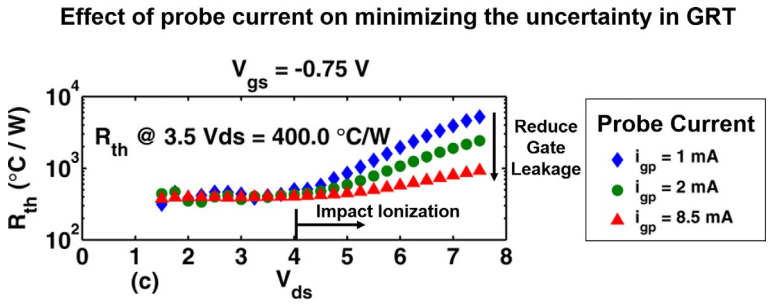

Fig. 9.2 Measured thermal resistance (R_{th}) plotted against drain bias, V_{ds}, for a given gate voltage, V_{gs}. Three different values of probe current, i_{gp}, are used. The results highlight a sharp rise in R_{th} beyond a critical value of V_{ds}. The effect becomes more pronounced for lower values of i_{gp} and coincides at the V_{ds} voltage where a significant increase in gate leakage current arises due to impact ionization.

Reproduced from B.K. Schwitter, A.E. Parker, A.P. Fattorini, S.J. Mahon, M.C. Heimlich, Study of gate junction temperature in GaAs pHEMTs using gate metal resistance thermometry, IEEE Trans. Electron Devices 60 (10) (2013) 3358–3364, https://doi.org/10.1109/TED.2013.2278704.

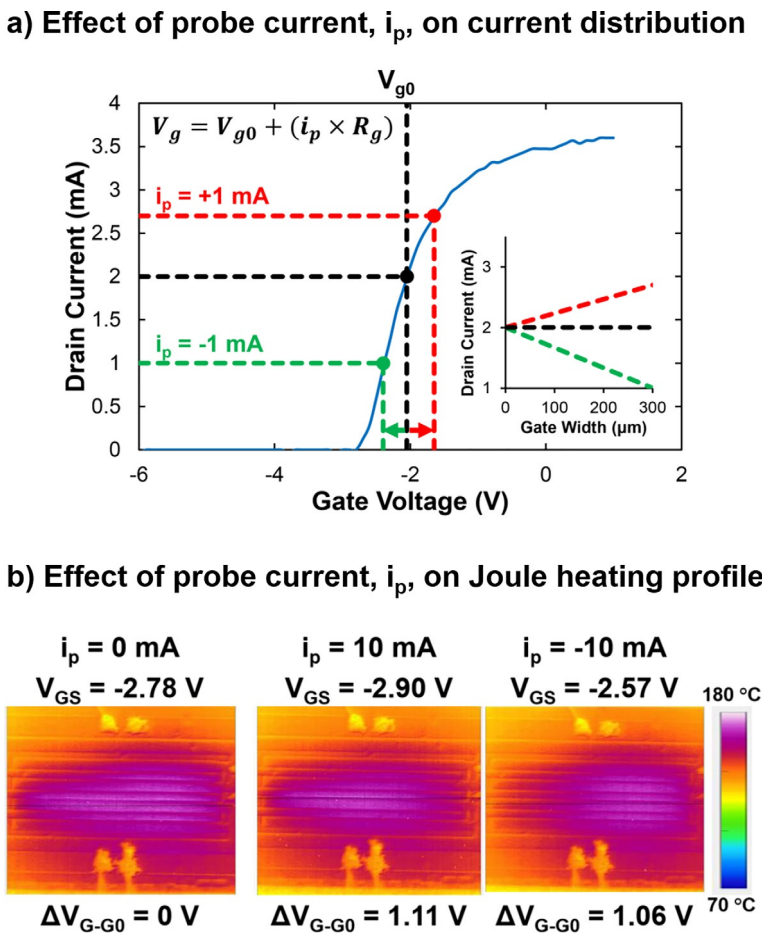

Fig. 9.3 (A) Effect of probe current's magnitude and direction on drain current, I_{ds}. Inset shows I_{ds} distribution along gate when probe current is applied. (B) Effect of probe current, i_p, on overall thermal distribution. $6 \times 1000\,\mu m$ GRT devices were biased at 0.8 W/mm. Reproduced from G. Pavlidis, Assessing the Performance and Reliability of GaN Based Electronics via Optical and Electrical Methods, Georgia Institute of Technology, 2018.

DC gate leakage effects, the differential probe can be reset to zero after applying the gate and drain bias under pinch-off conditions. This will set the potential difference reading to zero when minimal power is being dissipated. Since the gate leakage is found to vary with bias conditions [29], however, the differential probe must be recalibrated for every measurement to avoid any error (not doing so can lead to temperature errors of 5–7°C [42]).

To avoid constant recalibrations, alternating gate probe currents, i_{ac}, can be used. Previous studies have shown the feasibility of using an alternating current (AC) to measure the gate resistance in GaAs pHEMTs [43] as well as GaN HEMTs [37].

The method is based on the difference between voltages measured when a forward probe current is supplied and when a reverse current is supplied. This process enables GRT differential probe measurements to be conducted without the necessity of calibrating to a zero-probe current state. To ensure high accuracy, the forward and reverse current must have the exact same magnitude.

9.2.2 Voltage driven

An alternative approach to measuring the gate end-to-end resistance can be taken by supplying a constant probe voltage instead of a current. Using this method, the current is measured with high precision and can facilitate accounting for leakage current [9]. The leakage current is estimated by monitoring the current flowing in/out of each gate end. If the V_{ds} and V_{gs} biasing is significantly greater than the voltage across the gate (which will be controlled by the probe voltage), the HEMT is geometrically symmetric. Taking advantage of this symmetry, the leakage current can be assumed to be equally distributed to each gate end and thus easily calculated [29].

To calibrate under this procedure, the probe voltage is swept over a given voltage range and the resistance is extracted from the slope at different baseplate temperatures. To avoid any self-heating and disturbance of electric fields, the probe voltage is limited to tens of millivolts, as shown in Fig. 9.4. Once calibrated, the temperature measurements are conducted by supplying a fixed probe voltage across the gate end-to-end pads. Paine et al. [29] investigated the minimum probe voltage necessary to achieve

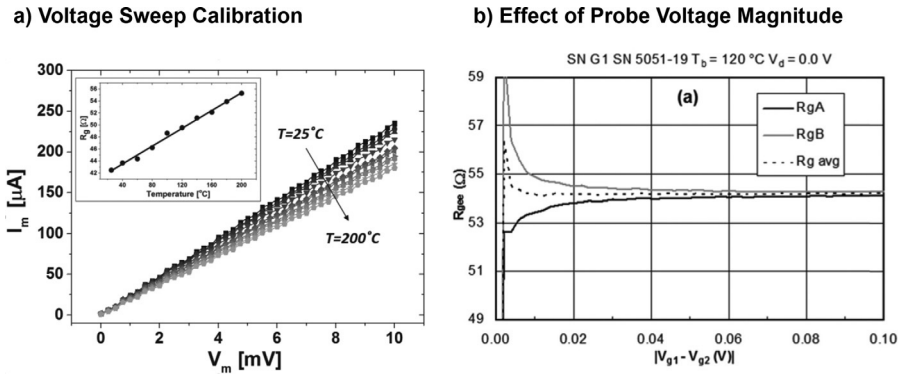

Fig. 9.4 (A) Temperature calibration of the resistive sensor (gate metal), where the slope of the V_m–I_m curve represents the resistance at each temperature. Inset: change of the sensor resistance with respect to temperature. (B) End-to-end gate resistance, R_{gee}, measured with the two current directions, and the average. Probe voltage is varied to determine minimum voltage necessary for convergence.
(A): Taken from V. Sodan et al., Experimental benchmarking of electrical methods and mu-Raman spectroscopy for channel temperature detection in AlGaN/GaN HEMTs, IEEE Trans. Electron Devices 63 (6) (2016) 2321–2327, https://doi.org/10.1109/Ted.2016.2550203; (B): Taken from B.M. Paine, T. Rust, E.A. Moore, T. Rust III, E.A. Moore, Measurement of temperature in GaN HEMTs by gate end-to-end resistance, IEEE Trans. Electron Devices 63 (2) (2016) 1–8, https://doi.org/10.1109/TED.2015.2510610.

convergence between resistances measured under different polarity (Fig. 9.4B). As previously discussed, when employing an alternating probe current, averaging the resistance values measured under the two different polarities can remove any error caused by voltage offsets.

9.2.3 Temperature coefficient of resistance

The accuracy of the temperature estimated by GRT is heavily dependent on extracting the correct TCR. Potential errors associated with estimating the TCR can be attributed to poor thermal contact with the temperature controlled base plate or drift in TCR. To ensure that the gate metal is uniformly heated with a constant temperature during calibration, sufficient time should be given to allow the device to reach steady state. This can be validated by monitoring the transient temperature of the gate metal for an extended time of heating. Furthermore, to improve thermal contact between the base plate and the device, a thermal interface material can be used in combination with applying a small contact force.

Drifts in TCR were reported by Paine et al. [29] to occur over just a few hours of biasing the devices. The change in the TCR value was proposed to be caused by microstructural changes in the gate metal including microcracks or seams in the gates. Other potential errors were predicted to be caused by change in electrical contact or trap occupation in nearby semiconductor or dielectrics. To avoid drift error, recalibration every few hours was necessary.

Changes in the TCR were also observed when comparing the TCR value of packaged devices to on wafer measurements (Fig. 9.5). One study performed an extensive

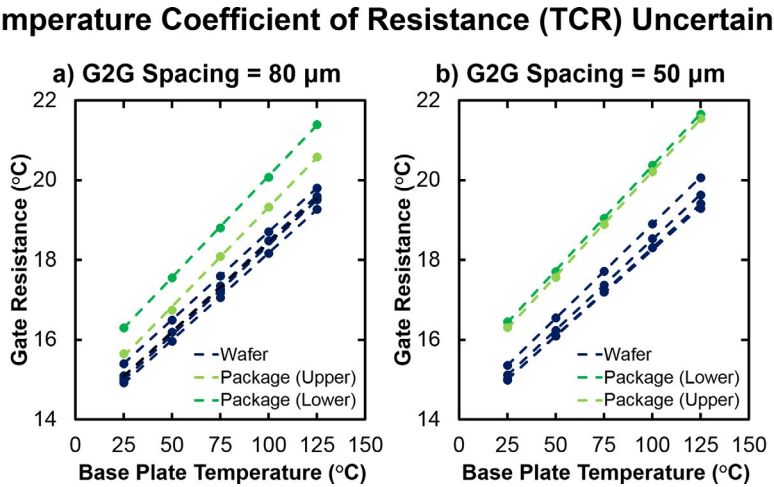

Fig. 9.5 Comparison of TCR extracted from GaN/Si HEMTs with different gate to gate (G2G) spacing. The gate resistance was measured both on packaged devices and devices on wafer. Taken from G. Pavlidis, S. Som, J. Barrett, W. Struble, S. Graham, The impact of temperature on GaN/Si HEMTs under RF operation using gate resistance thermometry, IEEE Trans. Electron Devices 66 (1) (2019) 330–336, https://doi.org/10.1109/TED.2018.2876207.

analysis of the TCR extracted for several devices on both wafer and packages [37]. Despite the TCR remaining the same value for devices on the same wafer, the results demonstrated that the TCR significantly changed (maximum 15% difference) when the devices were packaged. The TCR of packaged devices originating from the same wafer was even shown to differ in values. The potential cause of this discrepancy was initially attributed to the large thermal contact resistance between the package and the thermal stage, which causes a lower temperature to be achieved at the gate metal during calibration. This theory was dismissed, however, since the gate resistances of the packaged devices at room temperature already differed. The effect of the electrical contact resistance of probe was also dismissed as the error was estimated to be on the order of 1% of the total resistance and should also be corrected for when performing a four-point measurement. The study proposed that the change in the TCR was potentially due to the chemical alteration of the gate metal during packaging. More specifically, the solvent that was applied to remove the photoresist after dicing and substrate thinning may have chemically reacted with the gate metal and thus cause a change in the TCR. The change in TCR shows the importance of performing frequent calibrations to account for any experimental changes.

9.2.4 Determining thermal resistance

One key parameter that can be extracted via steady-state GRT analysis is the vertical stack thermal resistance. Validating whether the structure has a low thermal resistance is essential to ensure efficient thermal conduction from the hotspot to the substrate. Typically in units of °C/W, this parameter is defined as the ratio between the channel temperature rise (with reference to the base temperature) and the input power dissipated. Many material properties and physical phenomena can contribute to increasing the thermal resistance with increasing power density. This includes the temperature-dependent thermal conductivities of the thin film materials in GaN electronics as well as the thermal boundary resistance (TBR) between interfaces. While the average channel temperature provides a useful estimation of the device performance and thermal resistance, measuring the peak channel temperature rise enables a more accurate evaluation of the device's thermal characteristics and prediction of lifetime and reliability.

At high drain biases, the hot spot in GaN HEMTs tends to form near the gate making GRT the most suitable electrical technique to estimate the peak temperature. Comparative studies (such as the one shown in Fig. 9.6) have confirmed GRT's advantage of measuring a temperature closer to the peak channel temperature [9]. In this case study, the GRT temperatures agree well with the localized Raman temperature measurements, whereas other electrical techniques (spatially averaged across the channel) significantly underpredict the peak channel temperature. An additional study also showed that other electrical techniques underpredict the peak channel temperature confirmed by Raman [33].

The sensitivity of the GRT to detect small changes in thermal resistance has been demonstrated in a thermal study on GaN/Si HEMTs [37]. In this study, GRT is used to show the decrease in thermal resistance due to efficient thermal spreading when increasing the gate to gate spacing from 50 to 80 μm. While this trend was true for

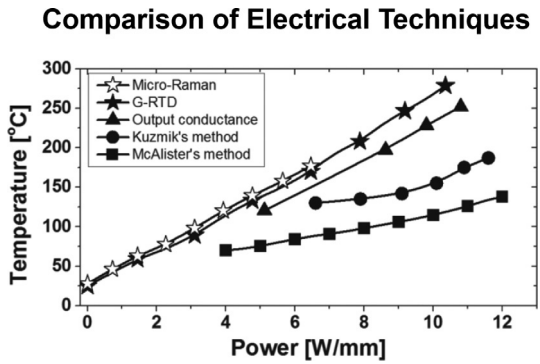

Fig. 9.6 Comparison of temperatures measured by steady state thermal characterization techniques to Gate Resistance Thermometry.
Taken from V. Sodan et al., Experimental benchmarking of electrical methods and mu-Raman spectroscopy for channel temperature detection in AlGaN/GaN HEMTs, IEEE Trans. Electron Devices 63 (6) (2016) 2321–2327, https://doi.org/10.1109/Ted.2016.2550203.

the devices measured on wafer, the packaged devices resulted in the opposite phenomena where the 80 μm gate-to-gate devices reached a higher temperature than the 50 μm gate-to-gate devices. After further examination of the packaging process, the thickness of the die attach was measured to be 40% greater for the 80-μm gate pitch device. The unexpected change in thermal resistance was thus attributed to the discrepancy in die-attach thickness. The results of this study exemplify GRT's accuracy and the ability to measure changes in the stack configuration that contribute to the thermal resistance.

The peak temperature, however, is not always located near the gate and can thus cause the GRT method to underestimate the thermal resistance in the device [44]. Furthermore, an additional cause of underestimating the peak temperature can be attributed to large temperature gradients formed along the gate width. One study showed that the temperature gradient (from center to edge) increases from 16°C to 30°C when elongating the gate width from 370 to 1000 μm [45]. This translated to a GRT measured temperature that is 11% lower than the Raman measured temperature at the center of the device.

9.3 Transient analysis

Despite steady-state methods enabling the accurate quantification of the device's thermal properties such as thermal resistance and power density dependence, transient analysis is needed to gain deeper insight into the dynamic performance of GaN based electronics. Devices such as HEMTs are normally biased under pulsed or RF operation, which causes large temperature swings on the time scale of micro to nanoseconds [46]. Furthermore, phenomena such as trapping become more significant during pulsed mode operation and have been shown to be heavily temperature dependent [47,48].

Capturing the transient temperature enables the detection of the peak temperature at the maximum power dissipation (which could potentially be an order of magnitude higher than the average temperature captured by a steady-state technique). The transient rise and decay profiles can be used to extract properties such as thermal time constants, which can be inputted into advanced finite element electrothermal models [49] for more accurate prediction of the device's lifetime and reliability [50]. Additionally, transient temperature measurements can assist in developing nonlinear device models for FET device optimization and layout design.

Besides using GRT, other electrical techniques have been developed to monitor the transient temperature in GaN HEMTs such as monitoring the change in drain current [36]. Decoupling the transient drain current from trapping effects, however, has proven difficult. Additionally, transient measurements have also been conducted via optical techniques such as Raman thermometry [51] and Transient Thermoreflectance Imaging [22,52]. To obtain nanometer spatial resolution, the transient temperature can also be inferred from measuring the expansion of the surface via scanning joule expansion microscopy (SJEM) [53]. Although these optical techniques offer greater spatial resolution than GRT, their temporal resolution can be limited. For example, the time resolution of a transient thermorelfectance image is defined by the minimum LED pulse width which could be on the order of 50 ns. Since GRT is an electrical technique near the heat source, it can achieve nanosecond resolution that would be more desirable when operating devices at higher frequencies. Overall, transient thermal characterization of GaN HEMTs has been performed both in the time domain and frequency domain. The following sections demonstrate the capability of performing transient gate resistance thermometry (tGRT) in both domains.

9.3.1 Time domain

For most tGRT measurements, the transistor is typically biased with a pulsed-IV instrument that is synchronized with an oscilloscope to monitor the voltage drop across the gate metal (see Fig. 9.7A). To minimize the effect of the gate bias on

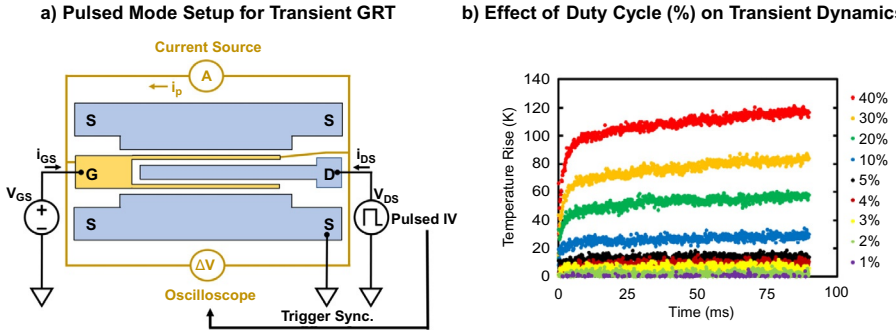

Fig. 9.7 (A) Experimental setup for transient GRT measurement using pulsed IV. (B) Transient device temperature response for varying duty cycle at a power density of 3 W/mm.
Taken from G. Pavlidis, Assessing the Performance and Reliability of GaN Based Electronics via Optical and Electrical Methods, Georgia Institute of Technology, 2018.

the GRT measurement, the gate voltage is often kept constant while the drain bias is pulsed at a given time period and duty cycle. Attempts to pulse the gate have resulted in perturbation of the GRT signal [42] due to the significant generation of gate leakage. Other modifications to the setup could include resistors, which can be inserted in series with the gate pad, to provide isolation for potential RF measurements [30].

Another advantage tGRT has over many optical-based transient measurements is the ability to perform in situ measurements. To capture a sufficient Raman peak or thermoreflectance signal at a short time interval, averaging the signal over multiple pulses at a given time delay is necessary. While averaging is also needed for GRT when measuring temperature changes on the order of nanoseconds, in-situ measurements have been reported successful at the microsecond [54] and millisecond level [42]. For example, the effect of the duty cycle on the transient gate temperature is shown in Fig. 9.7B. Results like these can be used to measure the device's "pseudo step" response and extract the multiple time constants associated with it [51].

To obtain higher temporal resolution under pulsed operation and capture the full temperature rise and decay, tGRT can be averaged over multiples pulses. For a given pulsed drain and gate bias, temperature rises on the order of hundreds of nanoseconds have been reported [52]. Additional studies have shown that an active differential probe can improve the temporal resolution to nanoseconds [55]. In order to capture the gate temperature rise and decay while averaging, the duty cycle should be kept below 30% to avoid accumulation of heat at the device level (as shown in Fig. 9.7B). Fig. 9.8A is an example of tGRT's capability to monitor the temperature rise and decay in GaN/SiC HEMTs.

For most techniques, the transient temperature rise is referenced to the base temperature when the drain bias is off. Despite attempting to minimize the accumulation

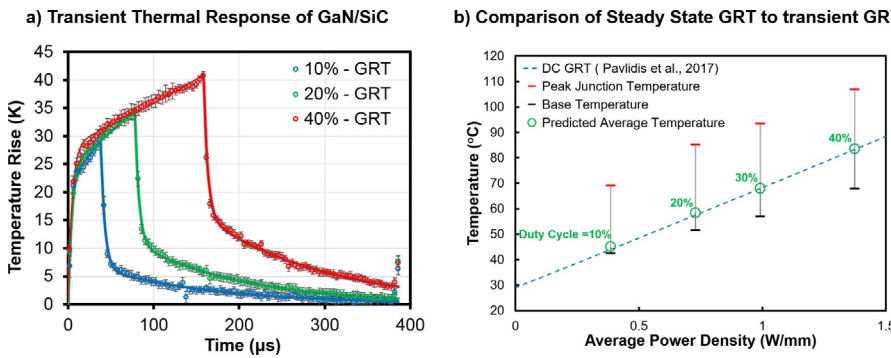

Fig. 9.8 (A) Transient thermal response of GaN HEMT under various duty cycles. The error bars represent the standard error of the GRT estimated temperatures using 95% confidence intervals. (B) Absolute base and peak temperature measured by GRT for varying duty cycle from 10% to 40% with a time period of 400 µs.
A: Taken from G. Pavlidis, Assessing the Performance and Reliability of GaN Based Electronics via Optical and Electrical Methods, Georgia Institute of Technology, 2018; B: Taken from G. Pavlidis, D. Kendig, E.R. Heller, S. Graham, Transient thermal characterization of AlGaN/GaN HEMTs under pulsed biasing, IEEE Trans. Electron Devices 65 (5) (2018) 1753–1758, https://doi.org/10.1109/TED.2018.2818621.

of heat by limiting the duty cycle, some heat will be conserved if several pulses are applied during averaging. Consequently, the device will reach a dynamic equilibrium after several pulses, but the reference base temperature will be higher than at the beginning of measurement due to heat accumulation. In order to quantify the increase in reference base temperature, the temperature must be measured prior to any biasing. Compared to other techniques, GRT can quickly and easily calculate this temperature rise by measuring the absolute resistance at the beginning of the measurement. One study converted the transient temperature rise to absolute temperature values to compare the temperatures to steady-state GRT under DC biasing (see Fig. 9.8B). Overall, great agreement is shown between the two techniques when directly comparing the average temperature of the gate metal over a pulse [52]. The significance of these results suggests that steady-state GRT could be used to estimate the peak temperature under pulsed biasing and approximate the maximum temperature.

9.3.2 Sensitivity

While the steady-state analysis potentially could estimate the peak temperature rise under pulsed biasing, unfortunately, the technique cannot extract the thermal time constants for characterizing the device's transient thermal dynamics. The advantages of tGRT over the steady method have also been reported to assist in investigating the effect of device geometry on thermal performance. Design and geometry variations of the device design include the effect of gate pitch or the number of gate fingers.

One research group demonstrated tGRT's capacity to monitor the temperature increase in GaN/Si HEMTs when decreasing the gate pitch from 80 to 50 μm [37]. While some of the longer pitch devices resulted in higher temperature under steady-state conditions due to variation in die attach thickness (discussed in Section 9.2.4), tGRT was insensitive to the device packaging effects. The cause of this phenomena was attributed to the thermal penetration depth that is dependent on the pulse biasing frequency. The results from this study suggest that the pulse biasing frequency can be adjusted to detect the thermal properties of different regions in the device stack layer configuration.

The effects of thermal coupling due to an increase in gate fingers were also reported through the tGRT analysis [56]. The transient temperature of a single gate device (100 μm gate width) was compared to the center gate temperature of an 8 finger device. To summarize, the gate temperature for both devices began to differ after 10 μs of heating. Using the tGRT results to validate advance electrothermal models, the models were accurately developed to model the effects of thermal coupling in multi finger devices. Prior to 10 μs, the heating of each channel is isolated in the *epi* layer and no differences were observed between a single and multifinger device. At longer time delays, the heat is dissipated out of the channel and the proximity of the neighboring channel thus has a significant effect on the gate temperature rise. In general, the results from this study highlighted the versatility of tGRT to differentiate the intrinsic thermal response from thermal coupling.

9.3.3 Frequency domain

An alternative approach to assessing the dynamic temperature in GaN electronics is monitoring the gate resistance in the frequency domain. Cutivet et al. reported the first GRT measurement in the frequency domain (fGRT) [57]. The experimental set-up (as shown in Fig. 9.9A) consists of supplying a probe current across the gate finger while applying a frequency-dependent drain bias. The drain bias can be applied using either a pulsed IV system (as previously discussed for tGRT) or a sinusoidal pulse via a function generator. The key component of fGRT is the lock-in amplifier which is used to measure the voltage drop across the gate and filter any other electrical noise. The addition of the lock-in amplifier (LIA) enables the user to improve the signal to noise ratio of the GRT measurement when applying a fixed frequency bias. To obtain the device's full thermal step response, the drain bias is swept at multiple frequencies typically ranging between 1 Hz and 100 kHz (more recent studies have reported a maximum frequency of 2 MHz [59,60]). The procedure can be compared to the 3-omega method with the key difference that the fGRT technique uses the gate metal as the sensor instead of the ON-resistance [61].

While using a LIA that is synchronized to the frequency of the drain bias has proven effective, fGRT can also be implemented by applying a small AC-voltage to the gate. This can be accomplished by coupling a small signal gate bias via a bias tee/DC-block and detecting the gate resistance with a LIA (shown in Fig. 9.9B). To validate the accuracy of this method, the novel configuration has been directly compared to steady-state GRT measurements (shown in Fig. 9.10A). Based on the good agreement between the two techniques, fGRT enabled a 100 × reduction in the probe current, which can significantly reduce any uncertainty associated with a gate bias gradient along the gate width. Furthermore, the fGRT set-up minimized the gate bias offset and fully isolated the lock-in equipment from the device bias connections. Beyond measuring the gate resistance of a single device, the ultrahigh sensitivity of fGRT

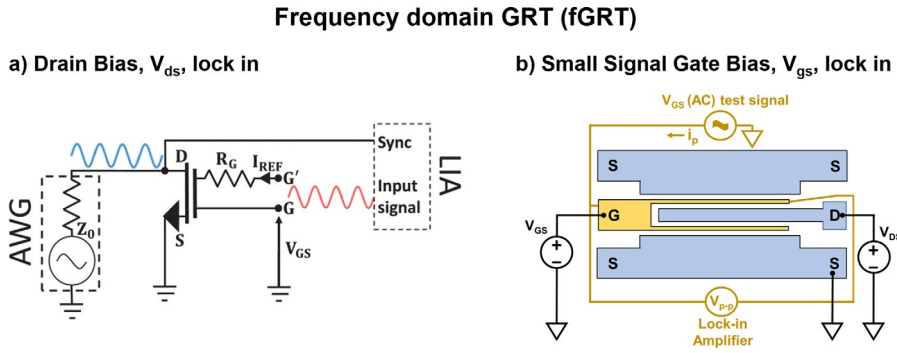

Fig. 9.9 (A) Experimental set-up of fGRT on GaN on Si HEMT using an arbitrary waveform generator (AWG) to control the power dissipation and a lock-in amplifier (LIA) to measure the gate-to-gate voltage variation, $\Delta V_{GG'}(f)$ [58]. (B) Alternative approach to fGRT using an arbitrary waveform generator to supply a small signal bias across the gate.

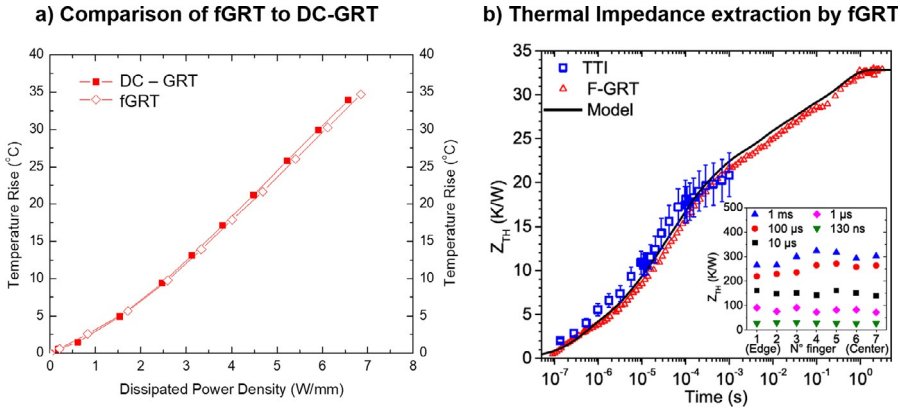

Fig. 9.10 (A) Comparison of temperature rises extracted in GaN HEMTs via the classical DC method and the novel gate-driven fGRT method. (B) Thermal impedance extracted by f-GRT and converted in the time domain to compare to transient thermoreflectance imaging (TTI). The errors bars represent the propagated uncertainty from the experimentally measured thermoreflectance coefficient with a ± 12% spatial standard deviation.
(B): Taken from A. Cutivet et al., Scalable modeling of transient self-heating of GaN high-electron-mobility transistors based on experimental measurements, IEEE Trans. Electron Devices 66 (5) (2019), 2139–2145, https://doi.org/10.1109/TED.2019.2906943.

enables the technique to be potentially used for investigating the thermal crosstalk between different devices on the same chip or sub mounts. Potential applications could include studying the thermal effect of interconnects in heterogenous systems [15,62].

The majority of fGRT experiments are conducted using a sinusoidal bias that contrasts with the step pulse biasing used in tGRT. Using a sinusoidal dissipated power can avoid many uncertainties associated with step pulses. For example, locking into a single frequency ensures an ideal dissipated power step with negligible rise time. The minimization of rise times translates to other benefits such as the prevention of ringing effects in large devices. Additionally, short rise times can minimize transient drain current reductions that are normally observed in step pulsed biasing (also known as power droop). In general, measuring electrical parameters in the frequency domain usually provides higher signal-to-noise ratio and thus requires less dissipated power amplitude. The drawback of fGRT, however, is its inability to conduct in situ transient measurements. Since the gate resistance values are measured at discrete frequencies, interpolation is required to fully build the transient curve captured by tGRT.

Another advantage of performing fGRT is the effective minimization of the gate-drain coupling effect previously observed in transient GRT measurements [58]. This effect is primarily a concern when measuring high frequencies and the coupling effect is significantly greater than the thermal contribution. For the 100 Hz to 100 kHz range, the coupling effect can be corrected by recording two measurements with probe currents of opposite polarity but same magnitude. For frequencies greater than 100 kHz,

the effect can be minimized by using an AC probe current, which was previously discussed in detail in Section 9.2.1. Furthermore, the effect of the gate bias on the gate leakage current is found to be less significant when measuring in the frequency domain.

Similarly to tGRT, one of the primary functions of transient characterization is the extraction of the device's thermal time constants that can verify the thermal impedance applied to advanced numerical models. A previous in-depth study showed that at least one time constant per decade is required to accurately model the device's transient thermal response [46]. Due to the presence of multiple thin films in GaN electronics, the range of time constants is very large and ranges from 1 ns to several milliseconds. This broad time range cannot usually be fully captured with one single technique and requires combining results from multiple experimental set-ups. Performing GRT in the frequency domain overcomes this barrier by having the capability to sweep over very broad frequency ranges. For example, the thermal impedance of a GaN on Si HEMTs extracted from fGRT is compared to TTI in Fig. 9.10B. This study shows that the TTI measurements are limited to 1 ms time constants, whereas the fGRT extends to time constants equating to single seconds. The ability to cover a large range of frequencies makes fGRT suitable to detect multiple thermal effects that occur at different time scales. This includes the localized self-heating near the gate, the thermal cross talk in multi fingered devices, and the efficiency of the heat sink.

9.4 Under RF operation

The ability to monitor the channel temperature under RF operation has proven difficult for several thermometry techniques [63] and can result in very high costs. For this reason, most reliability measurements, such as accelerated lifetime testing, are performed under DC biasing to predict the device's mean time to failure (MTTF). As previously mentioned, however, the Joule heating profile is complex and bias dependent. Operation under RF conditions could thus result in both different magnitude and position of the peak temperature in comparison to DC operation (one study predicts differences between the two modes of operation [50]). To fully develop GaN-based electronics into the high frequency microwave industry, an accurate thermometry technique is therefore required to estimate the junction temperature under RF operation. Acquiring this capability can provide deeper insight into the active degradation mechanisms under RF operation and whether they are similar to those under DC operation.

The feasibility of using GRT under RF operation has been reported only a few times in literature for GaN HEMTs [55,64]. The majority of these measurements involved time averaging the gate temperature when the HEMT is operated under continuous wave (CW) mode [37]. By doing so, the effect of device geometry and environmental factors (such as the gate pitch, power added efficiency (PAE), and baseplate temperature) on the RF thermal performance can be quantified. One study compared GaN/Si HEMTs under RF operation with two different gate pitches [37] (see Fig. 9.11). The baseplate temperature was also varied to study its effect on the thermal

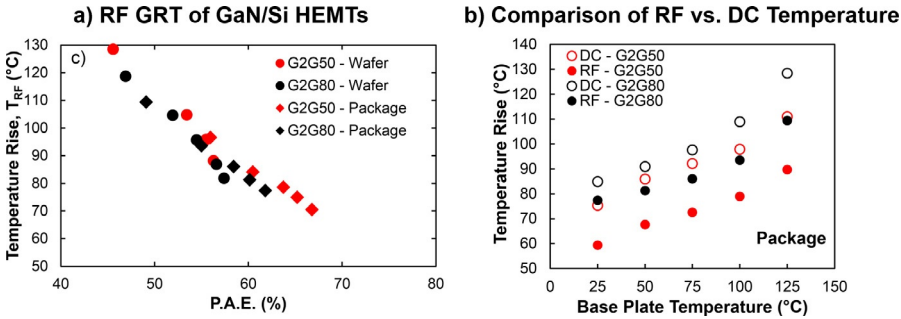

Fig. 9.11 (A) RF thermal performance of GaN/Si HEMTs at different PAEs for gate to gate (G2G) spacing of 50 and 80 μm. (B) Comparison of junction temperature measured under RF operation to DC steady-state biasing at different baseplate temperatures ranging from 25°C to 125°C.

Taken from G. Pavlidis, S. Som, J. Barrett, W. Struble, S. Graham, The impact of temperature on GaN/Si HEMTs under RF operation using gate resistance thermometry, IEEE Trans. Electron Devices 66 (1) (2019) 330–336, https://doi.org/10.1109/TED.2018.2876207.

performance. The results of these unique measurements confirmed that the elongating the gate pitch decreases the gate temperature under RF operation. Additionally, the PAE is observed to decrease linearly with an increase in the overall temperature measured by GRT (Fig. 9.11A). This quasi linear relationship is to be expected and consequently highlights the potential of using GRT under RF operation.

Having the ability to perform GRT measurements both under steady state and RF conditions now gives one the opportunity to directly compare the device's thermal performance under DC versus RF. The results of Fig. 9.11B demonstrate the direct comparison of the gate temperature under the two modes of operation. To accurately compare these two modes of operation, the average power dissipated must be correctly calculated. While the average power dissipated is easily calculated for the DC mode of operation, the RF average power was calculated by subtracting the net gain RF power from the DC dissipated power [23]. Overall, both modes of operation show a linear increase in temperature with power density. The RF temperature, however, appears to result in a lower gate temperature for all measurements. This decrease in temperature suggests there are indeed differences in the temperature profile of GaN HEMTs under RF operation in comparison to DC operation. In contrast, the Raman thermometry measurements under RF operation showed minimal differences in channel temperature between the two modes [23]. The discrepancy between the two measurements could potentially be attributed to the difference in magnitude of the drain bias between the two experiments. The Raman measurements were performed at a drain bias of 25 V, while the RF GRT measurements were recorded at a drain bias of 50 V. According to a numerical study [50], the difference between the two modes of operations becomes more significant with increasing drain bias. To summarize, RF GRT offers a fast-reliable solution to compare the thermal performance of GaN HEMTs under CW operation. The recent development of this technique will allow additional studies to be completed to gain better understanding of RF active degradation mechanisms.

9.5 Conclusions

Measuring the junction temperature has proven to be a key parameter for improving the performance and reliability of wide bandgap electronics. Several thermometry techniques have been developed over the years to provide a more accurate solution to this challenge. In comparison to other thermometry techniques, GRT has been demonstrated to provide a low-cost reliable method to estimate the device temperature. Since the hot spot is typically formed near the gate, GRT is often able to directly measure the hottest temperature in the device. This capability is necessary to understand the degradation mechanisms in GaN HEMTs and provide guidance on how to reduce the thermal resistance in these devices. Upon review, GRT offers robust solutions to both steady and transient methods that unlock the characterization of a wide range of parameters including thermal resistance and time constants. While this technique has been extensively developed to accurately measure the device temperature during operation, GRT could be further developed to be used as a sensor for detecting additional properties relevant to the device's performance. Based on the recent development of the technique being used in the frequency domain, this could include using the gate simultaneously as a heater/sensor to estimate the thermal conductivity of individual thin film layers or thermal interface resistances.

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