Mobility Extraction in 2D Transition Metal Dichalcogenide Devices – Avoiding Contact Resistance Implicated Overestimation

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Abstract: Schottky barrier (SB) transistors operate distinctly different from conventional metal-oxide semiconductor field-effect transistors (MOSFETs), in a unique way that the gate impacts the carrier injection from the metal source/drain contacts into the channel region. While it has been long recognized that this can have severe implications for device characteristics in the subthreshold region, impacts of contact gating of SB in the on-state of the devices, which affects evaluation of intrinsic channel properties, have yet comprehensively studied. Due to the fact that contact resistance (R_C) is always gate-dependent in a typical back-gated device structure, the traditional approach of deriving field-effect mobility from the maximum transconductance (g_m) is in principle not correct and can even overestimate the mobility. In addition, an exhibition of two different threshold voltages for the channel and the contact region leads to another layer of complexity in determining the true carrier concentration calculated from $Q = C_{OX} * (V_G - V_{TH})$. Through a detailed experimental analysis, the effect of different effective oxide thicknesses, distinct SB heights, and doping-induced reductions in the SB width are carefully evaluated to gain a better understanding of their impact on important device metrics.

1. Introduction

Two-dimensional (2D) transition metal dichalcogenides (TMDs) have received considerable attention as promising candidates for beyond silicon based devices. Owing to their atomically-thin layer structures and excellent transport properties, TMDs target a wide range of applications including post-CMOS logic,[1–3] memory,[4–6] flexible electronics,[7,8] and hardware-relevant artificial intelligence development.[9–11] The carrier mobility (μ) is a central parameter in characterizing electron and hole transport in a material. High mobility values enable particular promise for high-performance devices, especially for FETs. The most widespread method for mobility extraction uses the peak transconductance ($g_{m,max}$) value to extract the highest field-effect mobility (μ_{FE}) from an FET with a source, a drain and a gate contact (which we will refer to as "2-terminal FET" in the following) in the linear V_{DS} region employing:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L} \times \mu_{FE} \times C_{ox} \times V_{DS} \quad (1)$$

where I_D is the drain current, V_{GS} is an applied gate voltage, W/L is device's channel width/length, C_{OX} is the gate capacitance, and V_{DS} is an applied drain voltage. This approach is valid for Si FETs, since the highly doped source/drain (S/D) regions in conjunction with metal silicides create low resistive ohmic contacts and the silicides are not under gate control.[12,13] However, the story is more complicated for most TMD-based FETs, where a gate-dependent contact resistance (R_C) arises in a back-gated (BG) device geometry due to a modulation in Schottky-barrier (SB) width at the source/drain metal-to-channel interface. In addition, a pronounced Fermi-level pinning at the metal-TMD interface constitutes a main hurdle for realizing a low-resistive contact in the S/D regions.[14–17] Therefore, the common belief is that any contact resistance R_C can only impede the carrier transport and hence always results in an underestimation of μ_{FE} extracted from $g_{m,max}$.

However, it is not a definite case. C. Liu et al.[18] investigated the gate-dependent R_C from simulation which leads to an overestimation of mobility values (although noted that the concave-like R_C vs V_{GS} behavior given in their simulation is not a typical observation from experimental results due to a screening effect of gate fields). J. R. Nasr et al.[19] revealed the mobility overestimation by intentionally creating different channel threshold voltages (V_{TH}) in a dual-gate structure. H.-Y. Chang et al.[20] proposed the Y-function method to remove the R_C effect when evaluating the mobility values. Although the gate-dependent R_C is pointed out in above studies, a comprehensively analysis including the impact of effective oxide thickness (EOT) of the gate dielectric, different TMD channel materials, and the involvement of extrinsic doping schemes are yet carried out especially from experiments. These are all essential factors that will affect the threshold voltage identification and the interplay between R_C and channel resistance (R_{CH}), which eventually impact the evaluation of device metrics. It is especially important for devices with a large SBH, for instance WSe_2 where a feature of ambipolar characteristics are typically observe due to the Fermi-level pinning closer to the middle of the bandgap,[21,22] or for the monolayer TMDs where a larger bandgap is expected which attributed to a pronounced quantum confinement.[23]

In this article, we will first discuss why a careful extraction of the correct, i.e., intrinsic mobility μ_{int}, explicitly mandates the use of a 4-terminal FET geometry for certain TMD FETs, e.g., WSe_2 devices with thick gate dielectrics. We will explain how μ_{FE} as defined above can be *larger* than actual μ_{int} for those types of devices, revealing a rather surprising finding that this artefact is a result of the contact gating. In this context, it is critical to evaluate the 2-terminal and 4-terminal threshold voltage ($V_{TH\_2\text{-}terminal}$ and $V_{TH\_4\text{-}terminal}$), which can be vastly different for certain TMD materials and gate dielectrics. In particular, we will also show how μ_{int} depends on the gate voltage, which affects the carrier concentration in the channel. Note that for conventional CMOS devices, an increase in carrier concentration deep in the device on-state typically implies a reduction in mobility,[24,25] which is NOT observed in any of our TMD

devices. Next, we will discuss why 2-terminal FET measurements on MoS_2 and WS_2 (irrespective of gate oxide thickness) as well as on WSe_2 with thin gate dielectrics are adequate to extract intrinsic mobilities with a moderate error. Lastly, we will discuss how SiN_x doping in case of WSe_2 devices with a thick gate dielectric also allows recovering intrinsic device properties.

2. Result and Discussion

2.1. Precisely Designed 4-terminal Device Geometry

A critical finding of our research is that 2-terminal and 4-terminal FET devices as defined above can behave vastly different. In order to create our 4-terminal devices, in addition to the conventional source/drain (V_S/V_D) contacts, two additional voltage leads (V_1 and V_2) as shown in **Figure 1**(a) and (b) were defined. Figure 1(a) shows a schematic of the 4-terminal FET and Figure 1(b) displays a scanning electron microscope (SEM) image, where L_G and W are the channel length and channel width, respectively. We avoid any etching process to create a Hall-bar structure which could potentially lead to a significant amount of residue on the channel surface, impacting the intrinsic properties of a TMD.[26] Instead, we ensured lithographically that the overlap region between the voltage leads and the channel is as small as possible to avoid current shunting induced inaccuracies.[27] In addition, for an accurate extraction of R_C and μ_{int}, the width of the voltage leads (W_{probe}) needs to be sufficiently narrow in order to precisely probe the potential profile at *one* location in the channel and to identify the distance (dL) between the two voltage leads with a minimal uncertainty. A similar 4-terminal geometry to evaluate device properties had been employed by references,[28,29] and more details on the fabrication process are discussed in the Experimental Section.

2.2. Revealing Intrinsic Device Metrics

2.2.1 Contact Resistance (R_C)-implicated g_m Overestimation and V_{TH} Disparity

As the first example, emphasizing the importance of employing a 4-terminal geometry for the correct extraction of intrinsic mobilities, we have characterized WSe_2 back-gated devices fabricated on a 90 nm SiO_2 on Si substrate – a device configuration commonly used due to fabrication simplicity. The 4-terminal measurement (see red curve in **Figure 2**(a)) gives direct access to the normalized channel resistance in the units of Ω·μm: $\boldsymbol{R_{CH} = \frac{V_1 - V_2}{I_{DS}} \cdot \frac{W \cdot L_G}{dL}}$. Contact resistance is then calculated from (R_{Total} – R_{CH}) / 2, given R_{Total} (the 2-terminal resistance) and R_{CH} being measured experimentally. Figure 2(a) presents the dependence of these three resistance values on the back-gate voltage V_{BG}. Not only does this plot reveal that there is a regime (for small V_{BG}) where R_{Total} is dominated by R_C, but also shows a stronger dependence of R_C than R_{CH} on V_{BG}, which is the key reason for an overestimation of mobility if $g_{m,max}$ is extracted from 2-terminal measurements. This point becomes more apparent from Figure 2(b) that displays I_{DS}-V_{BG} curves. The "2-terminal" black curve reveals the change of current impacted by the back-gate dependences of R_C and R_{CH}, while the "4-terminal" red curve presents the channel response after elimination of the contact resistance contribution through our 4-terminal measurements, i.e., current being calculated by dividing V_{DS} of 1V by R_{CH} from Figure 2(a). As expected, the current level in the 4-terminal configuration is higher at the same V_{BG} than that from the 2-terminal measurement, since the contact resistance contribution has been eliminated. Figure 2(b) also reveals a steeper slope of the 2-terminal measurement if compared to the 4-terminal one, which in turn gives rise to a larger $\boldsymbol{g_m = \frac{dI_{DS}}{dV_{BG}}|_{V_{DS}}}$ and, therefore, produces higher mobility value than the correct one associated with the slope of the 4-terminal curve. The discrepancy stems from the presence of the gate dependent R_C that is part of the 2-terminal measurement. Since R_C changes more rapidly with V_{BG} close to the 2-terminal threshold ($V_{TH\_2\text{-}terminal}$), it dominates the g_m-extraction, giving rise to an overestimation of mobility. A more detailed analysis concerning the convoluted g_m-value in a 2-terminal geometry is provided in the Section SI (Supporting Information).

Another interesting aspect, which is apparent from Figure 2(b) is the difference between the $V_{TH\_2\text{-}terminal}$ and $V_{TH\_4\text{-}terminal}$ values. There exists a substantial gate voltage range where the current in the 2-terminal measurement is suppressed due to R_C domination as discussed in the context of Figure 2(a). This discrepancy between $V_{TH\_2\text{-}terminal}$ and $V_{TH\_4\text{-}terminal}$ is significant since the actual amount of charges at a given back gate voltage in the device on-state is indeed $\boldsymbol{Q = C_{ox} \cdot \left(V_{BG} - V_{TH\_4-terminal}\right)}$ and thus a smaller Q-value would be extracted using the larger $V_{TH\_2\text{-}terminal}$. An underestimated Q in turn results in an overestimated μ values. Thus, using the classical 2-terminal current equation of a MOSFET in its on-state and g_m extracted from a 2-terminal measurement will both result in systematic errors in the mobility extraction. Instead, the correct current expression using the 4-terminal configuration should be applied as follows:

$$I_D = \frac{W}{dL} \times \mu_{int} \times C_{ox} \times (V_{BG} - V_{TH\_4\text{-}terminal}) \times V_{DS,V1\text{-}V2} \quad (2)$$

where dL is the distance between two voltage leads and $V_{DS,V1\text{-}V2}$ is the voltage drop across them. Figure 2(c) compares the extracted 2-terminal and 4-terminal g_m-values and Figure 2(d) displays extracted mobility values as a function of overdrive voltage, according to different extraction methods. In particular, Figure 2(d) compares the correct μ_{int} with extracted μ-values of the same device, employing g_m from 2-terminal measurements (black filled squares) following the approach from.[30–33] Note that different from silicon devices, there is barely any dependence of μ_{int} on overdrive voltage. This result is expected, considering that the position of the electron wave function in the channel above threshold is almost entirely defined by the geometry, i.e. the ultra-thin TMD body, and the gate voltage has little or no impact on that position. Open black squares are a result of a method suggested by that combines g_m-values extracted from 2-terminal measurements with an adjustment of channel voltage drop through their 4-terminal measurement.[34–38] Note that the latter results in an even larger error and

inaccurate gate voltage dependent trend, which is discussed in greater detail in the Section SII (Supporting Information).

Figure 2(e) illustrates the impact of the metal contact on the carrier distribution in WSe_2, which is the cause for the different V_{TH}-values. Due to Fermi level pinning at the metal contact, there is a depletion of electrons near the contact region. As a result, when the channel region has reached threshold at $V_{BG}=V_{TH\_4\text{-terminal}}$. , the contact region is still below threshold. A larger $V_{BG}=V_{TH\_2\text{-terminal}}$ is required to reach V_{TH} in the contact region and enable the electron injection, as shown in the band diagrams. Whether the correct V_{TH} has been used when analyzing device data, namely the $V_{TH\_4\text{-terminal}}$, can also be examined by plotting $\log(R_{CH})$ vs. $\log(V_{OV})$ as shown in Figure 2(f), where V_{OV} stands for an overdrive voltage. A slope of "-1" is expected if the charge Q in the channel follows the expected $\boldsymbol{C_{ox}\cdot(V_{BG}-V_{TH})}$-dependence, which is according to our findings always the case when V_{TH} = $V_{TH\_4\text{-terminal}}$ is used in the charge expression. On the other hand, if the incorrect $V_{TH\_2\text{-terminal}}$ is employed for materials with a large SB height, a "wrong" slope smaller than "-1" will be observed as shown for the black curve. The above statement is particularly important if using transmission line measurements (TLM) instead of a 4-terminal geometry for devices with large SB height (SBH), where the measurement *cannot* distinguish between the two different V_{TH}. As shown in Figure S1 (Supporting Information) where TLM extracted R_{CH} of $MoSe_2$-FETs is displayed for various channel thickness (T_{CH}), slopes smaller than "-1" for *all* devices in the $\log(R_{CH})$ vs. $\log(V_{OV})$ plot are observed. This is a clear evidence of the fact that WSe_2 and $MoSe_2$ fall into the same category of high SBH devices and extra care needs to be taken when analyzing their mobilities.

To summarize the above findings: Implementation of a 4-terminal geometry is essential to accurately extract channel mobilities for SB-devices that include a strong gate-dependence of R_C. As we will discuss in the following, large SB heights and thick gate dielectrics as present in WSe_2 devices discussed above make the extraction of mobility from 2-terminal measurements particularly challenging.

2.2.2 Implementation on Thin Gate Dielectric – In Alleviating g_m Overestimation

To further explore the impact of device geometry on mobility extraction, WSe_2 FETs were implemented on thin gate dielectrics. More details about the process flow are discussed in the Experimental Section. Transfer and output characteristics for a representative device are shown in Figure S2 (Supporting Information), where steep subthreshold swings (SS) of ~75 mV/dec and current saturation in the output characteristics are clearly observed. **Figure 3**(a) and (b) display representative resistance and current curves similar to Figure 2(a) and (b). Interestingly, different from Figure 2(a), R_C is below R_{CH} for these devices irrespective of the gate voltage. Moreover, the slopes of the two curves in Figure 3(b) are rather similar, implying that similar g_m values can be extracted from the 2-terminal and 4-terminal measurements, as shown in Figure S3 (Supporting Information). In particular, this suggests that the mobility extraction in the thin dielectric case is much less sensitive to the measurement method. This experimental observation is the result of a reduced SB width (λ) at the metal-to-channel interface, which is typically expressed as $\boldsymbol{\lambda = \sqrt{(\varepsilon_{ch}/\varepsilon_{ox})T_{ch}T_{ox}}}$,[39] where T_{ch} is the channel thickness, T_{ox} is the oxide thickness, ε_{ch} and ε_{ox} are the dielectric constants of channel and oxide, respectively. SB devices with small λ exhibit similar $V_{TH\_2\text{-}terminal}$ and $V_{TH\_4\text{-}terminal}$, as illustrated by the example in Figure 3(b). In other words, all the effects that we discussed in the context of WSe_2 devices on thick gate dielectrics:

1) There exists a gate voltage range where R_C dominates over R_{CH}

2) The slope of I_{DS} vs. V_{BG} curve is substantially smaller in the 4-terminal compared to the 2-terminal case

3) There is a substantial difference between $V_{TH\_2\text{-}terminal}$ and $V_{TH\_4\text{-}terminal}$

are no longer (or merely) present for the same channel material on a thin back gate dielectric. The substantially reduced λ for the same SB height eliminates the impact of R_C and makes the

difference between the 2-terminal and 4-terminal measurement much less apparent. Therefore, the peak μ_{FE} extracted from a 2-terminal g_m is now similar to the correctly extracted μ_{int} value. However, using the combined 2- and 4-terminal measurement method can still overestimate the mobility substantially,[34–38] as shown in Figure S3 (Supporting Information).

2.2.3 Channel Materials with Smaller Schottky-barrier Heights

Up to now, we have focused our attention on WSe_2 FETs that exhibit a rather large SBH for electron injection. From the above discussion about R_C, one can expect that reducing the SBH should result in a similar device behavior as shown in Figure 3(b), since both the SB height and width impact R_C. Compared to WSe_2, both MoS_2 and WS_2 exhibit a smaller SBH for electron injection,[40–42] corroborated by the lack of a hole branch, as shown in Figure S4 (Supporting Information). Indeed, MoS_2 and WS_2 FETs with thick back gate dielectrics do not show the same discrepancy between 2- and 4-terminal measurements (see Figure 3(c) and (d)). Similar to our discussion about WSe_2 devices on thin gate dielectrics, mobility extraction is thus much less impacted by R_C and overestimation of mobility extracted from 2-terminal g_m is not a concern in both MoS_2 and WS_2 devices, as shown in Figure S5 (Supporting Information).

2.2.4 Overall μ_{int} vs Gate Fields for Four TMDs

Figure 4(a) summarizes our data on representative SB FETs from different TMDs, including data on $MoSe_2$ devices that behave similarly to WSe_2. As clearly evident, the mobility values are rather insensitive to the actual gate field, which is different from silicon as we already discussed above.[43] Statistical mobility values include 10 WSe_2 devices (black) with T_{CH} ranging from 2.8 nm to 7 nm, 8 MoS_2 devices (red) with T_{CH} ranging from 2.1 nm to 9.1 nm, and 10 WS_2 devices (blue) with T_{CH} ranging from 4.2 nm to 7 nm are shown as histogram in Figure 4(b). 5 $MoSe_2$ devices with T_{CH} ranging from 2.4 nm to 25 nm show a large mobility variation since TLM analysis is adopted but not 4-terminal method. Note that due to the

limitation of the TLM analysis not being able to distinguish the two different V_{TH}, the mobility data displayed in Figure 4(a) for $MoSe_2$ have been back-calculated using the knowledge about the expected slope of "-1" for R_{CH} as discussed above and in the context of Figure S1. The actual mobility value needs to thus be taken with a grain of salt, since it includes a much larger error bar correspondingly if compared with the values for the other materials. Considering the aforementioned, μ_{int} for WS_2 in terms of electron transport is in average the highest, which is in general consistent with what has been previously reported.[44] Finally, we do not observe a discernible channel thickness-dependence of μ_{int} at room temperature, which is believed to be dominated by phonon scattering.[45–47] We also want to point out that our reported μ_{int} is a lower bound of the actual mobility due to trapped charges and surface optical phonon scattering as compared to μ_{int} measured from devices fabricated on a smooth dielectric surface such as hexagonal boron nitride (hBN).[44,47,48]

2.2.5 Extrinsic Doping Scheme – In Alleviating g_m Overestimation

While we have focused on modulation of carrier concentration by the gate field, we will next explore the impact of devices being passivated by SiNx layer that induces additional electrostatic doping to the channel which is expected to also impact λ. The expectation is that a higher doping will ultimately result in a smaller λ and a reduced R_C will again lead to more similar device characteristics between 2- and 4-terminal measurements, even in the case of materials such as WSe_2 and $MoSe_2$ that exhibit large SBH. In our doping experiment, an apparent large negative shift of V_{TH} was observed from the transfer characteristics shown in the inset of **Figure 5**(a) after a SiNx film was deposited on the same device as shown in Figure 2, indicating that substantial n-doping has been achieved similar to previous reports.[49,50] R_C with respect to overdrive voltage for the device before and after the SiNx n-doping are compared in Figure 5(a), showing a clear R_C reduction across the entire overdrive range. As expected, much smaller differences between 2- and 4-terminal V_{TH} are observed in devices after SiNx doping,

as apparent from the example shown in Figure 5(b). Figure 5(c) summarizes the difference between 2-terminal and 4-terminal V_{TH} for eight devices. It is clearly evident that the V_{TH} difference is greatly reduced after doping. Hence, reducing R_C and thus enhancing electron injection at the source is the key, irrespective of whether this is accomplished by a reduction of SB height or SB width. Last, it is worth noticing that changing R_{CH}, for example by scaling L_G, would have the same effect as increasing R_C, since it is the interplay between R_{CH} and R_C, which ultimately matters for the correct mobility extraction.

3. Conclusion

A comprehensive study on the mobility of four different TMD channel materials, i.e. MoS_2, WS_2, $MoSe_2$, and WSe_2 has been presented. Particular attention has been paid to the importance of performing 4-terminal device measurements if contact resistances are large compared to the channel resistance. Interestingly, the mobility values extracted from 2-terminal g_m-measurements may suffer from potential overestimation, especially for devices with a large SB height associated with Fermi-level pinning. An obvious disparity of 2- and 4-terminal V_{TH} is observed in these devices. This phenomenon is attributed to a large R_C if compared with R_{CH} and can be partially mitigated in devices with a thin gate dielectric or intentionally doped FET channel. Our work also revealed that μ_{int} is rather insensitive to the gate field.

4. Experimental Section

Crystal growth: $MoSe_2$ crystals were grown by the Chemical Vapor Transport (CVT) method. A vacuum-sealed quartz ampoule containing polycrystalline $MoSe_2$ and $SeBr_4$ transport agent was placed in a horizontal tube furnace with a temperature gradient: the $MoSe_2$ charge was held at 980 °C and the growth section of the ampoule at ≈ 890 °C. After 7 d of growth, the ampoule was slowly cooled by turning off the furnace power.

$MoSe_2$ FETs fabrication on thick gate dielectric: $MoSe_2$ flakes were transferred onto 285 nm SiO_2/Si substrates using the gold-assisted exfoliation method.[51] Rectangular 5 μm × 70 μm $MoSe_2$ channels were photo-lithographically patterned and reactively-ion-etched. Ti(15 nm)/Au(150 nm) contacts were e-beam deposited in a transmission-line-measurement (TLM) configuration with 2 μm, 4 μm, 8 μm and 12 μm gaps. The FET data reported here were performed on devices with 2 μm channel length. All electrical measurements were conducted using a parameter analyzer Agilent B1500A under ambient conditions.

MoS_2, WS_2, and WSe_2 4-terminal devices on thick gate dielectric: Multi-layer MoS_2, WS_2, and WSe_2 were exfoliated from a bulk crystal (commercially available synthetic crystal purchased from HQ graphene) onto a 90 nm SiO_2 capped p^{++} doped Si substrate as a global back-gating scheme. E-beam lithography was employed to define source/drain (S/D) contacts and two additional voltage probes followed by e-beam evaporation of Ni (30 nm, at pressure ≈ $1 \cdot 10^{-7}$ Torr) as electrodes and a PMMA lift-off process.

WSe_2 4-terminal device on thin gate dielectric: E-beam lithography was used to define local bottom gate electrodes, followed by e-beam evaporation of Ti/Au (0.5 nm/10 nm, at pressure ≈ $1 \cdot 10^{-6}$ Torr) as the back-gate metal and a PMMA lift-off process. To implement a thin gate dielectric, e-beam evaporated Al (1 nm) was deposited as a seeding layer, followed by atomic layer deposition (ALD) of 28 cycles of HfO_2 at 200 °C. The remainder of the fabrication process is identical to what was described in the first paragraph of the experimental section. Multi-layer WSe_2 were exfoliated from a bulk crystal (commercially available synthetic crystal purchased from HQ graphene) onto a the substrate with local bottom gates. E-beam lithography was employed to define source/drain (S/D) contacts and two additional voltage probes followed by e-beam evaporation of Ni (30 nm, at pressure ≈ $1 \cdot 10^{-7}$ Torr) as electrodes and a PMMA lift-off process.

SiNx n-doping process: SiNx was deposited by plasma-enhance physical vapor deposition at 150 ºC with a flow rate of NH_3/SiH_4 = 100 sccm/30 sccm, under 50 W plasma power and 600 mTorr chamber pressure for 6 min.

Characterization: The electrical measurements were performed using an HP 4156B precision semiconductor parameter analyzer in conjunction with a Lake Shore probe station under vacuum at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

ZC and JA conceive and managed the research project. SK and AD managed the research project. CSP, RZ, XL, TH, SG, and MZ designed experiments, fabricated samples, and carried out electrical measurements. PW performed simulations. All authors discussed the results and wrote the manuscript. CSP, RZ, XL, PW, TH, JA, ZC acknowledge financial support from Semiconductor Research Corporation (SRC) program sponsored by NIST through award number 70NANB17H041. SK, AD acknowledge financial support from Material Genome Initiative funding allocated to NIST.

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Conflict of Interest

The authors declare no conflict of interest

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

Keywords

doping, mobility overestimations, Schottky barrier devices, thin gate dielectrics, transition metal dichalcogenides

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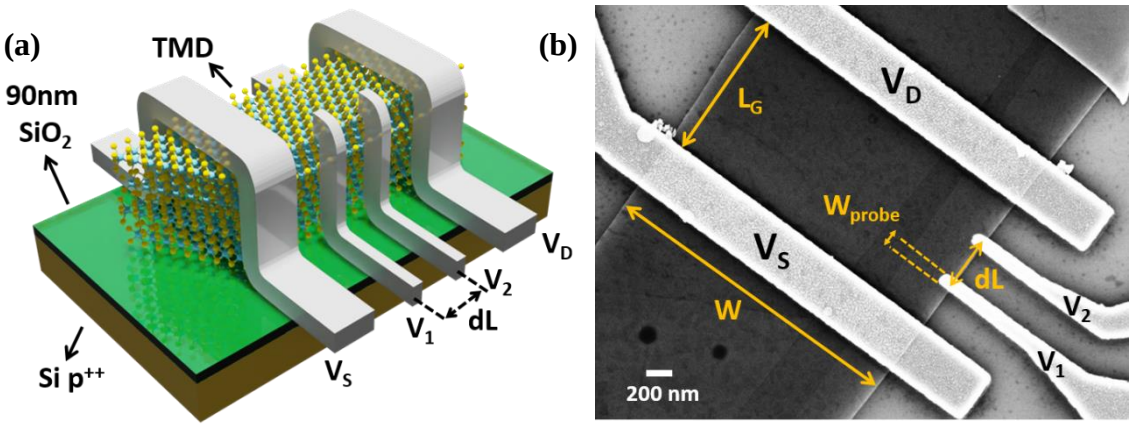
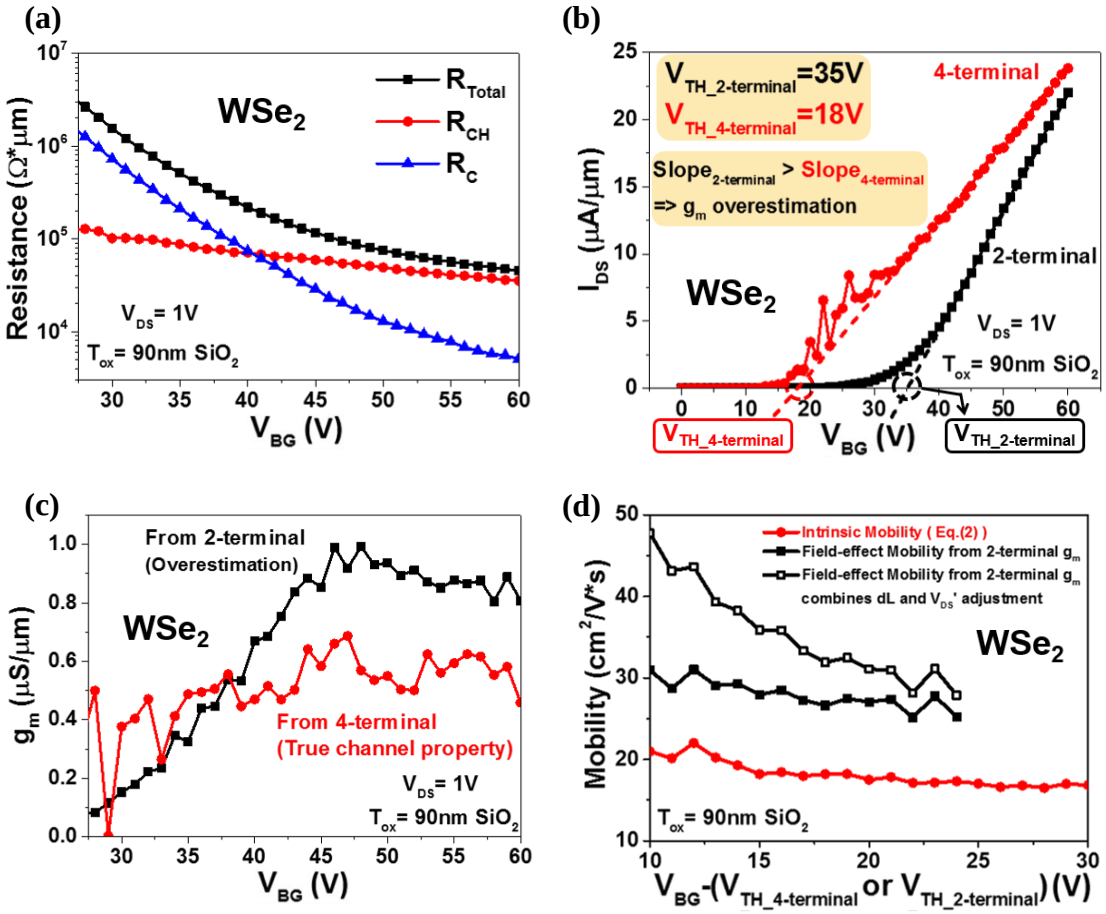


Figure 1. (a) A schematic illustration and (b) scanning electron microscope (SEM) image of a 4-terminal device structure, where L_G is the channel length, dL is the distance between two voltage probes V_1 and V_2, and W_{probe} is the width of each voltage probe. When only V_S and V_D electrodes are used together with the gate electrode in the measurement, it is referred to as 2-terminal measurement.



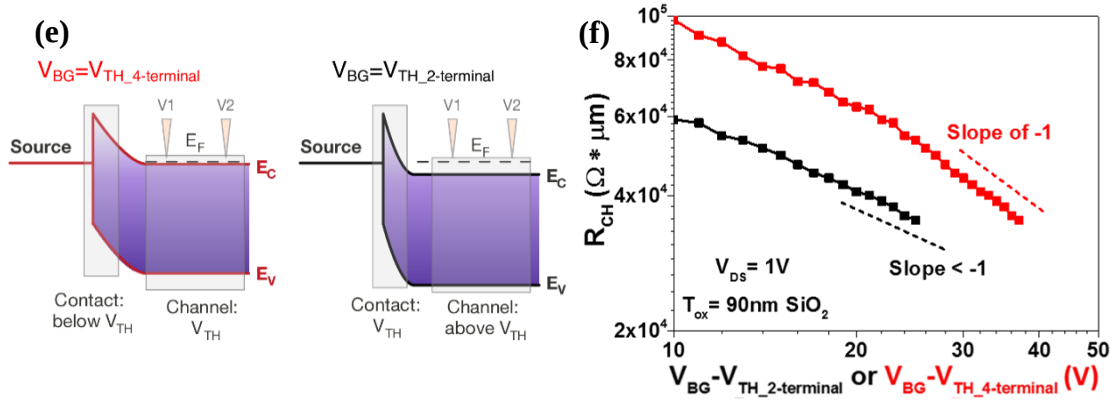


Figure 2. (a) 4-terminal (channel) and 2-terminal (total) as well as contact resistance as a function of back-gate voltage. (b) Comparison of 2- and 4-terminal I_{DS}-V_{BG} measurements on the same WSe_2 FET, where distinct differences in slope and threshold voltage of the I_{DS}-V_{BG} curves are observed. (c) Comparison of 2-terminal and 4-terminal transconductance extracted from Figure 2(b). (d) Comparison of the channel mobility values as a function of overdrive voltage for different extraction methods. (e) Band diagrams of the WSe_2 FET at the two threshold voltages. (f) Log(R_{CH}) vs log(V_{OV}) with different V_{TH} being used, where V_{OV} stands for an overdrive voltage.

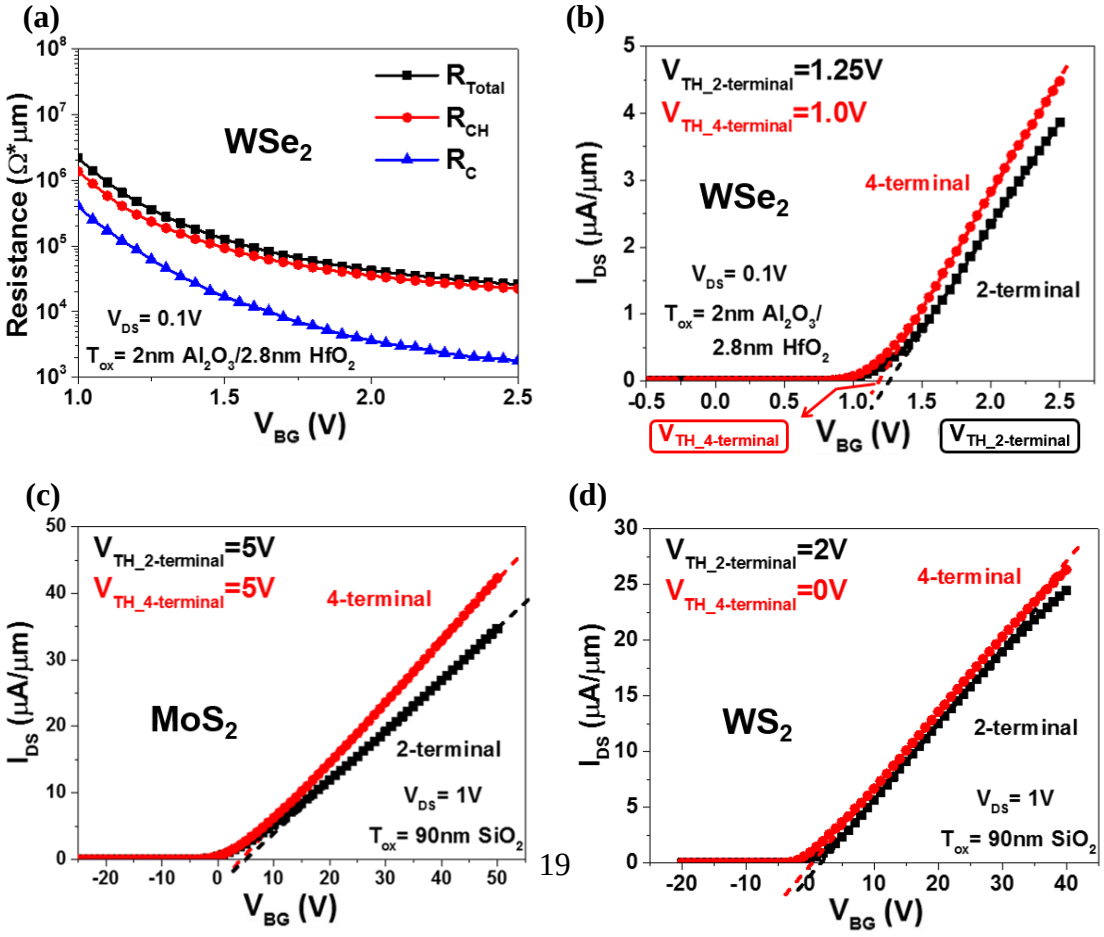


Figure 3. (a) Resistance values modulated by back-gated scheme on thin gate dielectric. **(b)** Comparison of 2- and 4-terminal linear I_{DS}-V_{BG} for a WSe_2 FET implemented on a thin gate dielectric. Note that the slopes of the I_{DS}-V_{BG} curves and V_{TH} extraction are similar (different from Figure 2(b)). Comparison of 2- and 4-terminal linear I_{DS}-V_{BG} for a **(c)** MoS_2 and **(d)** WS_2 FET implemented on a 90 nm SiO_2 gate dielectric.

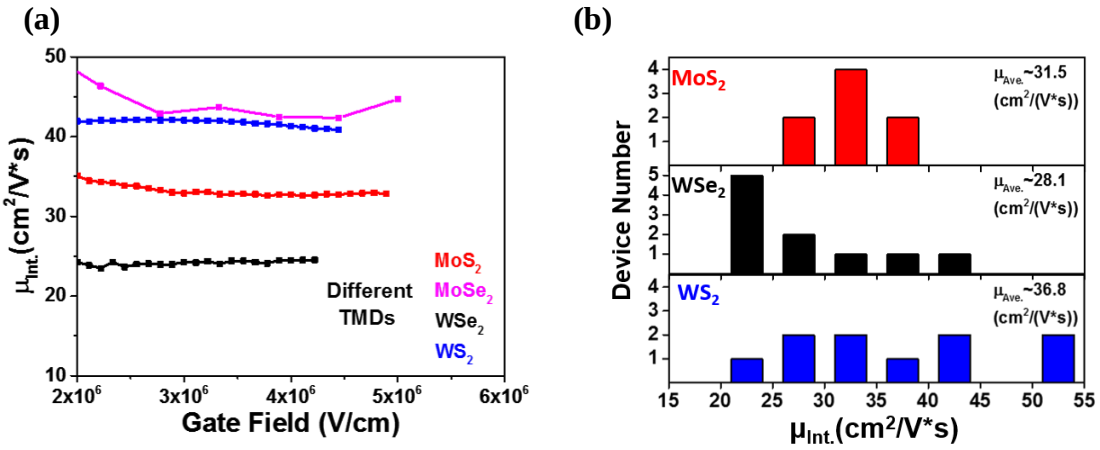
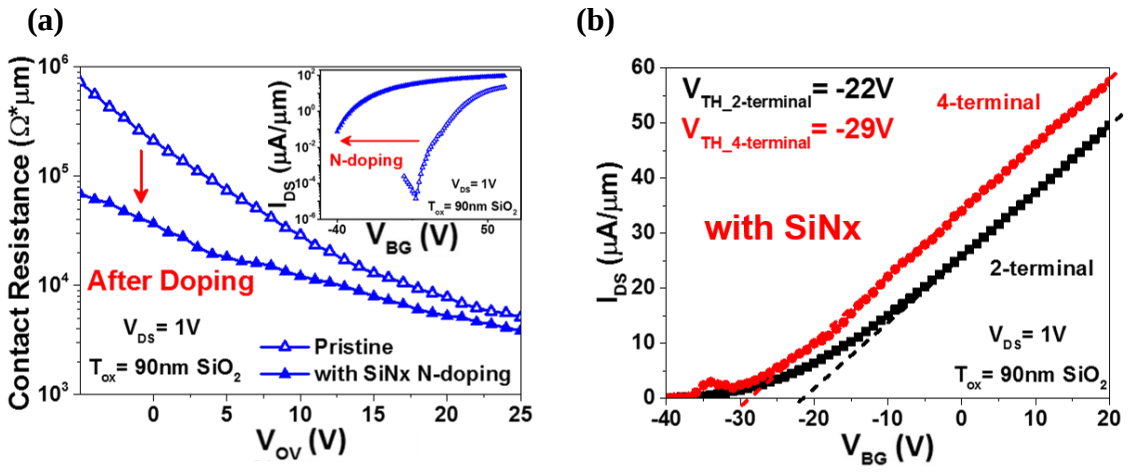


Figure 4. (a) Comparison of μ_{int} vs. gate field for representative SB FETs from four different TMDs. (b) Histogram of mobilities extracted from 4-terminal measurements for MoS_2, WSe_2, and WS_2 devices.



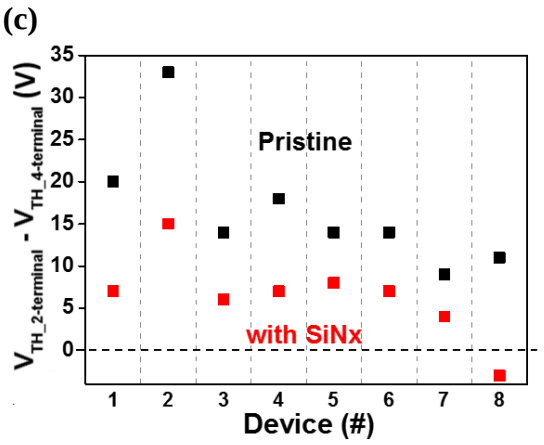


Figure 5. (a) Comparison of R_C as a function of overdrive voltage for a pristine device and the same device after n-doping. (b) Comparison of 2- and 4-terminal linear I_{DS}-V_{BG} curves after SiNx n-doping treatment. (c) The disparity between 2- and 4-terminal V_{TH} for eight different devices before and after SiNx doping.