Evaluating Solder Joint Failures and Solder Joint Reliability: A Side-by-Side Comparison of Direct Current and Microwave Based Monitoring Techniques

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Abstract
Historically, evaluations of solder joint failures and solder joint reliability have been done with direct current (DC) methods, using event detectors or data loggers for high-frequency circuits. Direct high-radio frequency (RF) measurements of signal paths are potentially more sensitive to incipient circuit (or solder joint) failure due to mechanical changes which may affect return loss, insertion loss, or phase angle, well before complete solder joint failure. Here are compared the fault detection capabilities and detection speeds, of direct current resistance (R_{DC}) to RF-based fault detection measurements to determine if RF signal loss could be a useful criterion for failure detection. In this paper, both high speed digital and analog RF circuits are considered.

Early S-parameter changes were observed, over time and thermal cycles, as the connectors were broken in from wear. Ultimately, the test circuits failed, due to cracks within the solder joints. The capacitance, and the capacitive reactance, of a partial crack in a solder joint was found to be substantially larger than the direct current resistance (R_{DC}) due to even a tiny remaining amount of intact solder joint. The low resistance so dominates the circuit that the circuit changes are unmeasurable

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by RF techniques until the crack is fully open. Thus, while the failures in high-frequency circuits from solder joint cracking are expected to occur simultaneously, or even after the DC failures occur, they are undetectable until total decohesion within the solder joint. As a result, the detection of failures using RF monitoring (S-parameters) lags that of failure detection by DC resistance measurement when evaluated by cycles to failure.

The results presented in this paper should be of benefit to component manufacturers working to determine the reliability of their components on test boards, their original equipment manufacturer (OEM) customers concerned about the components and their attachment to actual product circuit boards, and EMS and test labs providing services to component suppliers and OEMs.

Introduction

Many transmission lines on a high-speed server or network board have signal loss budgets of 10dB or less. A 1- or 2- dB loss on a solder joint could result in signal integrity failures. This is comparable to the loss typical in a well-designed FCBGA package. Traditional reliability measures such as DC-resistance (R_{DC}) may not adequately capture signal loss due to solder joint failures. Thus, new approaches to metrology need to be investigated. Kwon et al have demonstrated the application of microwave measurements in detecting incipient pre-catastrophic solder joint failure fractures in actual solder joints (as opposed to internal component electrical connectivity)[1-5]. High-frequency RF measurements of signal paths are potentially more sensitive to incipient circuit (or solder joint) failure[1-10]. Elsewhere, is researchers have correlation of DC-resistance due to device and material failures with changes in the microwave propagation characteristics[8].

Low-frequency measurements are done by direct current resistance (R_{DC}) measurements most often using event detectors or resistance data loggers. Low frequency resistance (R_{DC}) measurements are insensitive to incipient failures in emerging interconnects because of the large volume via fill in features such as through substrate vias (TSVs). Illustratively, void formation in TSVs was difficult to measure with electrical resistance change, while the onset of void formation results in impedance changes that are easily measured with the insertion losses of broadband microwave spectrum[9-10]. Furthermore, the phase changes in the propagating microwave can yield additional mechanistic information, such as changes in dielectric properties of the materials of construction, if they occur[6]. Prior to this test, it was anticipated that failures in RF circuits may occur because of mechanical changes that affect return loss, insertion loss or phase angle, well before complete solder joint failure.

RF testing may be done by monitoring scattering parameters (S-parameters) with a vector network analyzer (VNA) or high-speed time domain reflectometry (TDR) measurements. A TDR can measure the impedance changes and detect impedance discontinuities in the time domain, similar to what S-Parameters capture in the frequency domain[2-3]. These methods can measure travel time between source and defect site, attenuation constant (a measure of the total microwave energy loss from the dielectric and skin effect losses), RF signal phase, and group delay changes related to the changes in the dielectric properties of the device under test. Table 1 lists some of the relationships between common electrical measurements and the S-parameters commonly obtained in RF measurements[12]. These electrical quantities can be further transformed to provide more mechanistically relevant metrics. These can include Insertion Loss (S21) or Return Loss (S12).

Figure 1 illustrates some of the many chemical and mechanical changes that can result in changes in the microwave propagation characteristics in prototypical I/O circuits from previous published work[8]. Conceptually, the pre-catastrophic failure may result in a change in impedance of the device under test (DUT). Thus, the impedance can be used as a monitor of the solder joint reliability. The impact of an incipient mechanical crack will be discussed in detail below on a microwave bridge circuit.

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Table 1 Relationship between S-parameters from microwave measurements and some common electrical parameters

$$R = \mathrm{Real}\left(Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right)$$

$$L = \frac{\mathrm{Imag}}{\omega}\left(Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right)$$

$$G = \mathrm{Real}\left(\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{21}}{Z_0((1+S_{11})(1+S_{22}) - S_{12}S_{21})} \right)$$

$$C = \frac{\mathrm{Imag}}{\omega}\left(\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{21}}{Z_0((1+S_{11})(1+S_{22}) - S_{12}S_{21})} \right)$$

This paper directly compares the fault detection capabilities and detection speeds, of R_{DC} to RF, and determines if RF measurement of signal loss at different frequencies is a useful criterion for failure. Here, the attempt was made to use these microwave-based techniques on a customized PCB to study solder joint reliability, and to compare DC measurements to RF measurements. In this work, solder joints were stressed using accelerated thermal cycling, and changes in the microwave propagation characteristics of the circuits (usually represented as S-parameters) were measured. The changes in the S-parameters were leveraged to study the thermo-mechanical reliability associated with the thermal cycling of the purposely designed printed circuit boards.

The benefits were expected to be, but not limited to:

- Statistically determine the differences between DC and RF performance of solder joints
- Perhaps change our definition of "failed" solder joint
- Potentially explain many No Failure Found (NFF) field returns.

Materials

Printed Circuit Board (PCB) Design

Figure 2 shows the conceptual routing of the RF traces on the PCB design developed for this project. The figure shows the RF net (only), with a through-hole SMA connector routing through internal traces. The PCB boards were connected to a VNA with 40 GHz-rated semi-rigid RF cables through connectors rated for 27 GHz. Practical Components part number WLP256-.5-8MM-DC-SAC305. WSCSP dies were used as device components. All circuit packs consisting of the boards and the two components per board were built with SAC305, Indium 8.9HF1.

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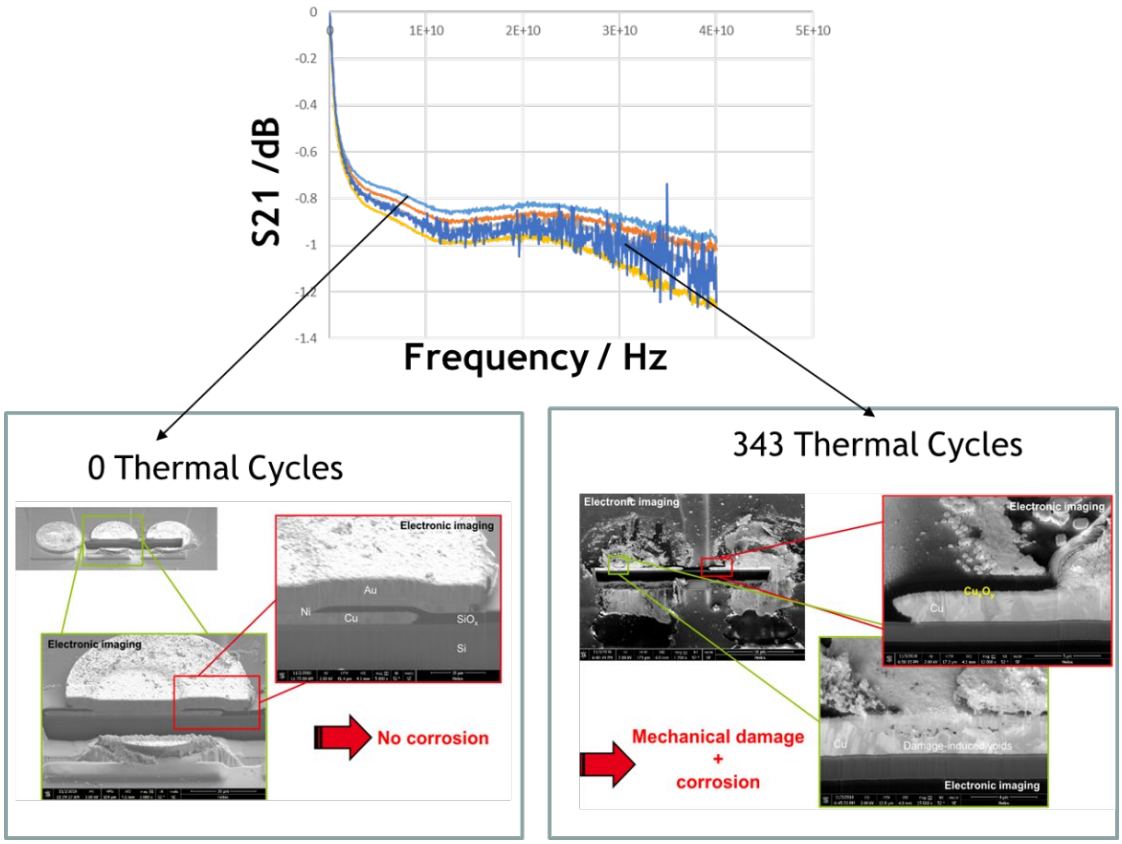

Figure 1: Illustration of the impact of thermal cycling on S-parameters of copper interconnects in open air due to corrosion (taken from Reference 5)

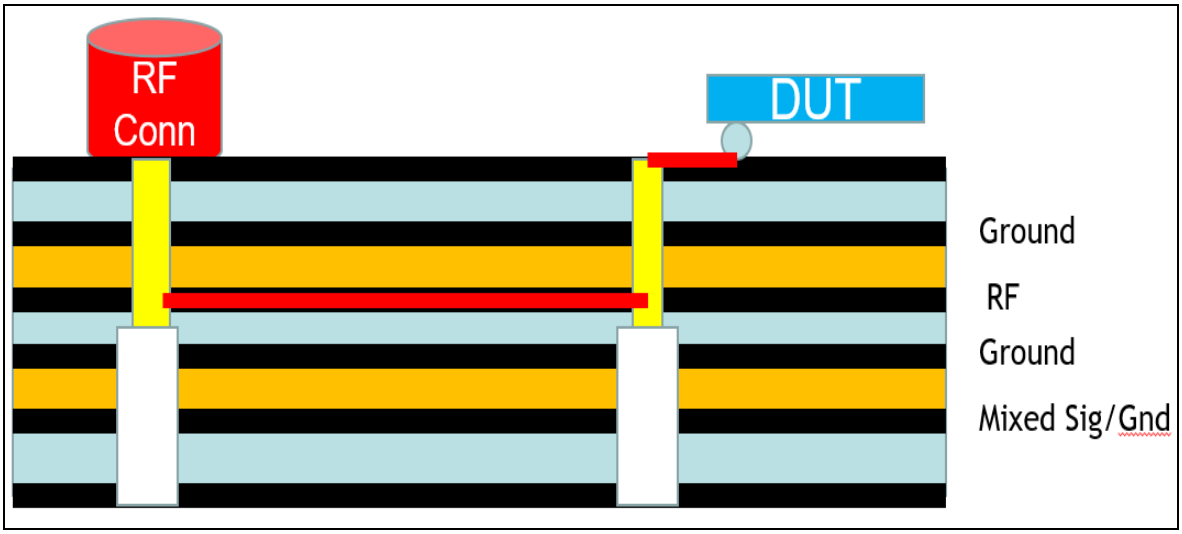

Figure 2: Conceptual routing of the RF traces

The top layer artwork design and the actual front and back of the completed PCB are shown in **Figure 2** while **Figure 3** shows the detailed PCB stack-up including trace width details. **Figure 4** shows the outer top surface of the test boards to illustrate the placement of the various test devices. The test board had the following features:

- Size: 16.5 cm X 17.8 cm, and 0.24 cm thick (i.e., 6.5" x 7"x 4, 93 mil thick)
- A single laminate material: Panasonic Megtron 7N (R5675N core, R5680N prepreg) with a board stackup as shown in Figure 3 was used.

- Immersion silver finish
- There are 2 identical components per board. One wired for DC resistance measurements, and one for S-Parameter measurements.
- For the 4 DC corner circuits, wires were soldered to the appropriate PTHs.
- For the 4 RF corner circuits Molex SMA Jacks, FLANGE with 0-80 THD, 50 OHM 27 GHZ EWR-3690 SMA-J/R/F connectors were attached to the boards.

Customer Req Thk: 93+/-9.3 mils Measured:Solder mask on plated copper

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.10	.5 oz			Foil .5 oz reduce to .25oz + Plating
			3.17	4.05	Prepreg M7N R5680N 3313
2	0.60	0.5 oz			
			3.20	29.50	Core M7N R5785N 29.50mils 6x2116 0.5 oz / 0.5 oz HVLP
3	0.60	0.5 oz			
			3.18	18.00	Prepreg M7N R5680N 2116/3313/3313/2116
4	0.60	0.5 oz			
			3.20	29.50	Core M7N R5785N 29.50mils 6x2116 0.5 oz / 0.5 oz HVLP
5	0.60	0.5 oz			
			3.17	4.00	Prepreg M7N R5680N 3313
6	2.10	.5 oz			Foil .5 oz reduce to .25oz + Plating

Layer	Drill Type	Via Fill		
1 - 6	PTH	Yes	87.45	Thickness over Laminate
			91.65	Thickness over Copper
			93.05	Thickness over Soldermask

Impedance Table

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Edge Coupled Pitch * (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)	CoPlaner Space (mils)
1	Single Ended	Yes	50.00	+/-5	<=8		(2)	7.50	50.02	
3	Single Ended	---	50.00	+/-5	20-40		(4, 2)	25.50	50.04	

Figure 3: Detailed PCB stackup including trace width details

Test Method

The daisy-chained components and the test circuit boards enabled electrical continuity testing after surface mount assembly and in situ, continuous monitoring during thermal cycling by DC measurements for one component and by RF measurement for the other component on each board. Thermal cycling was done in accordance with the IPC-9701A guidelines. The solder joints were monitored by DC means using the following criteria: a data logger set at a resistance limit of 3 ± 0.2 Ω. The RF measurements were obtained with a Keysight vector network analyzer (VNA). The switching system for the RF measurements is shown in **Figure 5**. The failure data are reported as characteristic lifetime eta η (the number of cycles to achieve 63.2% failure) and slope β from a two-parameter (2-P) Weibull analysis.

The temperature cycling profiles used in this investigation was 0 to 100°C testing with 915 cycles completed. This profile was selected to address the requirement of a specific industry or market segment as defined in standard IPC-9701A, specifically, telecom, represented by technical committee 1 (TC1). The temperature ramp rate was nominally 10 ºC/minute.

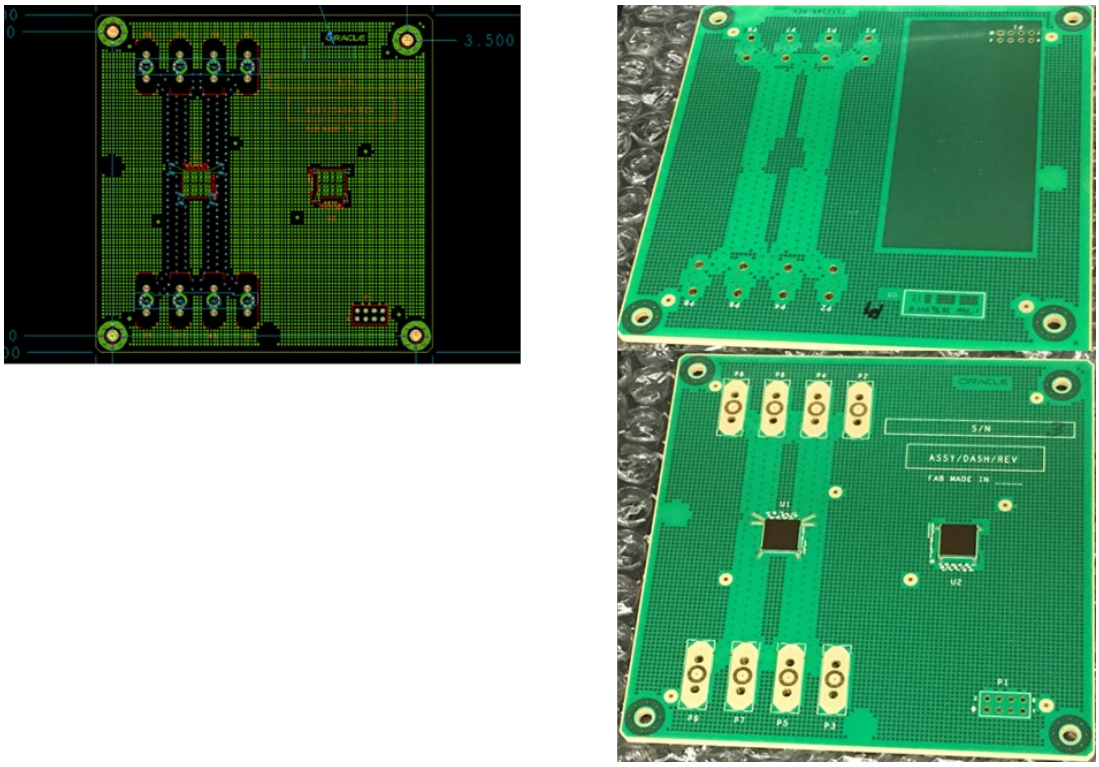

Figure 4: Outer Top Surface of the RF Failure Detection Test Board

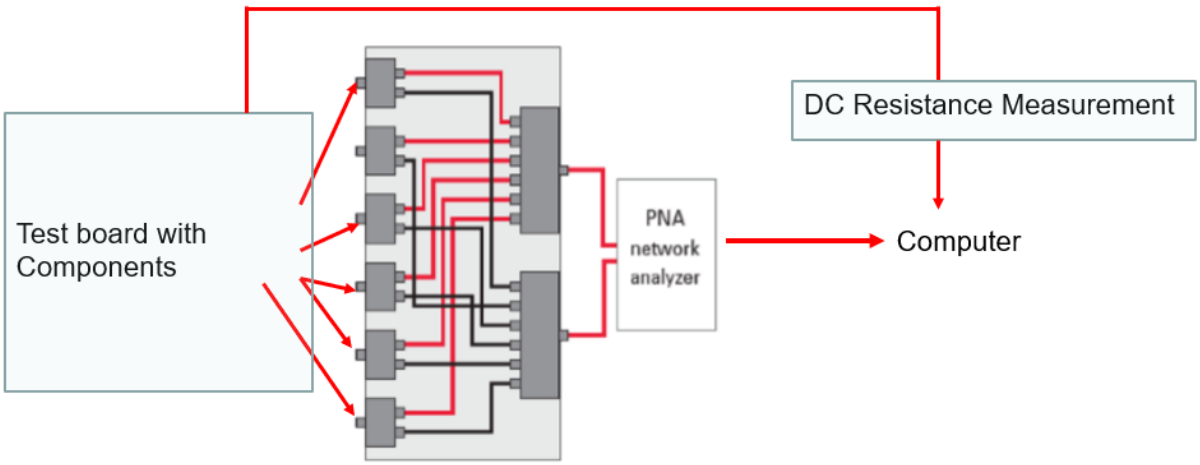

Figure 5: The switching system for the RF measurements

Results and Discussion

Failure Definition

DC-Resistance Monitoring: The direct current (i.e., low frequency) electrical resistance changes in the test boards were monitored at the corners of a dedicated circuitry (U2) mounted on the test board. As shown in **Figure 6** below, the DC resistance (R_{DC}) of all the four corners of the DC- test die remained constant for about the first 700 thermal cycles, and then changed rapidly as the joints failed with increasing thermal cycling. The onset of rapid R_{DC} increase was used as the failure point as shown in **Figure 6**.

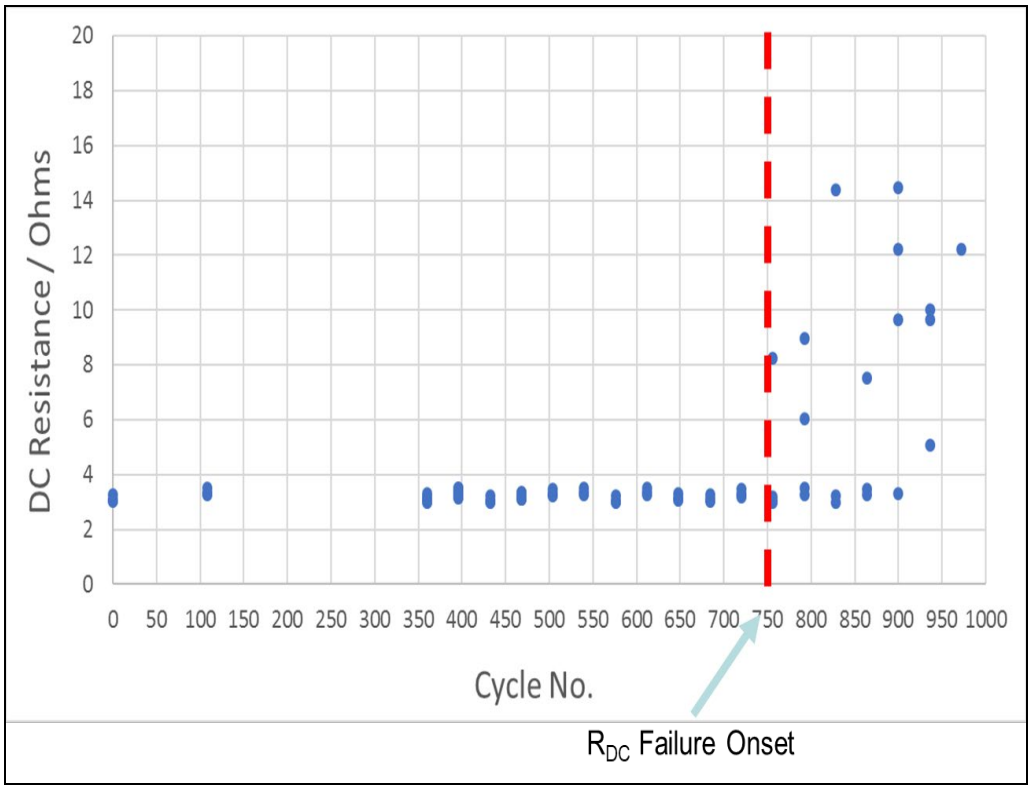

Figure 6: The evolution of the DC resistance of all the monitored DC-channels on a typical test board as a function of the number of thermal cycles.

Analysis of RF Data

Inspection of the accumulated experimental data revealed that both return loss, S11, amplitude and unwrapped phase (UP) angle afforded identical failure onset time at both frequencies. The following analyses focused only on the unwrapped phase (UP) angle of the return loss (S11) at 1 GHz for all the RF channels, **Figure 7** shows the evolution of the microwave signal phase at 1GHz for a single corner of a typical DUT as a function of thermal cycling. The figure shows several discrete breaks in the data evolution. The data for the first 300 cycles was used to characterize the break-in of the RF switches from mechanical wear of the electromechanical contacts.[13]. The initial 300 data points were used to set control limits of the 'aged' circuit and the onset of deviation from these control limits was used as the failure point. The stress duration before failure, using these definitions of failure as defined in Figures 6 and 7 respectively were used to generate the Weibull distribution plot in **Figure 8**.

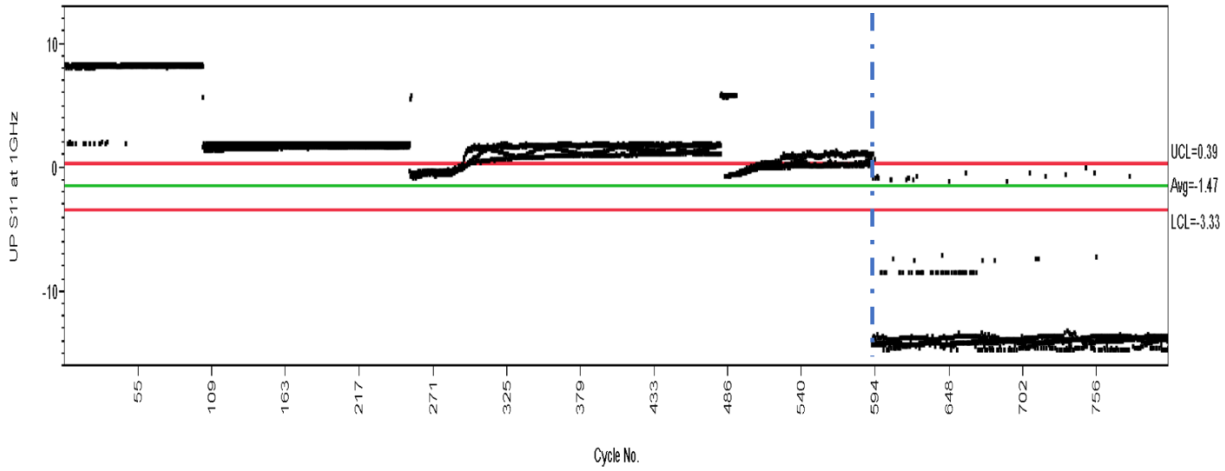

Figure 7: RF Monitoring (using S11 Phase changes at 1 GHz)

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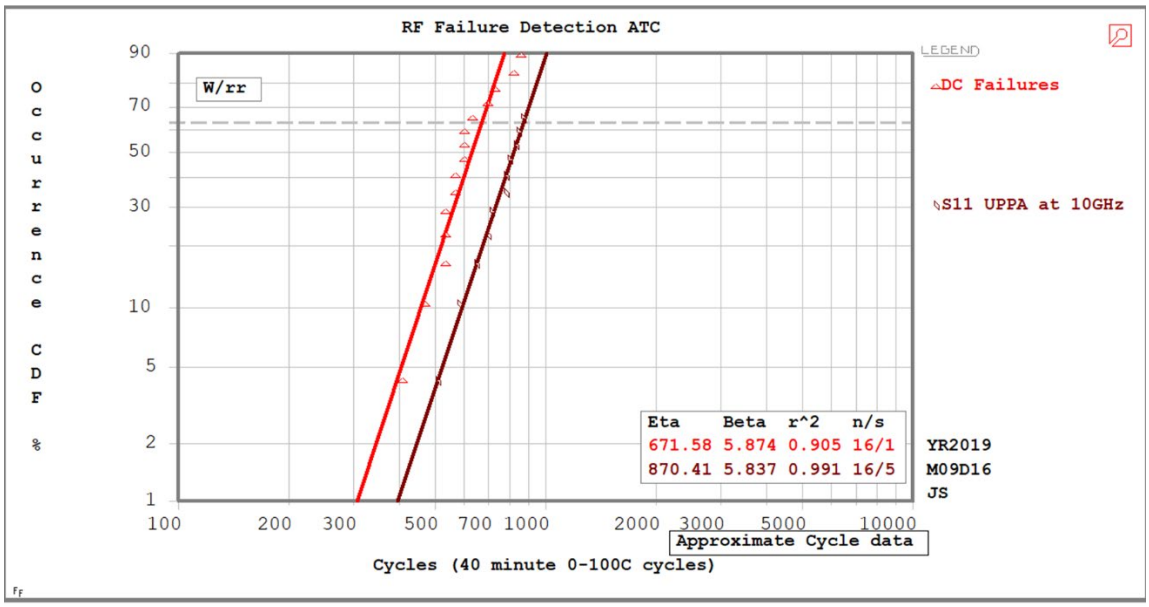

Figure 8: A Weibull distribution of the device failure times for R_{DC} and RF monitored components from Table 4. Clearly, the DC failures proceeded the RF failures.

Figure 9 shows the cross-section failure analysis of the failed waferscale CSP nets on a single board. These failed in all cases by solder fatigue as expected. Additional "Dye and Pry" analyses showed that both the RF and DC monitored components had similar failure patterns.

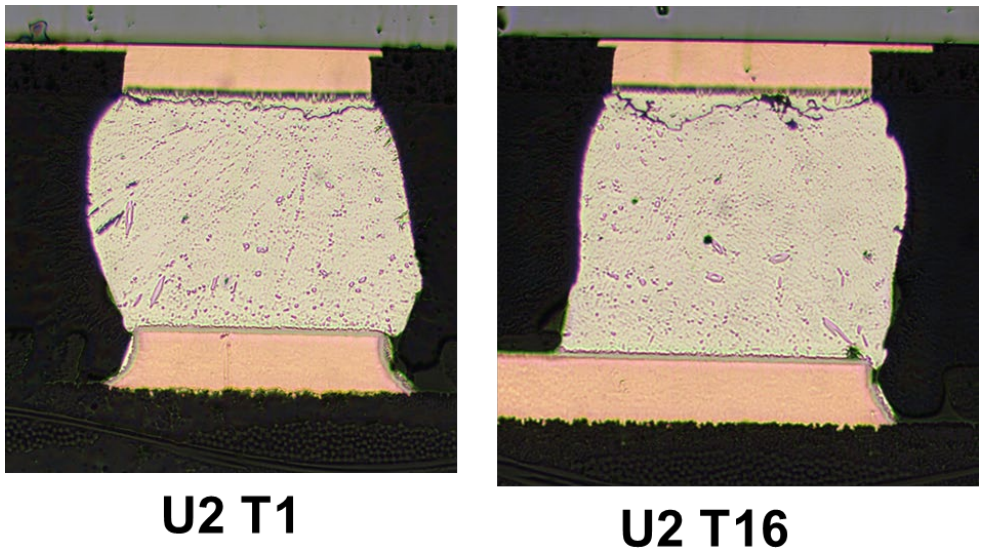

Figure 9: Cross-section of failed solder joints from two sample channels on a single test board. Similar for both the RF and DC monitored nets

Discussion of results and relevant electrical parameters

Previously published work on this subject reported that high frequency failures of the solder joint precede the DC failures[1-3]. Although the previous work was based on a very limited sample size, similar results were expected. In contrast, in the current report, the RF failures occurred after the DC failures. Current observations are explained at this point. When a crack opens or begins to open in a solder joint, it forms an air dielectric ($\varepsilon_r \approx 1$) capacitor, very similar to a parallel plate capacitor. The appearance of a change in a microwave measurement requires a change in the DC resistance (R_{DC}) of the joint. As the crack propagates, R_{DC} increases, and so does the capacitance (C). The prominence of microwave vs DC failure relates to the relative rate of increase of R_{DC} and C change. If R_{DC} (DC resistance of the crack) stays small until the crack fully propagates

across the joint, then it will not appear in a microwave measurement. As shown by the following theoretical analysis, if R_{DC} increases before the crack propagates all the way, then it would be observed in a microwave analysis and as well as in a careful DC measurement.

The value of the parallel plate capacitor is per the following formula:

$$C = \varepsilon_r \varepsilon_0 A/d \qquad \text{(Equation 1)}$$

Where C = Capacitance (in Farads)
ε_r = relative permittivity (dielectric constant)
$\varepsilon_0 = 8.85 \times 10^{-12}$ F/m (permittivity of free space)
A = Area of the capacitor plates (in meter^2)
d = distance between the plates (in meters)

The capacitive reactance of this capacitor, in ohms, varies as per the following formula:

$$X_c = 1/(2\pi fC) \qquad \text{(Equation 2)}$$

Where X_c is the Capacitive reactance in ohms, π is a constant (3.1416), f is frequency (hertz), and C is Capacitive reactance in ohms

From Equation 2, the capacitive reactance is smaller at the higher the frequencies, such that the capacitor acts like a short circuit at high frequencies. It varies per the curve shown below in Figure 10, below.

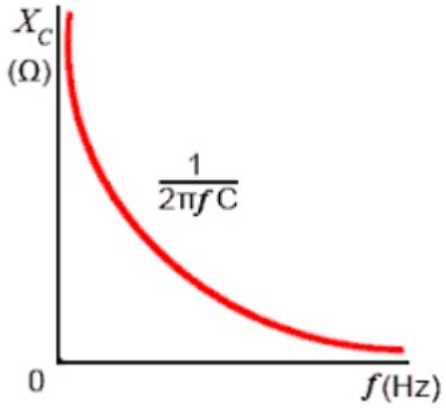

Figure 10: Capacitive reactance as a function of the frequency

It is obvious from equation 2 that the capacitive reactance also varies inversely to the capacitance, viz., the larger the capacitance, the smaller the capacitive reactance. Equation 1 shows that the capacitance value increases with decreasing separation distance between the plates of the capacitor. A typical fatigue solder joint crack has a very small distance between the "plates" resulting in a relatively large capacitance, even with the very small capacitor plates of a solder joint, until the solder joint fully opens and the joint separates. The crack surfaces are very nearly in contact up until the joint fully fails and the 'plates' become physically detached. The crack dimension, typically less than 1μm – on the order of about 0.1 μm (0.1 x 10^{-6} m) -- can be measured from the scanning electron micrographs of failed solder joints.

For the 0.5 mm waferscale CSP used in this testing, the crack area, which would be the capacitor plate size, is going to be very close to that of the pad size (0.3mm diameter), probably larger since the crack path is not straight. This is 7.069 x10^{-8} m^2. The rough approximate resulting capacitance for a fully open solder joint is

$$((8.85 \times 10^{-12}) \text{ x } (7.069 \text{ x} 10^{-8}))/ 0.1 \text{ x } 10^{-6} = 6.26 \text{ x } 10^{-12} \text{ Farads.}$$

The capacitive reactance for this at 10GHz is $1/(2\pi \text{ x } (1\text{x}10^{10}) \text{ x } (6.26 \text{ x } 10^{-12})) = 2.5$ ohms.

For a non-fully open solder joint, and, also for an "open" solder joint (the resistance of the "open" solder joint is considerably higher – usually over 1000 ohms), looking specifically at the crack and the crack alone (ignoring the rest of the circuit), the equivalent circuit schematic is shown in **Figure 11** below.

Here R is the resistance of the crack, L is the inductance of the crack, and C is the capacitance of the crack.

Considering the geometry of the solder joint crack, it is safe to consider the inductance of the crack to be zero. The capacitance of the crack was roughly estimated above. Until the crack is open, the resistance of the crack is going to be extremely low. The resistivity of tin is approximately $1x10^{-7}$ Ω-m. Resistance is equal to (resistivity x length) / area. Using the crack length number above and assuming a crack area equal to 75% of the crack area above (i.e. 25 % contact), the resulting resistance of the remaining attached solder in the crack is:

$$R = (1x10^{-7} \times 0.1x10^{-6}) / (.25 \times 7.068583x10^{-8}) = 5.66 \times 10^{-7} \text{ ohms}$$

The impedance, Z, is given by equation 3:

$$Z = 1/\text{Sqrt}\ ((1/R)^2 + (1/X_C + 1/X_L)^2) \qquad \text{(Equation 3)}$$

After calculating capacitive reactance and resistance above, one can ignore the inductive reactance. So, plugging in the number for resistance and capacitive reactance (and using 75% of that value), one can estimate Z as 5.66×10^{-7} ohms as the very low resistance dominates.

$$\text{Conductance } G = 1/R = 1.767 \times 10^6 \qquad \text{(Equation 4)}$$

And

$$\text{Admittance } Y = 1/Z = 1.767 \times 10^6 \qquad \text{(Equation 5)}$$

One can now estimate the phase angle, using equation 6, and relate this to the S-parameters in this testing. The phase angle will not change even if only a small portion of the joint is still attached; the phase angle will change if there is a complete break.

$$\text{Cosine } \varphi = G/Y = 1, \text{ so } \varphi = 1. \qquad \text{(Equation 6)}$$

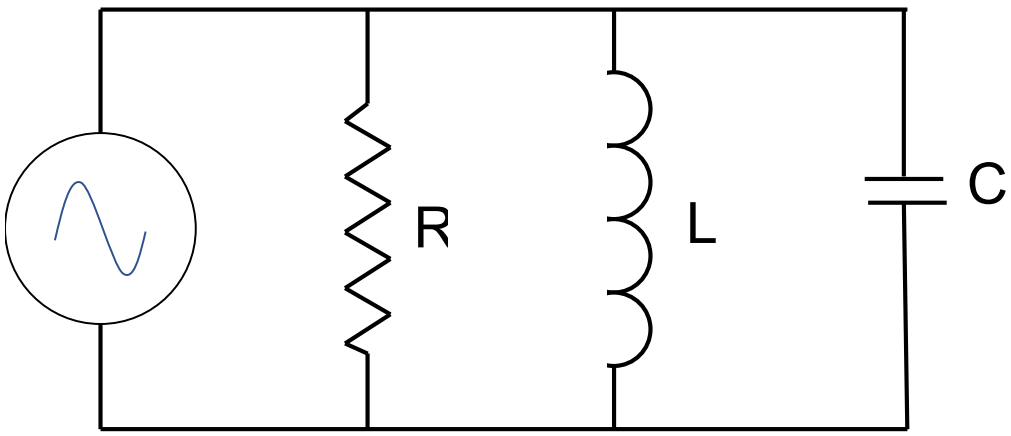

Figure 11 Solder Crack Equivalent Circuit

The insertion loss (S21) will only see degradation of the signal and the changes to the circuit as detailed above will be very small compared to the losses in the entire circuit. At very high frequencies, low resistance dominates the crack properties, and will not be seen until the crack opens completely so that the resistance is substantially increased. It generally takes multiple cycles after a DC open to create a significant separation of the solder joint. This, and the polling frequency, which is by necessity much lower than for DC monitoring, may help explain why the RF data suggests that the solder joints fail later.

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The theoretical analysis also shows why failures would be identified at the same cycle if the analysis is done using insertion loss, return loss, or unwrapped phase angle as the measurand. Return loss will see a change in impedance. The analysis above shows impedance is overwhelmingly driven by the very low resistance of even a small remaining portion of the solder joint. After the crack opens and the resistance becomes very high, then the capacitive reactance drives the impedance and it will go up. Since the impedance of the crack is dominated by the low resistance and the conductance is also dominated by the low resistance, the phase angle change from the crack is effectively zero until the crack opens, when both impedance and conductance change. The theoretical analysis agrees with the results obtained in this work; RF monitoring will not see a failing solder joint until during, or even after, DC monitoring of the same solder joint, as shown by the statistical analysis (Weibull plot, Figure 7)

Conclusions

The following are the conclusions from this work:

1) The historical DC based solder joint failures and solder joint reliability evaluations methods are also acceptable for high frequency circuits.
2) Failures in high frequency circuits from solder joint cracking are expected to be detected simultaneously or even after failures are detected with DC methods, as the resulting capacitance of the solder joint crack is effectively a short circuit for high frequency circuits.
3) The capacitance and associated capacitive reactance, formed by a partial crack in a solder joint is so much larger than the very small resistance of a tiny remaining amount of intact solder joint. The ultimate effect on the circuit is unmeasurable until the crack is fully open. The low resistance dominates the circuit.

Recommendations for future work

The analysis reported in this paper was based on a 0.5mm pitch Waferscale CSP device with very small solder joints. While the results are expected to be reproducible, a more extensive study, especially with devices with larger solder joints, or much smaller solder joints, would be required to verify the universality of the observations and conclusions.

For the proposed validation studies, a dedicated VNA is recommended for each net in order to avoid complications in the data analysis from the use of multiplexers and high frequency switches which complicate and add to measurement variations and uncertainties.

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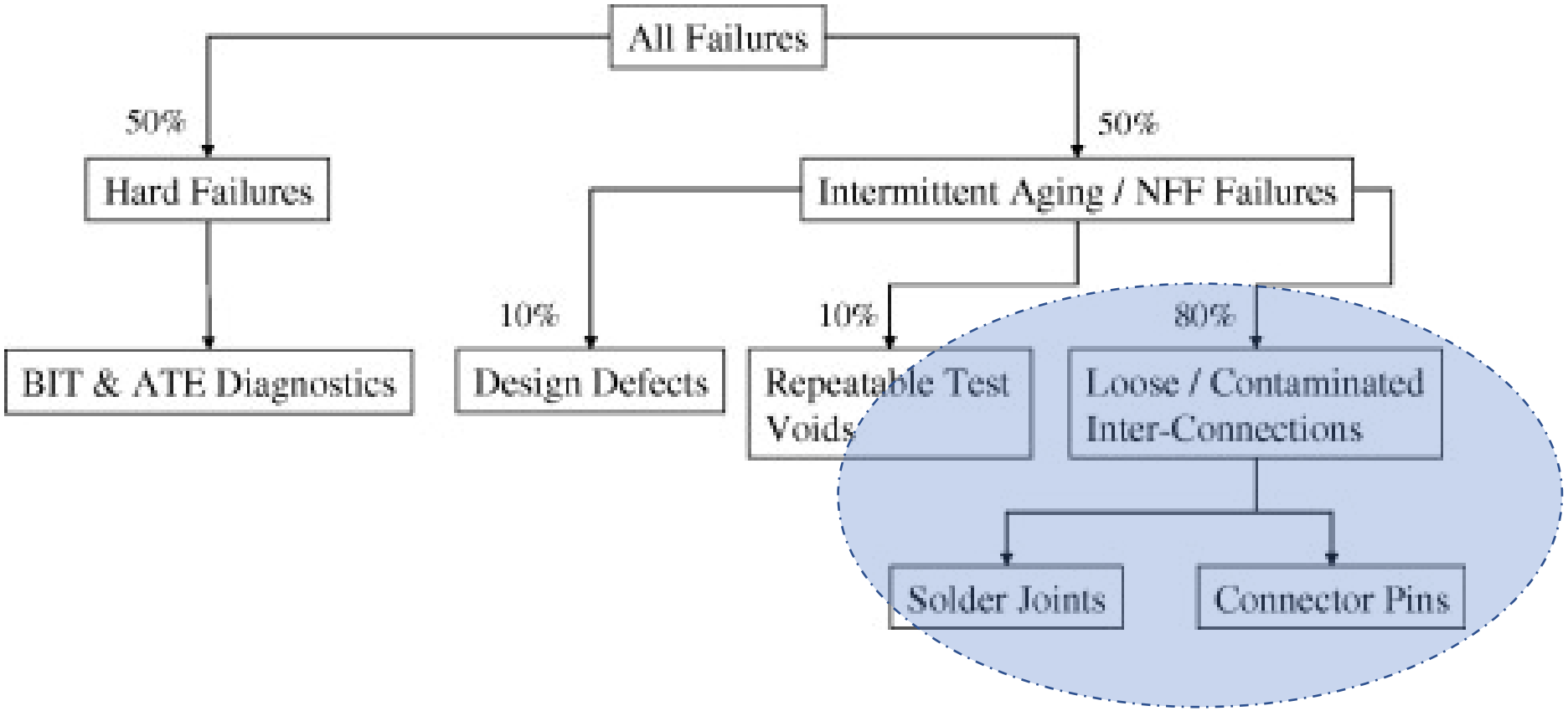
Technical Conference March 9–12, 2021

Talk Outline

- Purpose
- Theory and Monitoring Metrics
- Test Vehicle Design
- Test Results
- Failure Analysis
- Explanation of Results
- Conclusions

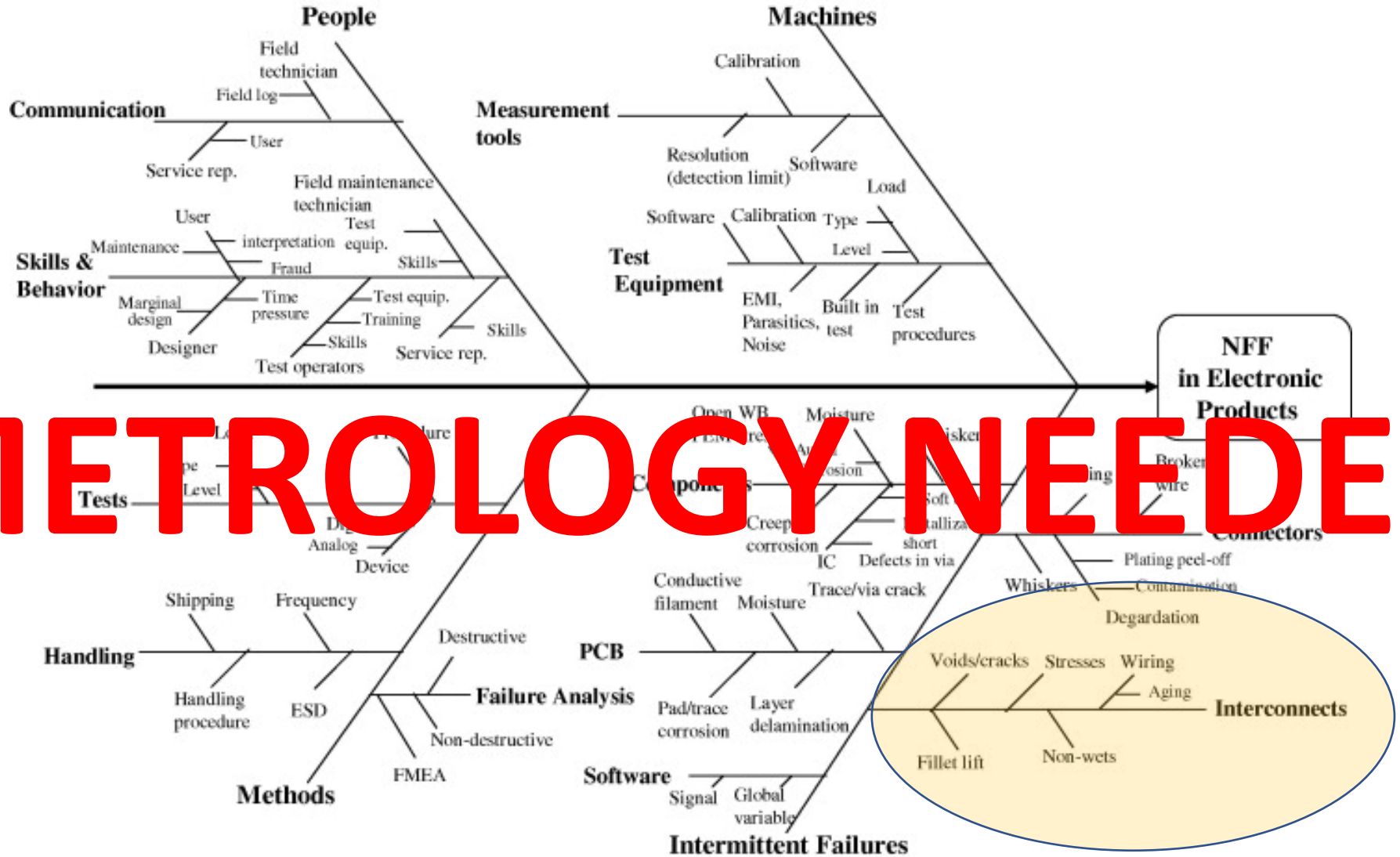
Hard and NFF Failures in Avionics



NFF failures costs the Defense Department (DoD) more than $2 billion annually

H. Q et al., Microelectronics Reliability, 2008, 48, 5, 663-674, doi: /0.1016/j.microrel.2008.02.003
C. Adams, Aviation Maintenance , 2014: Pages 26 -32.

Fish-Bone Diagram of NFF Issues



H. Q et al., Microelectronics Reliability, 2008, 48, 5, 663-674, doi: /0.1016/j.microrel.2008.02.003

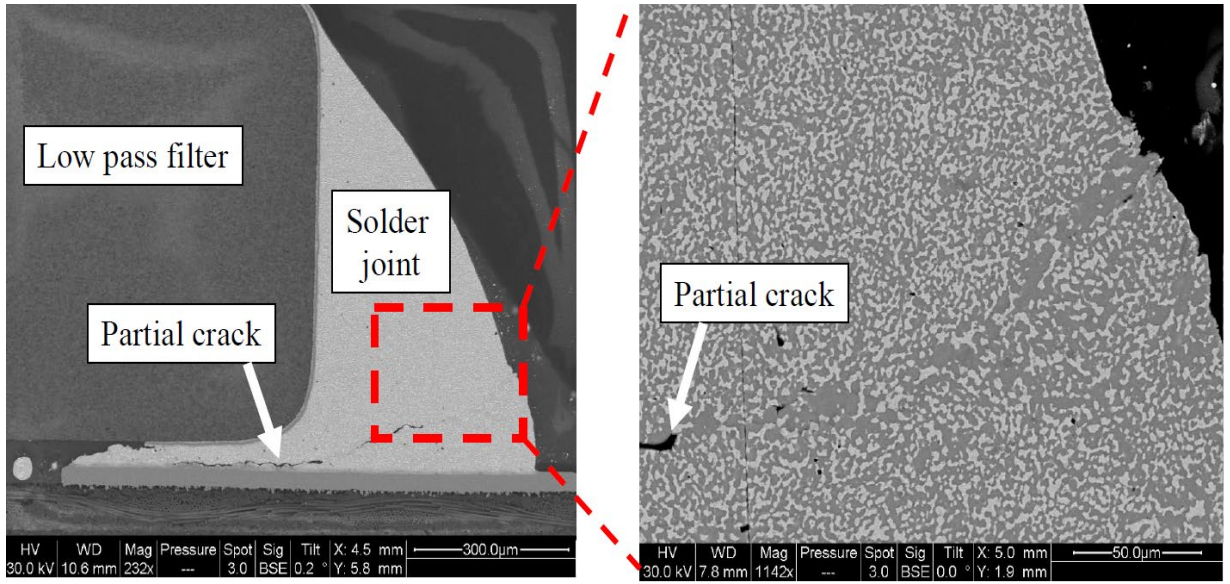
Purpose of the Work

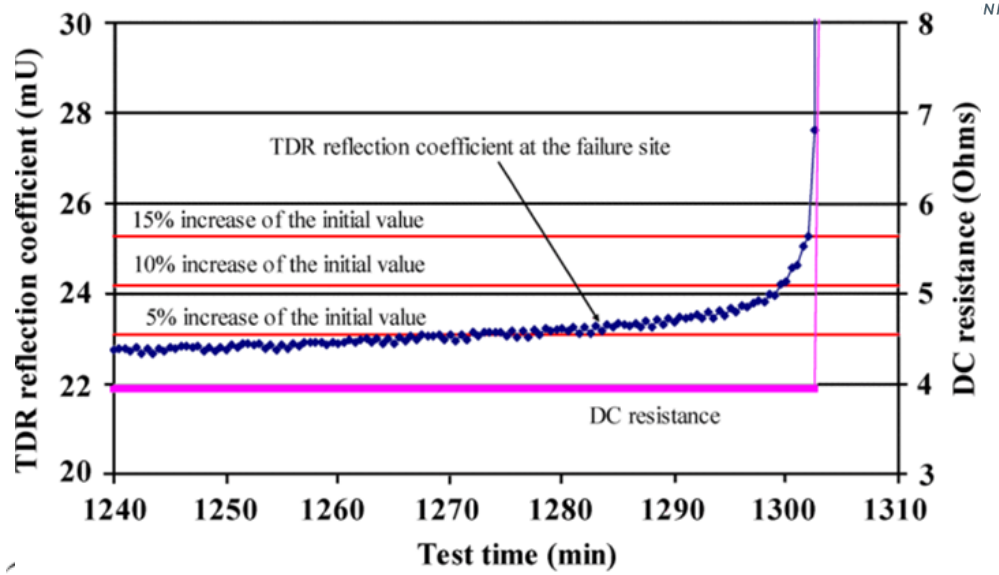
Determine whether RF-Based Is More Sensitive Than DC-Resistance Metrology in Detecting Solder Joints Degradation.

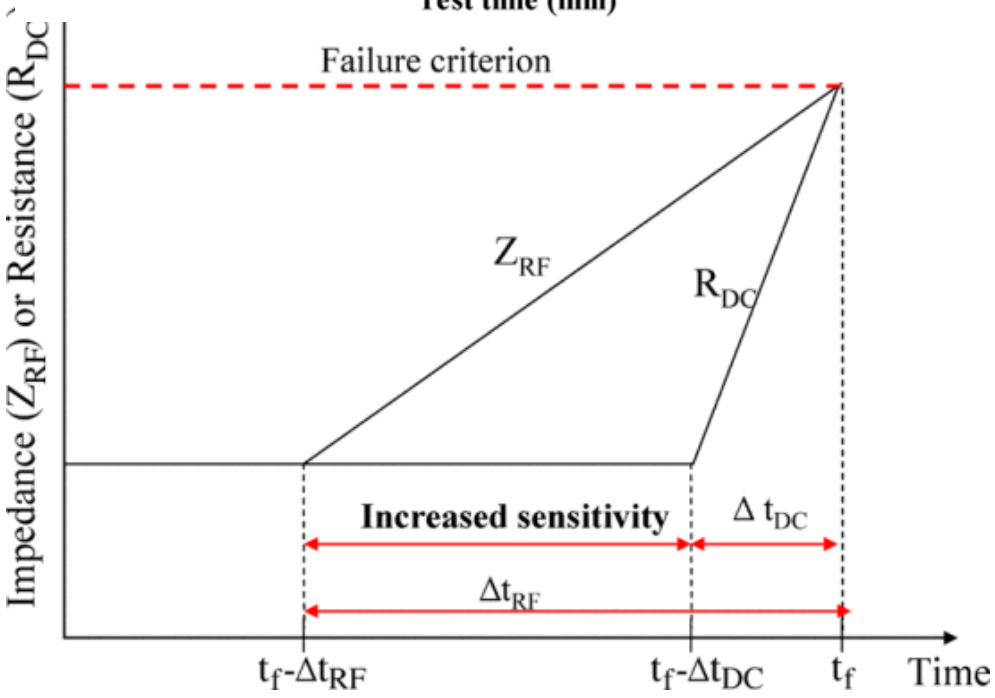
The goals:

- Understand the impact of defects on RF- and DC signal losses in I/O assemblies
- Use the signal loss phenomena to detect incipient defect formation, and determine the onset of performance limitation
- Statistically determine the differences between DC- and RF- detection capability for solder joints in thermal cycling
- Perhaps change our definition of the “failed” solder joint
- Potentially explain many No Failure Found (NFF) field returns

RF Signal Losses Due to Pre-catastrophic Solder Joint Failure







D. Kwon, et al., IEEE Transactions on Device and Materials Reliability, vol. 9, no. 2, pp. 296-304, June 2009

RF Monitoring Metrics

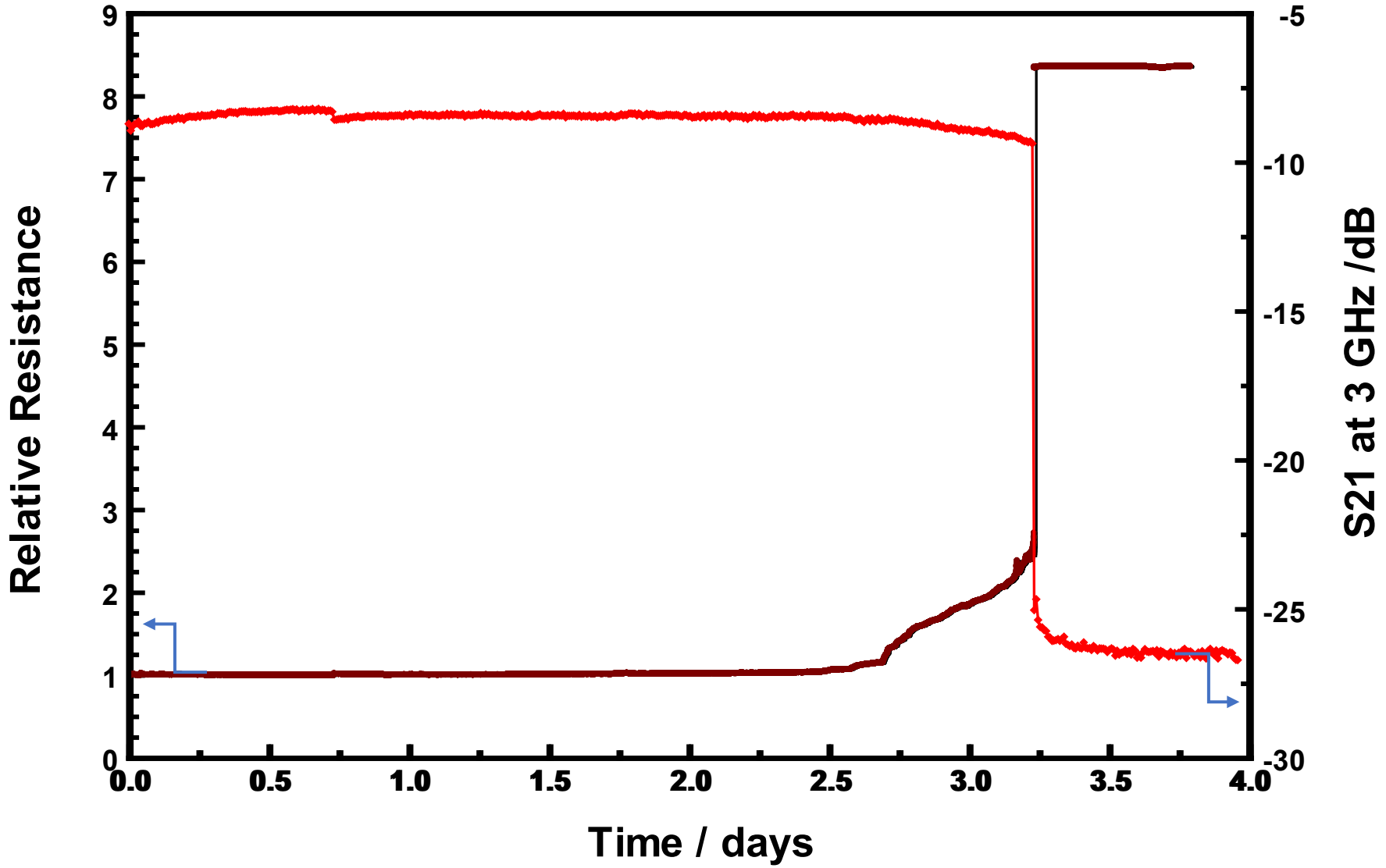
Direct Measurands

1. Insertion Loss (S21, S12)
   → Energy lost (usually as heat) due to impedance change
2. Return Loss (S11, S22):
   → Energy returned to source due to impedance change
3. TDR (time domain reflectance)
   → travel time between source and defect site

Calculated Measurements

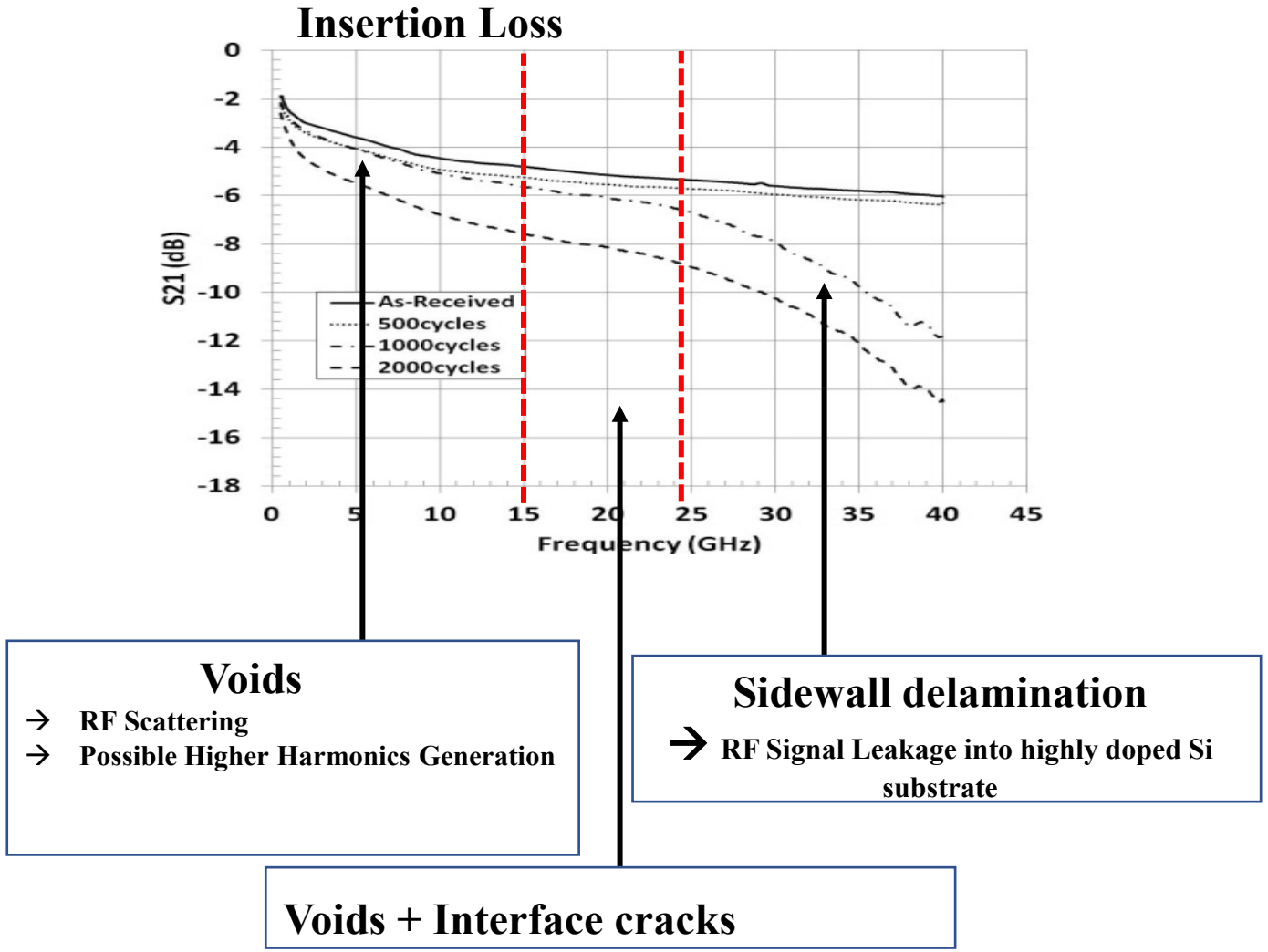
1. Attenuation Constant
   → Total microwave energy loss from the dielectric and skin effect losses
2. RF Phase
3. Group Delay

CORRELATION BETWEEN RF INSERTION LOSS (S21) AND DC REISTANCE (R_{DC})



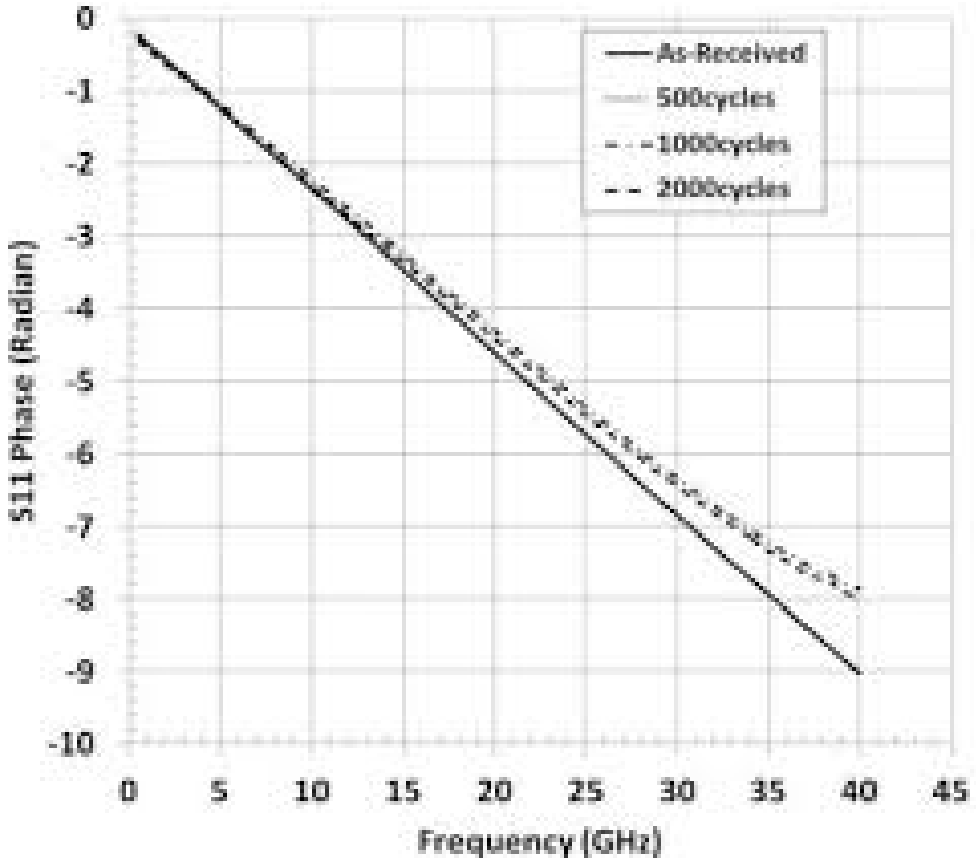
Christopher E. Sunday; et al., Journal of Applied Physics 2017, 122, DOI: 10.1063/1.4992135
Papa K. Amoah, et al., Microwave Monitoring of Atmospheric Corrosion of Interconnects. ECS Journal of Solid-State Science and Technology 2018, 7:12, N143-N149.

Insertion Loss (S21) as Thermomechanical Reliability Probe



Okoro et al. ,"Accelerated Stress Test Assessment of Through-Silicon Via Using RF Signals", IEEE TRANSACTIONS ON ELECTRON DEVICES, 60 (6), J, 2013 pp 2015-2021

Return Loss (S11) Phase as Thermomechanical Reliability Probe



Unwrapped Phase Angle

$$Phase\ Shift\ \phi = \arctan \frac{1}{2\pi fRC}$$

Okoro et al. ,"Accelerated Stress Test Assessment of Through-Silicon Via Using RF Signals", IEEE TRANSACTIONS ON ELECTRON DEVICES, 60 (6), J, 2013 pp 2015-2021

S-parameters Afford Complete Suite Of Electrical Parameters

$$R = \mathrm{Real}\left(Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right)$$

$$L = \frac{\mathrm{Imag}}{\omega}\left(Z_0 \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{2S_{21}} \right)$$

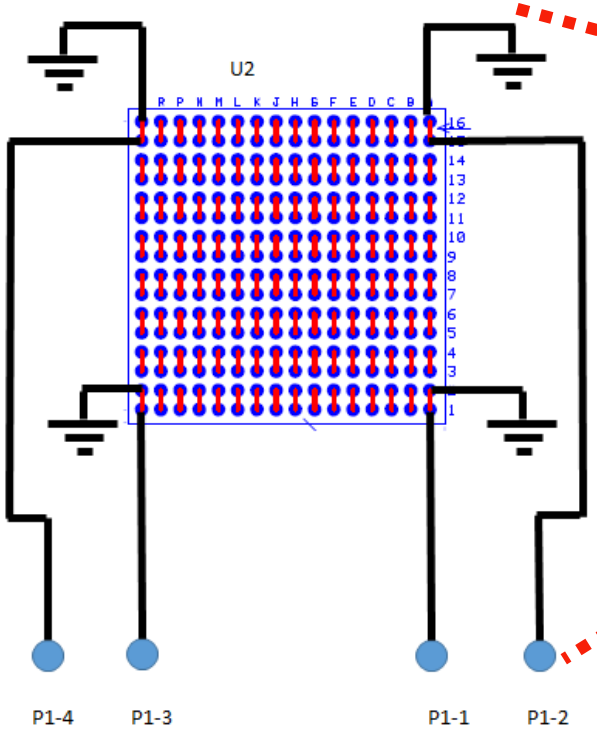
$$G = \mathrm{Real}\left(\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{21}}{Z_0((1+S_{11})(1+S_{22}) - S_{12}S_{21})} \right)$$

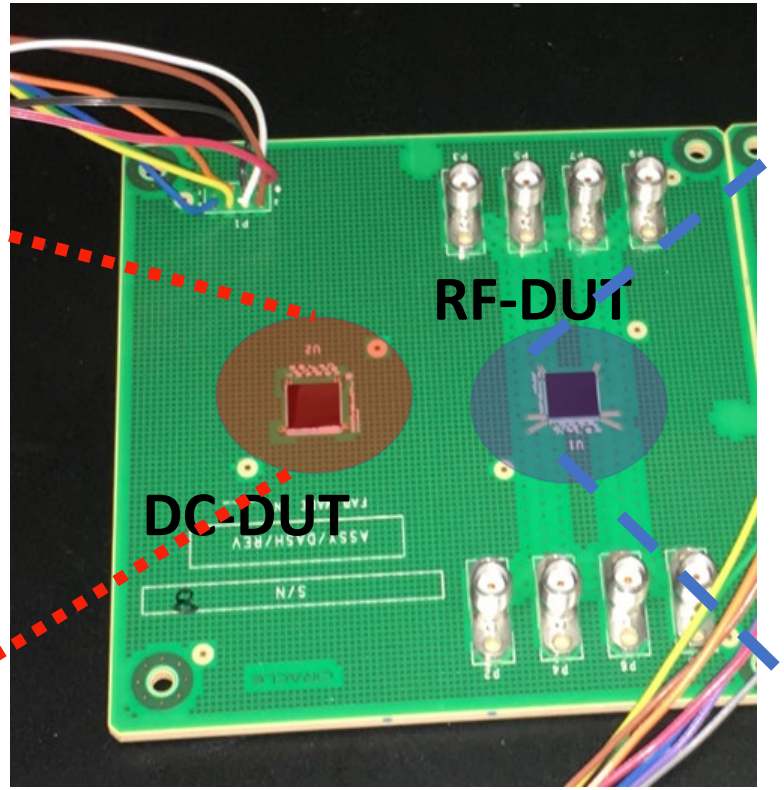
$$C = \frac{\mathrm{Imag}}{\omega}\left(\frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{21}}{Z_0((1+S_{11})(1+S_{22}) - S_{12}S_{21})} \right)$$

Device Wiring for In Situ Monitoring

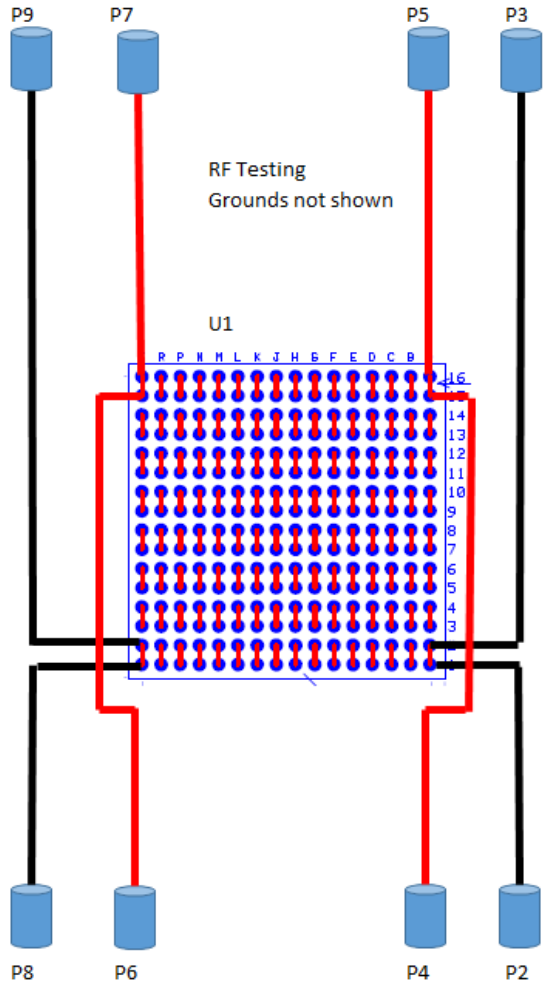
DC-DUT

DC testing , Connector Ground pins not shown

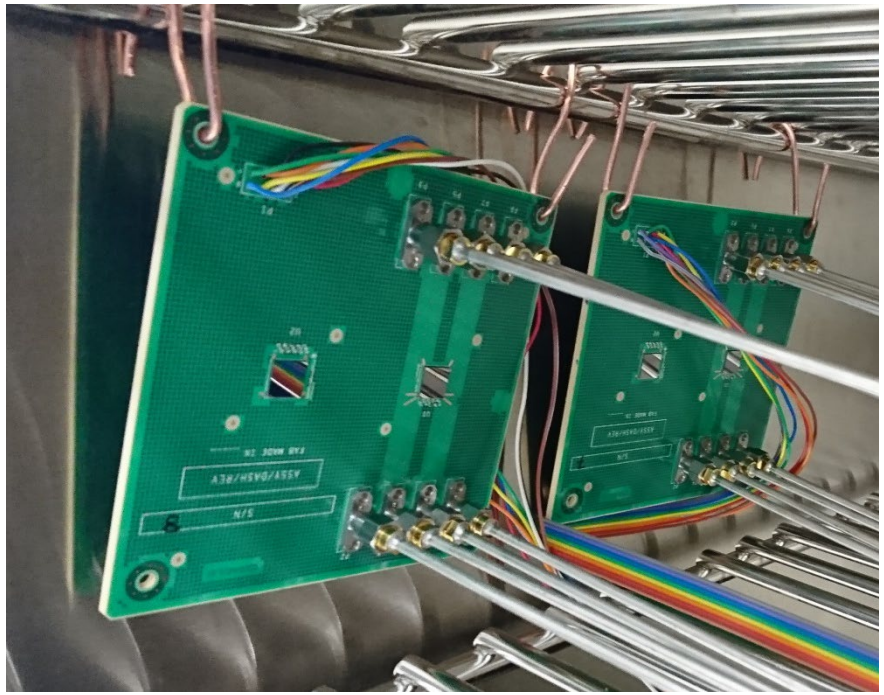


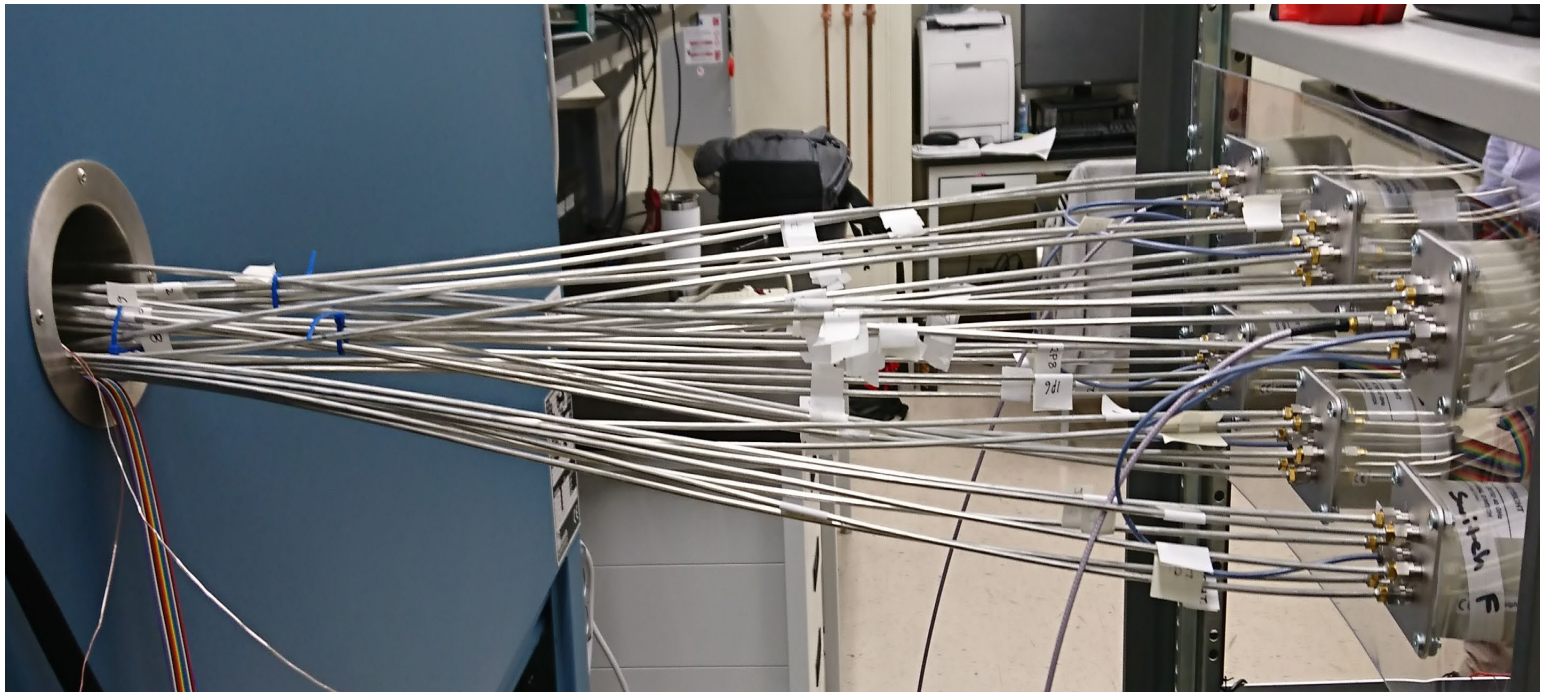


RF-DUT



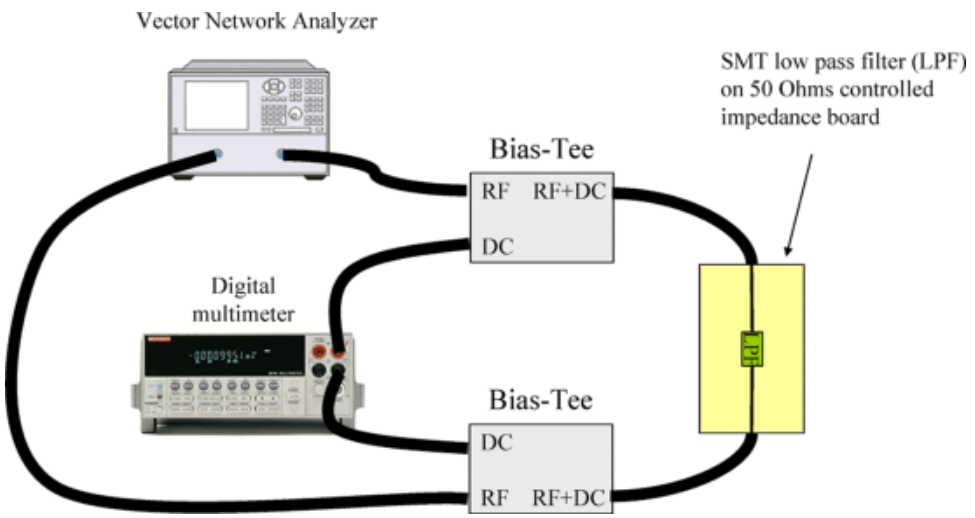
Boards Mounting and Connections to Switches





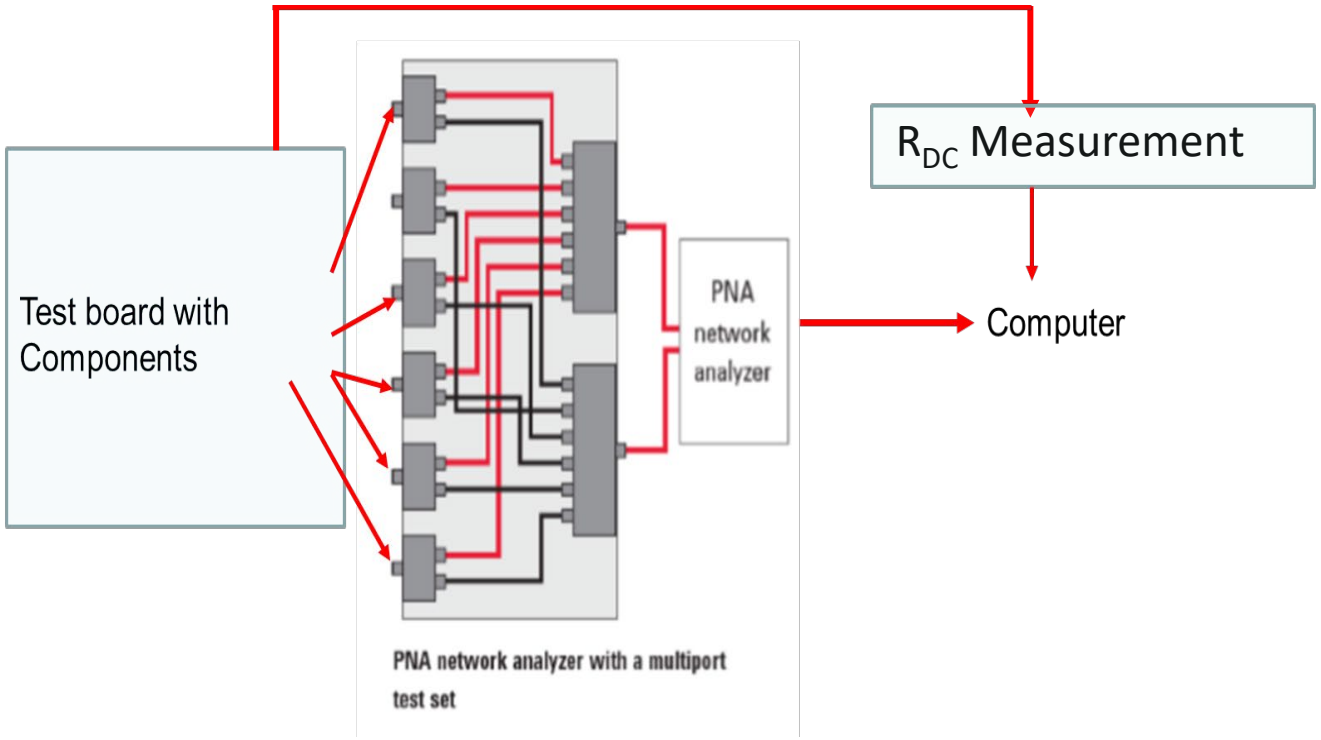
In-Situ Monitoring: 2 Ways to Run the Test

Single Device Tested with 2 Circuits (RF and DC)

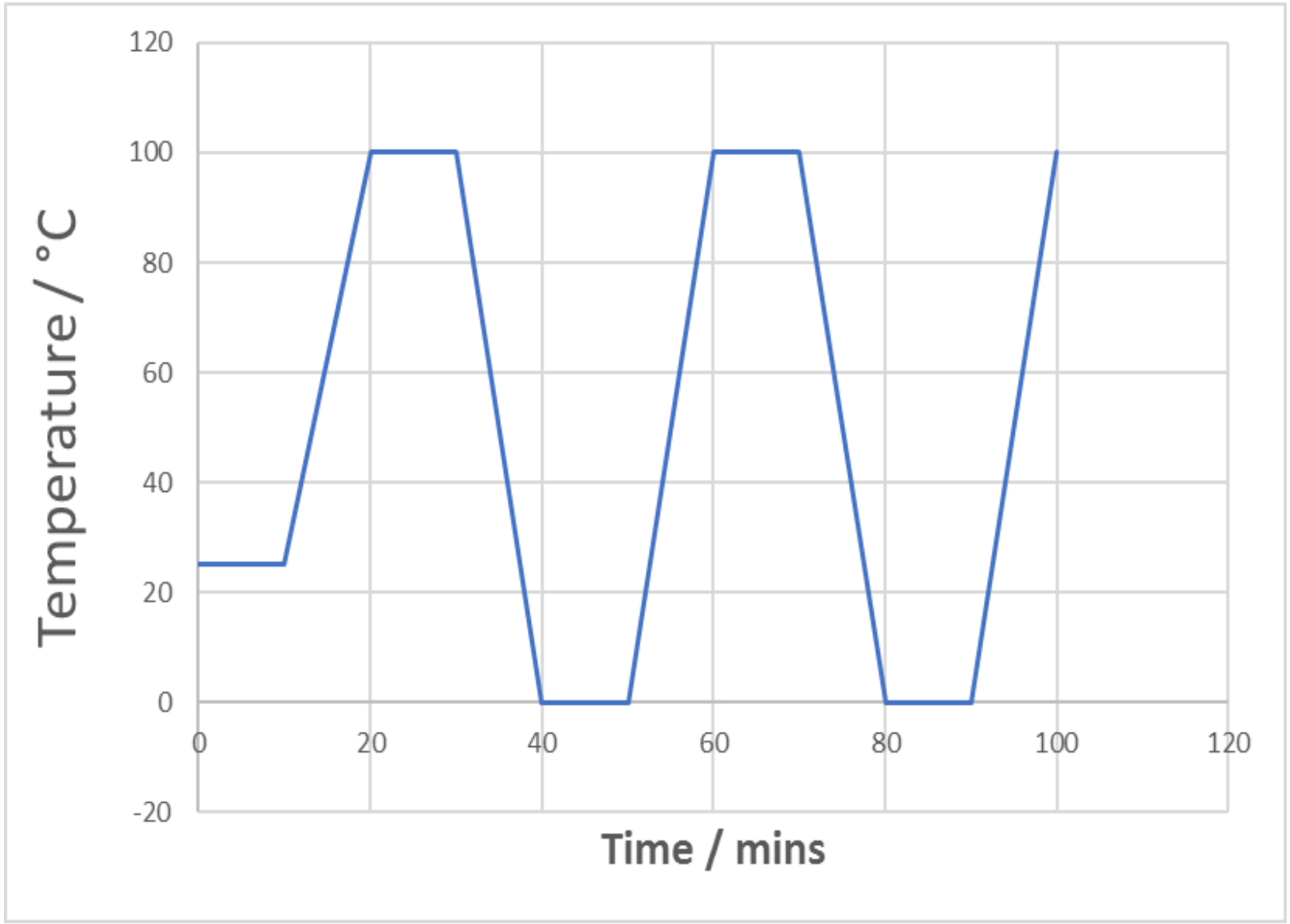


D. Kwon, M. H. Azarian and M. Pecht, IEEE Transactions on Device and Materials Reliability, vol. 9, no. 2, pp. 296-304, June 2009

Multiple Devices Tested with 2 Circuits (RF and DC)

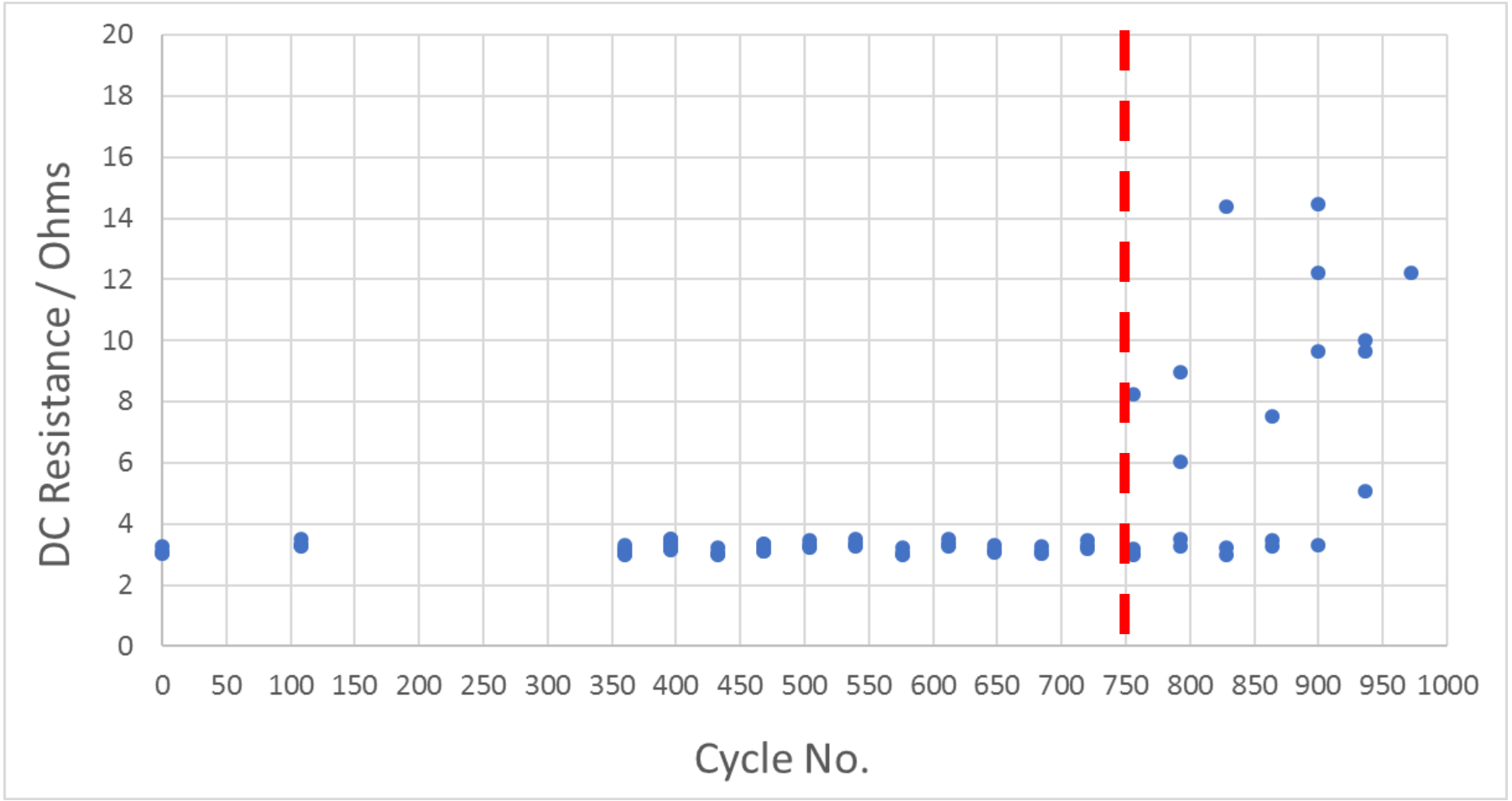


Thermal Cycle Profile

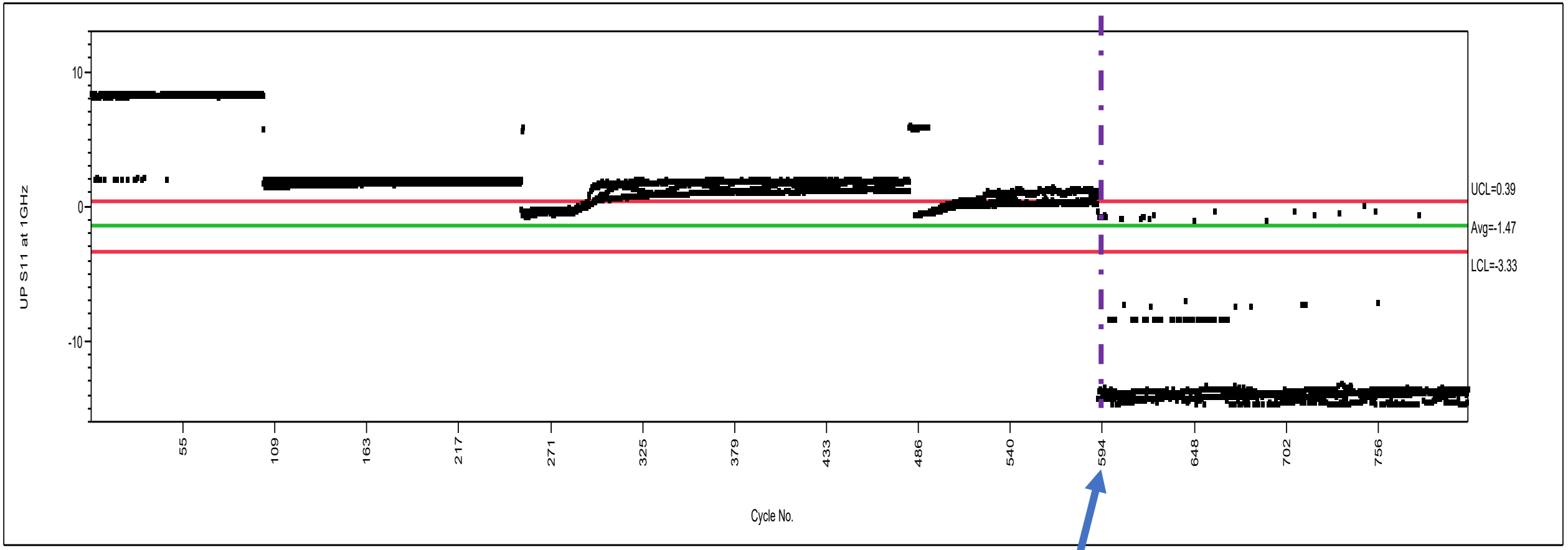


1000 cycles of :
10 min ramp-up
10 min soak
10 min ramp-down

Typical DC-Resistance Evolution



Typical RF Phase Angle Evolution



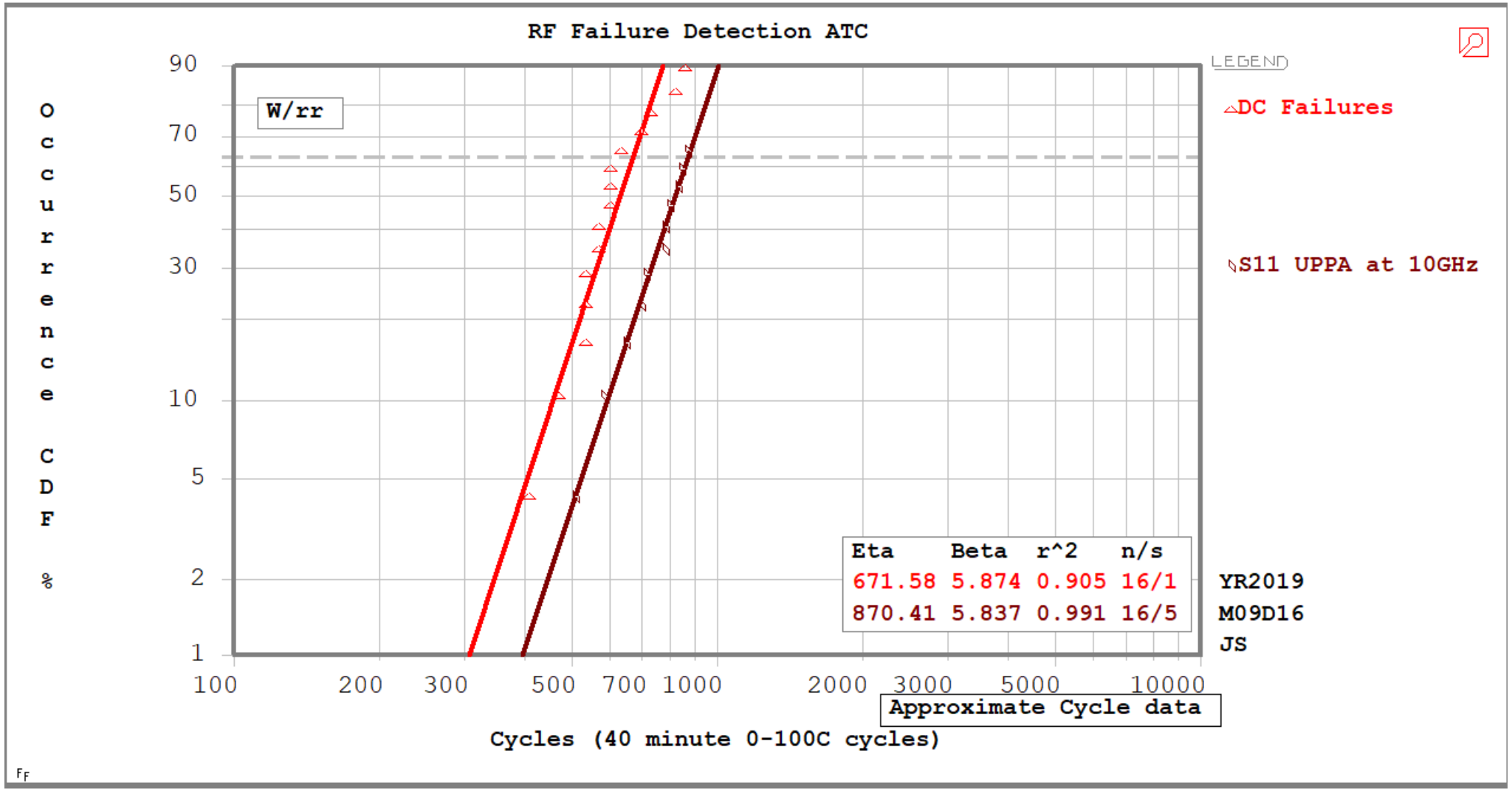
S11 Phase Angle at 1 GHz

RF Failure Onset

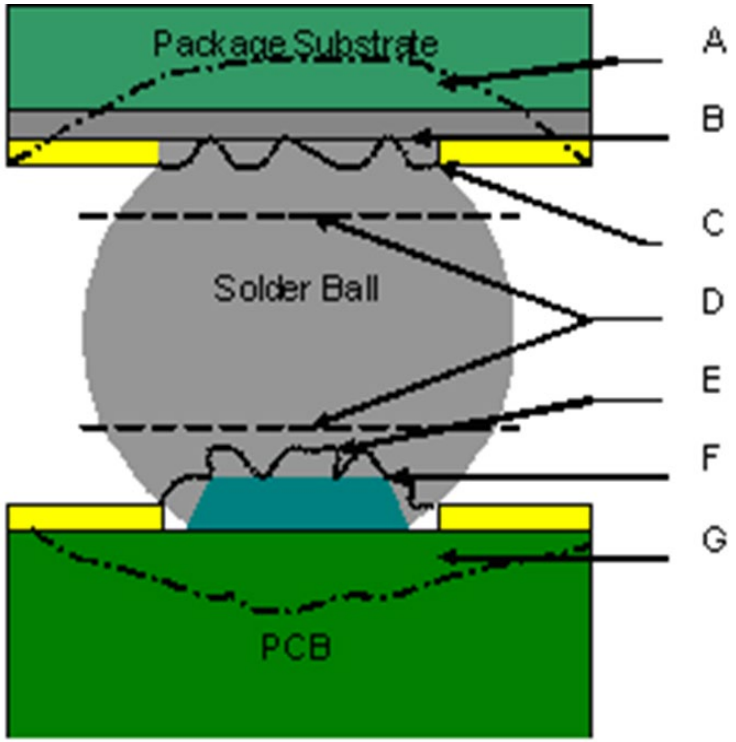
Potential Sources of Uncertainties in the RF Data

- Uncompensated temperature dependent gradients along semi-rigid cable characteristics during the thermal cycling.
  - This could add quite a bit of noise in the measurement.
  - We were unable to correlate noise in RF data with temperature transitions during the thermal cycling
- Mechanical aging of metallic contacts in the RF switch / relay network
  - Possible fretting of contact surfaces?

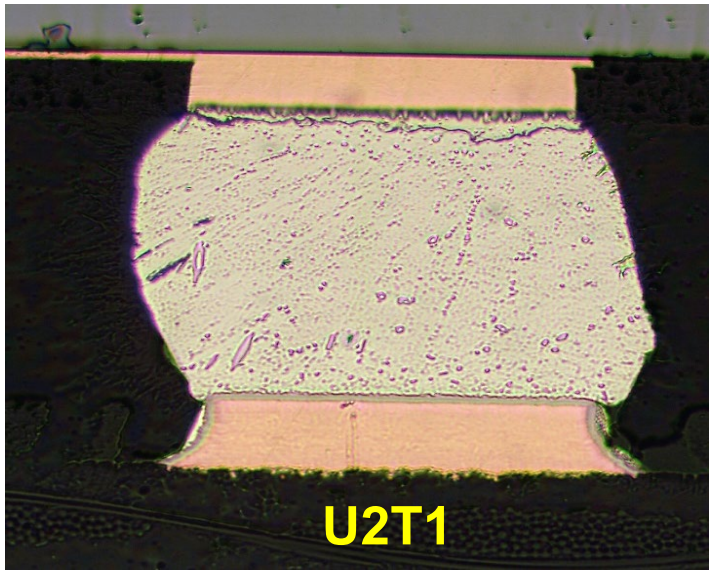
R_{DC} vs RF Failure Rates

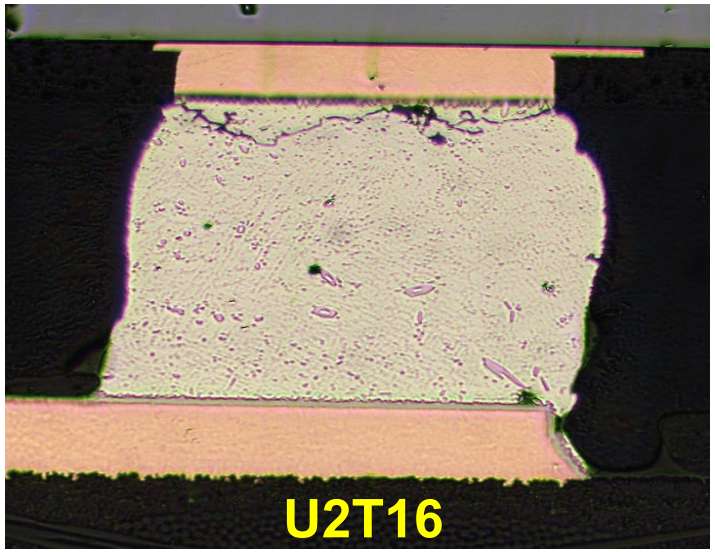


Physical Failure Analysis



A Package Pad Lift/Crater
B Pkg Base Metal/IMC Interface Fracture
C Pkg IMC/Solder Interface Fracture
D Bulk Solder Fracture
E PCB IMC/Solder Interface Fracture
F PCB Solder pad/IMC Interface Fracture
G PCB Pad Lift/Crater



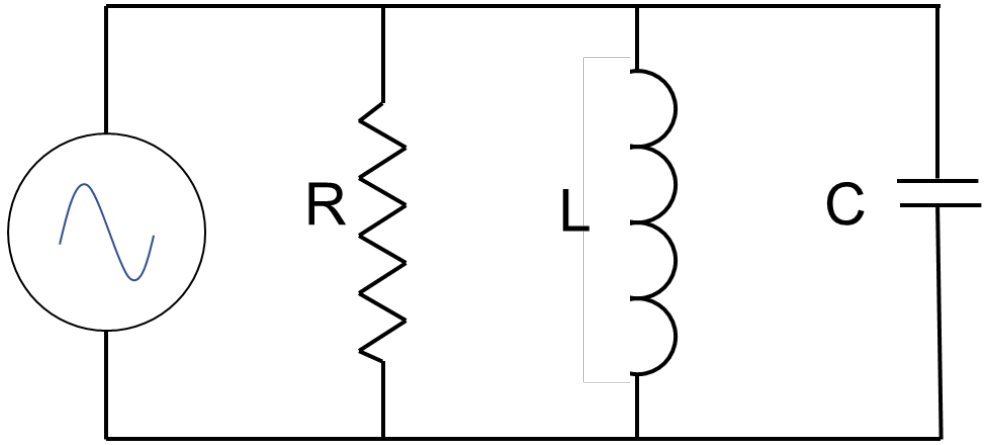


"METHODOLOGY TO CHARACTERIZE PAD CRATERING UNDER BGA PADS IN PRINTED CIRCUIT BOARDS" in the Proceedings of the Pan Pacific Microelectronics Symposium, Kauai, Hawaii, January 22 – 24, 2008.

Summary of Observations

- The DC failures preceded the RF failures
  - R_{DC} monitoring technique predicted shorter lifetimes than the RF monitoring.
- The return loss (S11) metrics (i.e., Amplitude and Unwrapped phase (UP) angle) afforded the identical failure onset time at both frequencies.
- Solder joint failed by fracture at / near the IMC-Solder interface.

Why the Difference Between R_{DC} and RF Lifetime Results?



Solder Crack Equivalent Circuit

Key Point *: As long as there is still a Connection in the crack, R dominates the impedance*

(akin to a Passive High Pass Filter)

- X_L so small it can be ignored
- $X_c = 1/(2\pi fC)$ = for a crack ~ 2.5ohms at 10GHz
- R crack = Extremely small (~5.7×10^{-7} ohms) until solder joint opens -
- $Z = 1/\text{Sqrt}((1/R)^2 + (1/XC + 1/XL)^2) = 5.66 \times 10^{-7}$ ohms – R dominates

Conclusions

- DC methods for evaluating solder joint failures and solder joint reliability are acceptable for high frequency circuits.

- The capacitance and associated capacitive reactance that is formed by a partial crack in a solder joint is so much larger than the very small resistance of an even tiny remaining amount of intact solder joint that the ultimate effect on the circuit is unmeasurable until the crack is fully open. ***The low resistance dominates the circuit.***

- Failures in high frequency circuits from solder joint cracking are expected to be detected simultaneously or even after the failures are detected with DC
  - The resulting capacitance of the solder joint crack is effectively a short circuit for high frequency circuits.

Recommendations For Future Work

- More extensive experiment would be required to verify and validate our conclusions.

- Have a dedicated VNA for each net. The use of long cables, multiplexers and high frequency switches complicates the data analysis and results in higher noise, uncertainty and variability.