RESEARCH ARTICLE | JANUARY 12 2021

Cryogenic microwave loss in epitaxial Al/GaAs/Al trilayers for superconducting circuits ⊘

C. R. H. McRae ✉ ; A. McFadden; R. Zhao; ... et. al

Check for updates

CHORUS

View Online   Export Citation   CrossMark

Articles You May Be Interested In

Concentric transmon qubit featuring fast tunability and an anisotropic magnetic dipole moment

Appl. Phys. Lett. (January 2016)

Analog Ising chain simulation with transmons

AIP Conference Proceedings (June 2020)

Towards merged-element transmons using silicon fins: The FinMET

Appl. Phys. Lett. (August 2022)

AIP Publishing

Cryogenic microwave loss in epitaxial Al/GaAs/Al trilayers for superconducting circuits

View Online   Export Citation   CrossMark

C. R. H. McRae,[1,2,a] ⓘ A. McFadden,[3] ⓘ R. Zhao,[1,2] ⓘ H. Wang,[1,2] ⓘ J. L. Long,[1,2] T. Zhao,[1,2] S. Park,[1,2] M. Bal,[1,2] ⓘ C. J. Palmstrøm,[3,4] ⓘ and D. P. Pappas[2]

AFFILIATIONS

[1]Department of Physics, University of Colorado, Boulder, Colorado 80309, USA
[2]National Institute of Standards and Technology, Boulder, Colorado 80305, USA
[3]Department of Electrical and Computer Engineering, University of California, Santa Barbara, California 93106, USA
[4]Materials Department, University of California, Santa Barbara, California 93106, USA

[a]Author to whom correspondence should be addressed: coreyrae.mcrae@colorado.edu

ABSTRACT

Epitaxially grown superconductor/dielectric/superconductor trilayers have the potential to form high-performance superconducting quantum devices and may even allow scalable superconducting quantum computing with low-surface-area qubits such as the merged-element transmon. In this work, we measure the power-independent loss and two-level-state (TLS) loss of epitaxial, wafer-bonded, and substrate-removed Al/GaAs/Al trilayers by measuring lumped element superconducting microwave resonators at millikelvin temperatures and down to single-photon powers. The power-independent loss of the device is $(4.8 \pm 0.1) \times 10^{-5}$, and the resonator-induced intrinsic TLS loss is $(6.4 \pm 0.2) \times 10^{-5}$. Dielectric loss extraction is used to determine a lower bound of the intrinsic TLS loss of the trilayer of 7.2×10^{-5}. The unusually high power-independent loss is attributed to GaAs's intrinsic piezoelectricity.

Published under license by AIP Publishing. https://doi.org/10.1063/5.0029855

I. INTRODUCTION

The investigation of the electrical properties of dielectric materials and interfaces in the millikelvin-temperature and single-photon-power regime is a burgeoning field in superconducting microwave circuits and is critical to performance enhancement in superconducting quantum computing.[1] In particular, epitaxially grown dielectrics are of interest because crystalline materials with low defect density have the potential to exhibit lower two-level-state (TLS) loss,[2,3] the dominant form of loss in high-performance superconducting quantum circuits.[1,4] In addition, the ultrahigh vacuum environment used in epitaxial growth allows for lower TLS loss attributed to cleaner interfaces between materials.[5,6]
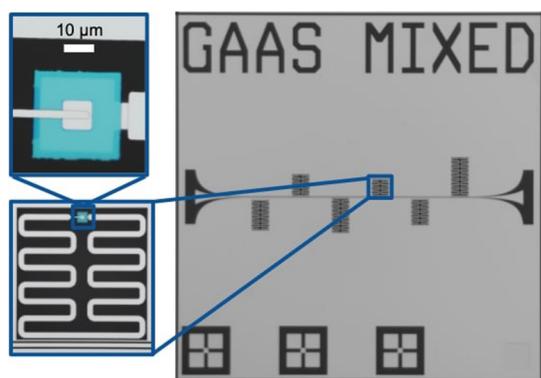
The discovery of a low-loss superconductor/dielectric/superconductor trilayer would allow the implementation of scalable, high-performance quantum computing designs such as the merged-element transmon.[7]

Because the epitaxial growth of GaAs and Al/GaAs heterostructures is well-established,[8–11] GaAs is a natural candidate for epitaxial growth for superconducting quantum devices.

In this work, we measure the power-independent loss and TLS loss of epi-Al/GaAs/Al trilayers on Al_2O_3 made using a wafer bonding technique.[12] To determine this loss, we perform cryogenic microwave measurements of lumped element superconducting microwave resonators with parallel plate capacitors formed from these trilayers. We demonstrate that these epitaxial films perform similarly to bulk GaAs[13] in both high- and low-power regimes and exhibit loss dominated by the power-independent loss which we attribute to the intrinsic piezoelectricity of GaAs.

II. DEVICE DESIGN AND FABRICATION

The material under test is a 40 nm epi-Al/40 nm epi-GaAs/ 40 nm epi-Al trilayer with a 20 nm atomic-layer-deposited (ALD) Al_2O_3 bonding layer, bonded to an $Al_2O_3(0001)$ substrate. The interfaces are abrupt and epitaxial, and the GaAs is single crystalline as determined by transmission electron microscopy (TEM).[12] More details on the growth, wafer bonding, substrate removal, and regrowth processes, as well as materials imaging and characterization, can be found in Ref. 12. Trilayer lumped element resonators

FIG. 1. Optical micrographs of a lumped element resonator with an Al/GaAs/Al parallel plate capacitor and a liftoff Al inductor. Blue region is GaAs, light gray is Al, and dark gray is the sapphire substrate. Blue squares show a zoom-in of the trilayer resonator with an inductor design of $N = 7$ (seven inductor meanders). Chip shown is sample trilayer 1, with a zoom-in of device A, as in Table I.
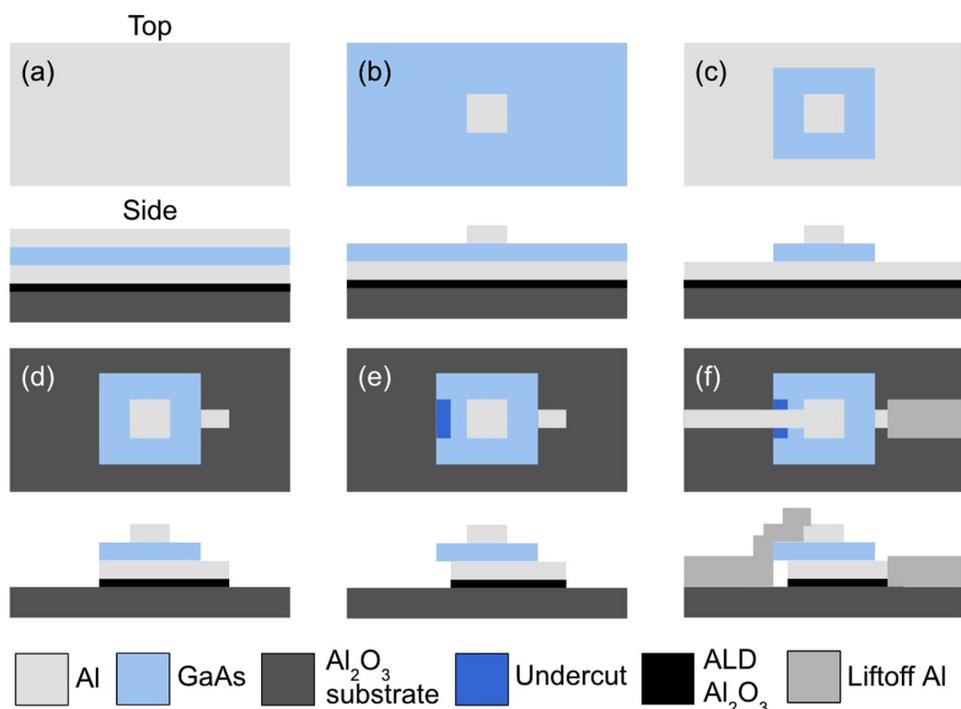
(shown in Fig. 1) are patterned using a six-step lithography and etch process (Fig. 2). First, the top capacitor plate is defined using a Megaposit MF26A developer[14] to etch the top layer of Al [Fig. 2(b)]. Then, the GaAs is etched away with Transene GA300 wet etchant heated to 33 °C [Fig. 2(c)]. A second MF26A etch is used to remove the next layer of Al as well as the AlO$_x$ bonding layer [Fig. 2(d)]. An undercut of the bottom capacitor plate is

performed with Transene D Al Etchant [Fig. 2(e)]. Transene A Al Etchant is used to fully remove residual Al in large blank areas. Finally, a liftoff process of e-beam deposited Al is used to form the feedline and inductors [Fig. 2(f)]. Auto-spun Megaposit SPR660 photoresist exposed using a maskless aligner is used for lithography in all but the liftoff step, where a trilayer of MicroChem PMMA A2, MicroChem LOR5A, and SPR660 is used. An oxygen plasma ash is used to prepare the surface prior to Al deposition.

The trilayer resonator design is similar to that in Ref. 15. The parallel plate capacitor is designed to have a $10 \times 10\,\mu m^2$ top plate and is connected to each end of the inductor by liftoff. The inductor is $15\,\mu m$ in width with a gap between inductive meanders of $30\,\mu m$ and inductor length varies by varying the number of meanders N between 7 and 17, corresponding to resonance frequencies f_0 between 4.7 and 7.5 GHz. Coupling quality factors vary between roughly 10 000 and 100 000 in order to facilitate critical coupling.

About 17% of the total Al top electrode area is liftoff Al, not epi-Al. This could obscure the epi-Al/GaAs/Al loss if trilayer loss is much lower than the liftoff interface loss. In addition, the capacitor undercut has an estimated participation of 6% based on the capacitance of that region. In future experiments, the undercut connection will be replaced by an airbridge in order to increase the measurement sensitivity to the trilayer loss.

In order to take into account the effect of the inductor circuit element, trilayer resonator measurements are compared to those of planar resonators, for which the same inductor design is used but the trilayer is replaced by an interdigitated capacitor. Planar resonators are fabricated using liftoff e-beam Al on sapphire to imitate the inductor fabrication in the trilayer devices.

FIG. 2. Diagram of the fabrication process for epi-Al/GaAs/Al trilayer lumped element resonators, with top and side views of the capacitor. (a) shows trilayer prior to processing. Fabrication steps shown are (b) capacitor top plate definition, (c) GaAs layer etch, (d) bottom Al layer etch, (e) undercut, and (f) Al liftoff.

III. MICROWAVE MEASUREMENTS AND LOSS EXTRACTION

Samples are clamped into sample boxes made from gold-plated oxygen-free high thermal conductivity copper, with wire-bonds used for electrical connection. Measurements are performed in two different cryogen-free dilution refrigerators (DRs): DR1, at a temperature of 12 mK, and DR2, at a temperature below 10 mK. Applied power is varied between −5 and −90 dBm with roughly 70 dB of line attenuation.

Internal quality factors Q_i, coupling quality factors Q_c, and resonance frequencies f_0 are determined by way of a fitting routine that implements the diameter correction method,[16] with a fixed-f_0 Monte Carlo fit, ten points on either side of the resonance frequency used for normalization, and one 3-dB bandwidth of data around the resonance used for the fitting itself. Resonator data, as well as measurement and fitting codes, can be found online.[17]

Four trilayer resonators and one planar resonator were successfully measured, as shown in Table I, and two were able to be fitted at sufficiently high and low powers as to allow TLS model fitting.[18] These two devices are labeled device A (trilayer resonator) and device B (planar resonator). Measurements of the other trilayer resonators in Table I support the values seen in the measurements of device A. Although inductors in devices A and B are identical, resonance frequencies f_0 and coupled quality factors Q_c of the two devices differ slightly due to the different capacitances of the trilayer and the interdigitated capacitor.

Figure 3 shows power sweeps of loss $\delta = 1/Q_i$ for resonators A and B as well as fits to the total loss model

$$\delta = \delta_{TLS}(T, \langle n_{\rm ph} \rangle) + \delta_{\rm other}(T), \tag{1}$$

where δ_{TLS} is TLS loss as defined in the following equation and varies with temperature T as well as time-averaged number of photons in the resonator $\langle n_{\rm ph} \rangle$, and $\delta_{\rm other}$ is a sum of power-independent losses such as quasiparticle loss, vortex loss, and piezoelectric loss.[13] The TLS model is given by[18,19]

$$\delta_{TLS} = F\delta_{TLS}^0 \frac{\tanh\left(\frac{\hbar\omega}{2k_B T}\right)}{\left(1 + \frac{\langle n_{\rm ph} \rangle}{n_c}\right)^\beta}, \tag{2}$$

where δ_{TLS}^0 is the intrinsic TLS loss, n_c is the resonator's critical

photon number, β is an exponential constant describing the homogeneity of the TLS population, and F is the filling factor of the TLS material. The resonator-induced intrinsic TLS loss, $F\delta_{TLS}^0$, is the effective loss due to TLS in the low-power, low-temperature limit. TLS model fitting results for Fig. 3 are reported in Table I. $\langle n_{\rm ph} \rangle$ is estimated using the resonator Q_c, Q_i, and f_0, and total power, as in Ref. 19.

At high power, where TLS is saturated and power-independent losses dominate, $\delta = 1/Q_{i,HP} \sim \delta_{other}$, where $1/Q_{i,HP}$ is the inverse high-power internal quality factor. In this regime, the loss of tri-layer resonator A is $(4.8 \pm 0.1) \times 10^{-5}$. This value is only a factor of two different than the loss at low powers [Fig. 3(a)], demonstrating that power-independent loss sources dominate the total loss of this device. Indeed, this high-power loss is more than an order of magnitude higher than expected, as shown by comparison to a power sweep of resonator B [Fig. 3(b)], which does not contain an Al/GaAs/Al trilayer. This unusually high loss in the high-power regime is demonstrated repeatably with four trilayer devices on two chips across multiple cooldowns, as shown in Table I.

The high-power loss in this work is within a factor of three of the piezoelectric loss measured in bulk GaAs.[13] We believe that this unusually high high-power loss can also be attributed to piezoelectricity. Quasiparticle and vortex loss are unlikely to vary so significantly between samples measured using the same experimental setup, such as resonators A and B. Another possible materials loss that would present at high power is loss due to interdiffusion between the Al and GaAs epitaxial layers. This can be ruled out by interface TEM images in Ref. 12 that show these interfaces as abrupt and epitaxial.
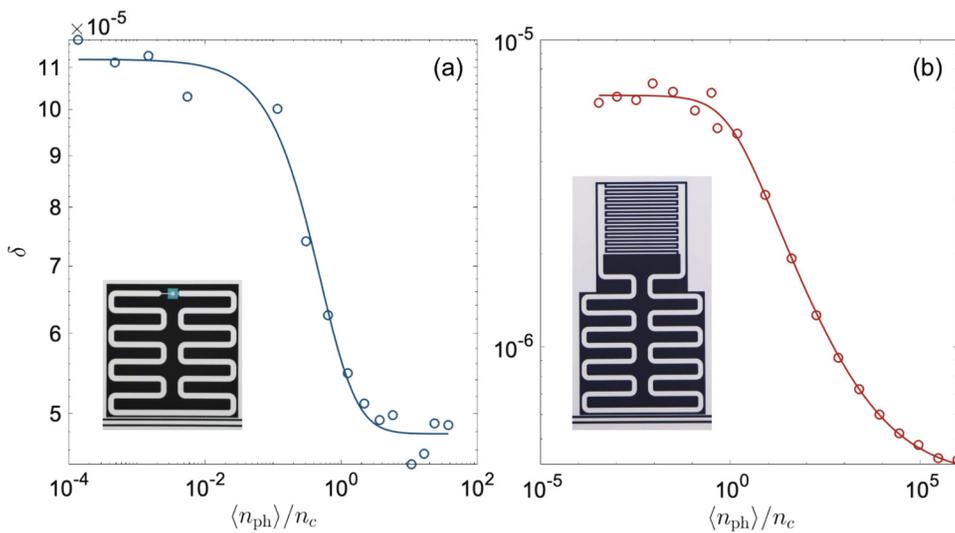
The resonator-induced intrinsic TLS loss in resonator A is $(6.4 \pm 0.2) \times 10^{-5}$. We can determine a lower bound for the intrinsic TLS loss of the Al/GaAs/Al trilayer, independent of the effect of the resonator wiring, by implementing a modified version of dielectric loss extraction.[15] Details on the simulations used can be found in the supplementary material of Ref. 15. The resonator-induced intrinsic TLS loss in device A, $\delta_A = F_A \delta_{TLS,A}^0$, where F_A is the filling factor of the TLS material in device A, is a weighted sum of intrinsic TLS loss in the planar inductor δ_L and the Al/GaAs/Al trilayer capacitor $\delta_{\rm Al/GaAs/Al}$, which is given as

$$\delta_A = \frac{C_L}{C_{\rm tot}}\delta_L + \frac{C_C}{C_{\rm tot}}\delta_{\rm Al/GaAs/Al}, \tag{3}$$

TABLE I. Parameters extracted from cryogenic microwave measurements of lumped element resonators with Al/GaAs/Al parallel plate capacitors (trilayer) and interdigitated capacitors (planar). All measurements were performed in DR1 unless stated otherwise. Values are given with their 95% confidence intervals where available. N: number of inductor meanders; f_0: resonance frequency; $1/Q_{i,HP}$: inverse high-power internal quality factor; $F\delta_{TLS}^0$: resonator-induced intrinsic TLS loss; $1/Q_{i,LP}$: inverse low-power internal quality factor (this value is reported if $F\delta_{TLS}^0$ is unavailable); $1/Q_c$: inverse coupling quality factor. Resonator A (B) TLS fit determined the critical number of photons $n_c = 50\,000$ (70 000) and exponential constant $\beta = 3$ (0.37).

Device label	Sample	N	f_0 (GHz)	$1/Q_{i,HP}$ ($\times 10^{-6}$)	$F\delta_{TLS}^0$ ($\times 10^{-6}$)	$1/Q_{i,LP}$ ($\times 10^{-6}$)	$1/Q_c$ ($\times 10^{-6}$)
A	Trilayer 1	7	7.41	48 ± 1	64 ± 2	…	15.3
B	Planar 1	7	7.92	0.3 ± 0.1	6.2 ± 0.2	…	2.6
…	Trilayer 1 DR2	17	4.79	57.8	~18.3	…	23.6
…	Trilayer 1	9	6.39	108	…	~217	17
…	Trilayer 2	7	7.41	92.6	…	~110	163

FIG. 3. Loss δ as a function of normalized number of photons in the resonator $\langle n_{ph} \rangle / n_c$ at $T \sim 12$ mK for resonators (a) A and (b) B, defined in Table I. Data are denoted as circles, and fitting to the total loss model in Eq. (1) is denoted as a solid line. Insets show representations of the measured devices.

where C_L (C_C) is the capacitance of the inductor (capacitor) circuit component, and the total capacitance is $C_{tot} = C_L + C_C$. If we assume all TLS loss in planar resonator B is from the inductor, which is identical in design to the inductor in device A, then $\delta_B = \delta_L$. We can then determine a lower bound on the loss of the epitaxial Al/GaAs/Al trilayer by

$$\delta_{Al/GaAs/Al} = \frac{C_{tot}}{C_C} \left(\delta_A - \frac{C_L}{C_{tot}} \delta_B \right) \qquad (4)$$

with trilayer capacitance $C_C = 285$ fF and inductor capacitance $C_L = 37.5$ fF, as determined by analysis and simulation, and loss values shown in Table I. For a parallel plate capacitor, $F = 1$, so we can say $\delta_{Al/GaAs/Al} = \delta^0_{TLS,Al/GaAs/Al}$.

From Eq. (4), we determine that $\delta_{Al/GaAs/Al} = 7.2 \times 10^{-5}$, slightly higher than the resonator-induced TLS loss for device A, $\delta_A = (6.4 \pm 0.2) \times 10^{-5}$, verifying that the TLS loss of device A is dominated by the Al/GaAs/Al trilayer. This value includes the loss of the undercut region, the liftoff Al on the capacitor, and capacitor edge effects, which could increase the effective loss. Even so, these values agree within a factor of two with bulk GaAs TLS loss measurements.[13]

For a target qubit lifetime of 50–100 μs, losses must fall within the mid-10^{-7} range. Thus, the measured loss in this materials set in both the high- and low-power regimes is too high for superconducting qubit applications. However, power-independent and TLS losses may be lower in other similar epitaxial trilayers such as Al/Si/Al and Al/Ge/Al, which will be explored in future work.

IV. CONCLUSION AND NEXT STEPS

Due to the presence of a significant power-independent loss in thin epitaxial Al/GaAs/Al trilayers, GaAs can be ruled out as a promising dielectric material for superconducting quantum computing applications unless mitigation methods are implemented. In the future, similar growth, fabrication, and measurement techniques could be applied to other promising, non-piezoelectric materials sets such as epi-Al/Si/Al trilayers and could yield substantial performance enhancement.

In future materials measurements of this type, the replacement of the undercut connection with an airbridge could reduce loss from this region and increase measurement sensitivity. In addition, the variation of capacitor size and thickness could allow the extraction of losses for individual regions within the capacitor such as the superconductor/dielectric interfaces and the superconductor and dielectric surfaces.

DATA AVAILABILITY

The data that support the findings of this study are openly available in Boulder-Cryogenic-Quantum-Testbed/data at http://doi.org/10.5281/zenodo.4025406, Ref. 20.

REFERENCES

[1]C. R. H. McRae, H. Wang, J. Gao, M. Vissers, T. Brecht, A. Dunsworth, D. Pappas, and J. Mutus, Rev. Sci. **91**(9), 091101 (2020).
[2]S. Oh, K. Cicak, R. McDermott, K. B. Cooper, K. D. Osborn, R. W. Simmonds, M. Steffen, J. M. Martinis, and D. P. Pappas, Supercond. Sci. Technol. **18**, 1396 (2005).
[3]Y. Nakamura, H. Terai, K. Inomata, T. Yamamoto, W. Qiu, and Z. Wang, Appl. Phys. Lett. **99**, 212502 (2011).
[4]C. Müller, J. H. Cole, and J. Lisenfeld, Rep. Prog. Phys. **82**, 124501 (2019).
[5]A. Megrant, C. Neill, R. Barends, B. Chiaro, Y. Chen, L. Feigl, J. Kelly, E. Lucero, M. Mariantoni, P. J. O'Malley *et al.*, Appl. Phys. Lett. **100**, 113510 (2012).
[6]C. J. Richardson, N. P. Siwak, J. Hackley, Z. K. Keane, J. E. Robinson, B. Arey, I. Arslan, and B. S. Palmer, Supercond. Sci. Technol. **29**, 064003 (2016).

[7]R. Zhao, S. Park, T. Zhao, M. Bal, C. McRae, J. Long, and D. Pappas, Phys. Rev. Appl. 14, 064006 (2020).

[8]A. Y. Cho and P. D. Dernier, J. Appl. Phys. 49, 3328 (1978).

[9]P. M. Petroff, L. C. Feldman, A. Y. Cho, and R. S. Williams, J. Appl. Phys. 52, 7317 (1981).

[10]R. Ludeke and G. Landgren, J. Vac. Sci. Technol. 19, 667 (1981).

[11]S. Pilkington and M. Missous, J. Cryst. Growth 196, 1 (1999).

[12]A. P. McFadden, A. Goswami, M. Seas, C. R. H. McRae, R. Zhao, D. P. Pappas, and C. J. Palmstrøm, J. Appl. Phys. 128, 115301 (2020).

[13]M. Scigliuzzo, L. E. Bruhat, A. Bengtsson, J. Burnett, A. F. Roudsari, and P. Delsing, New J. Phys. 22, 053027 (2020).

[14]Certain commercial equipment, instruments, and materials are identified in this paper to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

[15]C. R. H. McRae, R. E. Lake, J. L. Long, M. Bal, X. Wu, B. Jugdersuren, T. H. Metcalf, X. Liu, and D. P. Pappas, Appl. Phys. Lett. 116, 194003 (2020).

[16]M. Khalil, M. Stoutimore, F. Wellstood, and K. Osborn, J. Appl. Phys. 111, 054510 (2012).

[17]See https://github.com/Boulder-Cryogenic-Quantum-Testbed/ for data acquisition, preprocessing, and data fitting software used in this work.

[18]D. P. Pappas, M. R. Vissers, D. S. Wisbey, J. S. Kline, and J. Gao, IEEE Trans. Appl. Supercond. 21, 871 (2011).

[19]J. Burnett, A. Bengtsson, D. Niepce, and J. Bylander, IOP Conf. Ser. J. Phys. Conf. Ser. 969, 012131 (2018).

[20]C. R. McRae, "Boulder-Cryogenic-Quantum-Testbed/data: Data for Dielectric loss in epitaxial Al/GaAs/Al trilayers for superconducting circuits," Zenodo, Dataset: https://doi.org/10.5281/zenodo.4025406.