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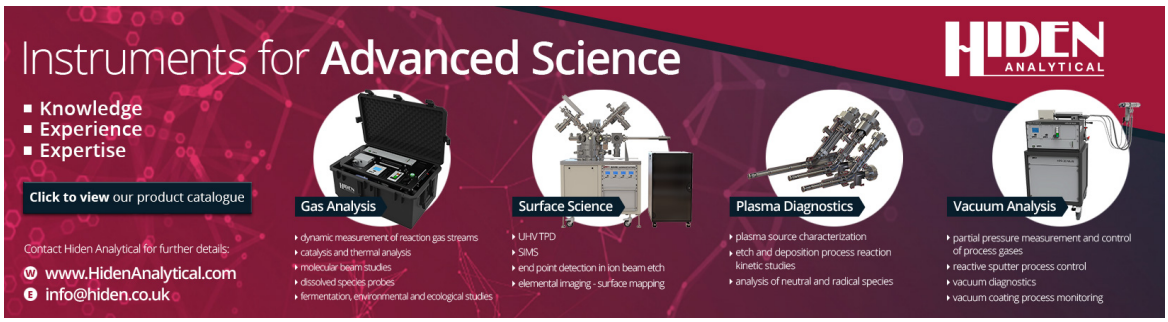

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ABSTRACT

Epitaxial Al/GaAs/Al structures having controlled thickness of high-quality GaAs and pristine interfaces have been fabricated using a wafer-bonding technique. III–V semiconductor/Al structures are grown by molecular beam epitaxy on III–V semiconductor substrates and bonded to silicon and sapphire. Selective etching is used to remove the III–V substrate followed by surface cleaning and superconductor regrowth, resulting in epitaxial Al/GaAs/Al tri-layers on sapphire or silicon substrates. Structures are characterized with reflection high energy electron diffraction, atomic force microscopy, x-ray photoelectron spectroscopy, transmission electron microscopy, and x-ray diffraction. Applications of these structures to the field of quantum information processing are discussed.

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I. INTRODUCTION

Superconductor heterostructures are playing an important role in the rapidly developing field of quantum information processing. Superconducting qubits utilize superconducting circuit elements and Josephson junctions (JJs), which are made using nanofabrication techniques to store information.[1,2] Transmon qubits, which consist of capacitively shunted JJs, are made using a variety of superconductors typically deposited on low-loss substrates such as silicon and sapphire. Voltage-tunable "gatemon" qubit structures have been demonstrated using Josephson junctions consisting of superconducting aluminum contacts to high mobility InAs nanowires[3] and 2D electron gases.[4] In reports exploring topological superconductivity motivated by topological quantum computation, high mobility III–V materials with spin–orbit interaction are integrated with superconductors (most commonly aluminum) in fabricated mesoscopic structures consisting of semiconducting channels, superconducting contacts, and gates.[5–7]

In all of the above-mentioned applications, the observed physics and device properties have been shown to be quite sensitive to the superconductor–semiconductor interface. Mechanisms of loss and decoherence in superconducting qubits have been studied extensively,[8–11] and it has been shown that material imperfections at superconductor interfaces can be the dominant source of loss.[10] As a result, large planar capacitors are commonly used in transmon circuits to dilute surface and interface loss which increase coherence at the cost of scalability.[12] In mesoscopic superconductor–semiconductor structures employed to study topological superconductivity, a so called "hard" induced superconducting gap has been shown to be a requirement for topological protection of the proposed topological qubits.[13,14] These hard induced gaps have only been observed when the superconductor/semiconductor interface is clean and free of oxides.[15,16]

Epitaxial JJ structures are of particular interest in the field of superconducting qubits where the Al/AlO_x/Al JJ elements used in state-of-the-art transmons contain a high density of structural and chemical inhomogeneities,[17,18] which contribute to loss and decoherence. High-quality superconductor/dielectric/superconductor tri-layers could replace the JJ and capacitor elements currently used in transmon designs, improving scalability, and coherence. Transmons could even be made from a single superconductor/dielectric/superconductor tri-layer having the appropriate dimensions with a single

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structure serving as both the capacitor and the Josephson junction,[19] if the loss associated with the dielectric and interfaces could be made low enough, a challenge that has not yet been overcome. Conventional semiconductors could be an excellent candidate for this application, owing to their well understood and tunable properties including bandgap energy and lattice constant.

Growth of many superconductors on semiconductors including Al-on-GaAs[20–23] and Al-on-Si[24,25] is well established. However, growth of high-quality single-crystal semiconductors such as Si and III–V's on conventional elemental superconductors such as Al is likely not possible due to concerns such as symmetry mismatch and reactions and roughening that occur at the high growth temperature required for the semiconductor. Yan *et al.*[26] succeeded in growth of high-quality nitride-based semiconductor structures on superconducting NbN, but the authors used thick AlN/GaN buffer layers grown on the NbN and did not address the problem of moving to thin semiconductor layers required for tunneling junctions. Because of the challenges of materials integration, single-crystal semiconductor based tunnel junctions have not been fabricated by direct growth of semiconductors on superconductors, though several other techniques have been used to create tunneling junctions using semiconductors.

JJ structures using amorphous Si[27,28] and Ge[29] have been successfully fabricated and studied; however, the semiconductors are amorphous, which limits their usefulness for superconducting qubit technology due to loss associated with the structural and bonding disorder. Van Huffelen *et al.*[30] have studied transport in Nb/Si/Nb JJ's with single-crystal degenerately doped p-Si layers. These structures were fabricated using a backside selective etch to form a thin membrane, which was subsequently coated with Nb on both sides. Because of the fabrication technique, the thickness of the Si layers could not be precisely controlled in contrast to direct growth techniques, and high Boron doping was required to obtain etch selectivity.

Magnetic tunnel junctions (MTJs) having single-crystal GaAs tunneling barriers were fabricated by Kreuzer *et al.*[31,32] In these studies, an adhesive wafer-bonding technique was used to obtain pinhole free tunnel junctions with single-crystal GaAs barriers and poly-crystalline Fe electrodes. Performance of the Fe/GaAs/Fe MTJs was limited by the imperfect magnetic structure at the Fe/GaAs interfaces due to reactions that occur between Fe and GaAs.[32,33] Direct wafer bonding of III–V wafers to silicon without the use of epoxies has also been accomplished, especially in the field of silicon photonics.[34] Veractor diodes fabricated on silicon using a wafer-bonding and III–V substrate removal technique have shown similar performance to diodes on their native III–V substrate.[35]

In this work, a novel wafer bonding and aluminum regrowth process is presented for fabrication of epitaxial Al/GaAs/Al tri-layer structures. These structures have been made with arbitrary GaAs thickness and are shown to be structurally homogeneous with clean, atomically sharp interfaces. Though GaAs was the only semiconductor used in this study owing to the ease of materials growth and established selective etches, it is expected that much of the presented process may be extended to other semiconductors including other III–V's and Si as well as semiconductor heterostructures.

II. PROCESS OVERVIEW

The novel process used to fabricate epitaxial Al/GaAs/Al tri-layers is outlined in Fig. 1. GaAs/AlGaAs structures grown by MBE are capped with epitaxial Al and removed from vacuum. A wafer bonding process is used to bond the III–V/Al stack to either Si

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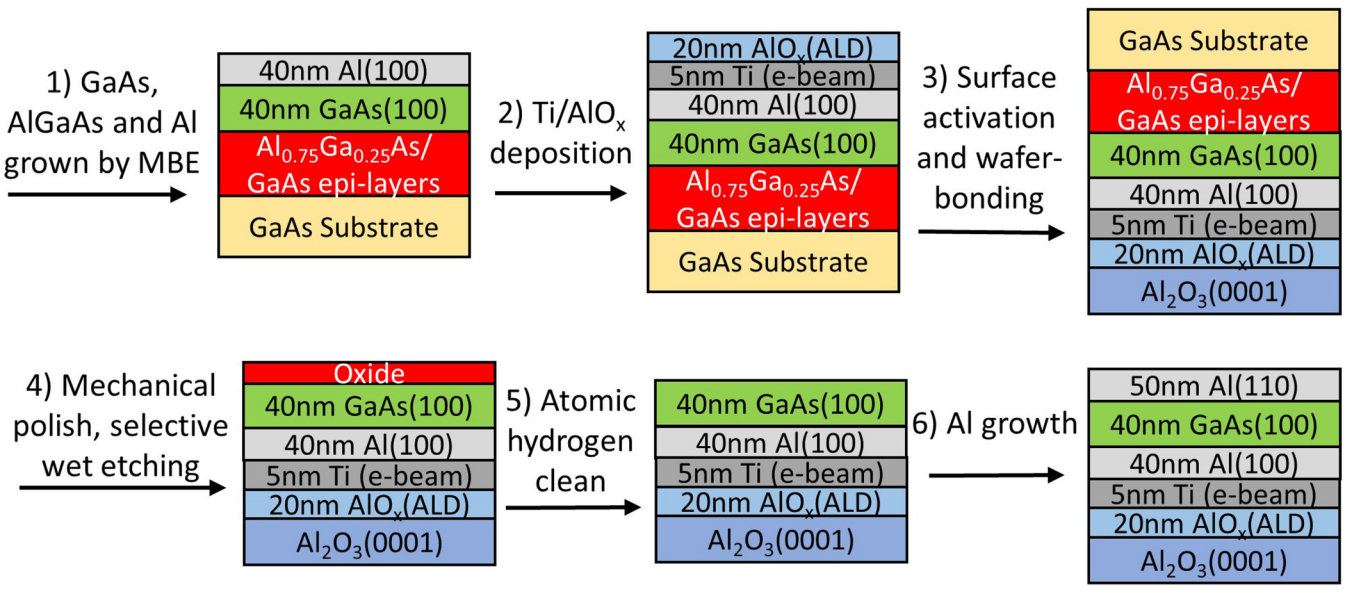

FIG. 1. Overview of the Al/GaAs/Al tri-layer process flow.

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(100) or Al_2O_3(0001) after which the GaAs(100) substrate is removed using selective wet etching. Following removal of the final AlGaAs protective layer, samples are loaded back into ultrahigh vacuum, the surface oxide is removed using an atomic hydrogen cleaning procedure, and epi-Al is regrown resulting in the complete Al/GaAs/Al tri-layer structure.

III. MATERIALS GROWTH

A Veeco Gen3 III–V MBE system was used for both III-V semiconductor and aluminum (superconductor) growth. Semi-insulating, epi-ready 50.8 mm (2-in.) diameter GaAs(001) substrates were baked at 200 °C in a high vacuum loadlock before outgassing at 350 °C in an ultrahigh vacuum (UHV) preparation chamber. Outgassed substrates were loaded in to the MBE chamber followed by native oxide desorption at 600 °C in an As_2 overpressure. GaAs/AlGaAs "double-etch-stop" structures were grown at 580 °C having the layer structure: GaAs(40 nm)/$Al_{0.75}Ga_{0.25}As$(50 nm)/GaAs (250 nm)/$Al_{0.75}Ga_{0.25}As$(200 nm)/GaAs(500 nm)/GaAs(001) substrate. Following III-V semiconductor growth, samples were cooled to below 350 °C in an As_2 overpressure. Upon cooling, the surface reconstruction observed by reflection high energy electron diffraction (RHEED) changed from a $(2 \times 4)/c(2 \times 8)$ observed during and immediately after growth to the expected As-rich $c(4 \times 4)$ surface reconstruction. Once the sample was cooled, the arsenic valve was closed, the sample was removed from the MBE chamber, and was further cooled to room temperature in the UHV prep chamber for a duration of at least 10 h.

After cooling to room temperature, samples were loaded back in to the MBE growth chamber for epitaxial aluminum growth. Previous reports have shown that the orientation of Al thin films grown on GaAs(100) can be controlled using the GaAs surface termination, growth rate, and growth temperature.[20–23] When the substrate is kept at room temperature, Al grows predominantly in the (110) orientation on As-rich GaAs(100) and in the (100) orientation on the Ga-rich GaAs(100) surface. These results were repeated using the system employed for this study on separate calibration samples, which were studied with x-ray diffraction (XRD) and atomic force microscopy (AFM).

The wafer-bonding procedure used to complete the tri-layer process is very sensitive to surface roughness and therefore minimizing surface roughness of the epi-Al layer is required. The lowest surface roughness (RMS roughness below 1 nm in a 1 μm square scan window) was observed for Al(100) grown on the Ga-rich GaAs(100) surface, which was used for the remainder of the process for that reason. An As-rich GaAs(100) surface can be transformed to Ga-rich by either reducing the As-flux during growth or by annealing in the absence of, or in a reduced As overpressure. The surface reconstruction may be monitored by RHEED with the Ga-rich surface indicated by a $c(8 \times 2)$ or (4×6) surface reconstruction.[36,37]

While obtaining a Ga-rich surface near growth temperature is straightforward, it was found that maintaining this Ga-rich surface while cooling the sample to below 350 °C was difficult to reproduce due to residual arsenic partial pressure immediately following MBE growth. In order to achieve the required reproducibility, samples were cooled to room temperature with the As-rich $c(4 \times 4)$ reconstruction as was described previously. 2 ML of Ga was deposited on the $c(4 \times 4)$ surface at room temperature and the RHEED was observed to transform to a (1×1) or unreconstructed surface. 50 nm of Al was immediately grown on this surface at a rate of 0.8 Å/s. RHEED observed during Al growth showed that the first few nm were rough indicated by a spotty RHEED pattern which became streakier as the growth progressed. A fourfold symmetric RHEED pattern consistent with Al(100) was observed throughout the Al growth which was confirmed by XRD. The evolution of the RHEED patterns during this procedure is included as Fig. 2.

IV. WAFER BONDING AND SUBSTRATE REMOVAL

After Al growth, samples were removed from vacuum, coated with a layer of photoresist, which is used to protect the wafer surface from particles, and cleaved into quarters of the original 50.8 mm (2-in.) diameter wafers. The remaining procedure was carried out using these quarter wafers in order to conserve material while still having adequate material area for device preparation. Photoresist was then stripped in acetone, rinsed with isopropanol (ACE/ISO), a thin 5 nm Ti layer was deposited by e-beam evaporation to serve as an adhesion layer, and 20 nm of aluminum oxide (AlO_x) was deposited by atomic layer deposition (ALD) using trimethylaluminum (TMA) and H_2O at a substrate temperature of 300 °C. After AlO_x deposition, samples were again cleaned in acetone along with a 76.2 mm (3-in.) diameter as-received Al_2O_3(0001) wafer for bonding. After rinsing in isopropanol, both the AlO_x/Al/GaAs sample and the sapphire bonding wafer were immediately loaded into an EVG 810 plasma activation tool. After pumping down, the wafers were exposed to an O_2 plasma for 30 s to activate the surface.

Following the surface activation process, samples were exposed to atmosphere, the surfaces were immediately brought into contact, and pressed together using graphite clamping fixtures. Pressure was administered by applying a calibrated torque to nuts on the press fixture resulting in an approximate pressure of 200 kPa. The press fixtures containing the samples were then loaded into an air oven held at 300 °C for a period of about 12 h to complete the wafer-bonding process. With the exception of the Ti and AlO_x coating layers, this wafer-bonding procedure is very similar to the low temperature plasma assisted bonding procedure used for InP/Si direct bonding, which is discussed in more detail by Pasquariello and Hjart.[38]

After wafer bonding was completed, the GaAs(100) substrates were mechanically thinned prior to selective wet etching. The sapphire bonding wafer was attached to a polishing fixture using wax followed by mechanical polishing using 600 grit sandpaper with isopropanol as a lubricant. The GaAs substrate was thinned using this technique from the initial wafer thickness of 350 μm to approximately 150 μm. After mechanical polishing, the sample was removed from the polishing fixture and cleaned with ultrasonic agitation in acetone in two steps to remove the adhesive and particles created during the mechanical thinning. The GaAs substrate was then removed completely using H_2O_2:NH_4OH, which can be a highly selective etchant of GaAs with respect to AlGaAs.[39]

A three-step etching procedure was used with varying ratios of H_2O_2:NH_4OH starting with 12:1 for 15 min followed by 30:1 for approximately 20 min longer until the GaAs substrate was

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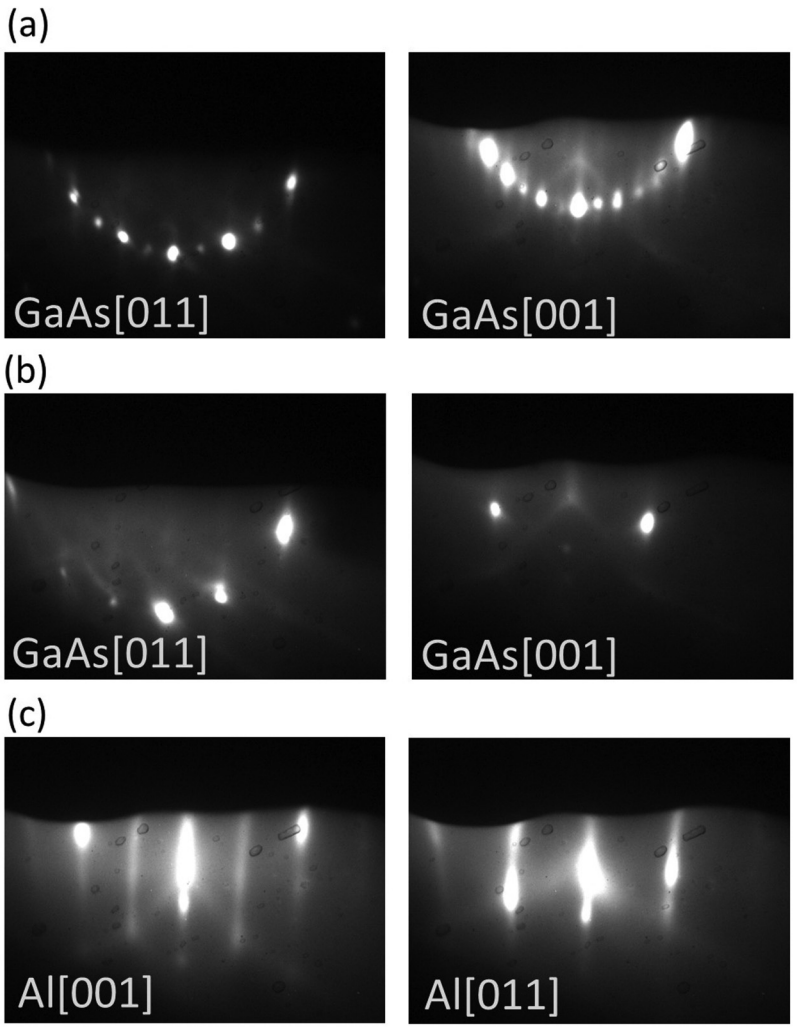

FIG. 2. Evolution of RHEED patterns observed during Al growth. (a) c(4 × 4) reconstructed GaAs at room temperature. (b) The same surface following deposition of 2 ML Ga. (c) 40 nm Al(100) deposited on the surface shown in (b) with the expected epitaxial relationship Al[001]||GaAs[011]. The direction of the RHEED beam is indicated in each image.

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entirely removed revealing the first 200 nm thick AlGaAs etch stop layer as indicated by a shiny surface. After the GaAs substrate was removed, the sample was transferred to a third H_2O_2:NH_4OH solution having concentration 40:1 for 5 min to remove the residual GaAs substrate not visible by eye. A stir bar was used in all of the etchant solutions, and the wafer placement in the beakers ensured that solution was constantly flowing over the entire wafer surface. The three-step etch was found to result in a more reproducible procedure.

Once the substrate was removed, the remaining MBE grown etch stop layers were selectively removed. Buffered HF (BHF) is a highly selective etch of $Al_xGa_{1-x}As$ with respect to GaAs for $x > 0.7$[40] and was used to remove the $Al_{0.75}Ga_{0.25}As$ layers. Following removal of the first 200 nm thick AlGaAs layer, the 250 nm GaAs etch stop was removed using a 10:1 1M $C_6H_8O_7$:H_2O_2 solution, which is another known selective etchant for GaAs with respect to AlGaAs.[40] The citric acid solution was chosen over the H_2O_2:NH_4OH solution used to selectively remove the GaAs substrate as it was found to be more controllable for removal of thin GaAs films. The final AlGaAs etch stop layer was then removed using BHF, and the sample was immediately loaded in to the MBE growth system for surface cleaning and aluminum regrowth.

V. SURFACE CLEANING AND ALUMINUM REGROWTH

If both Al/GaAs interfaces in the tri-layer structure are to be pristine, the native oxide formed on the sample surface by exposure to atmosphere must be removed. The native oxide formed on the sample surfaces was removed at temperatures below 400 °C using atomic hydrogen. This low temperature process was used as opposed to thermal desorption both to protect the wafer bond and to maintain the pristine Al/GaAs interface. In order to determine appropriate conditions for native oxide removal on the GaAs surfaces resulting from the substrate removal and selective etch processes, three samples were prepared in the manner just described and loaded in to an ultrahigh vacuum (UHV) growth and

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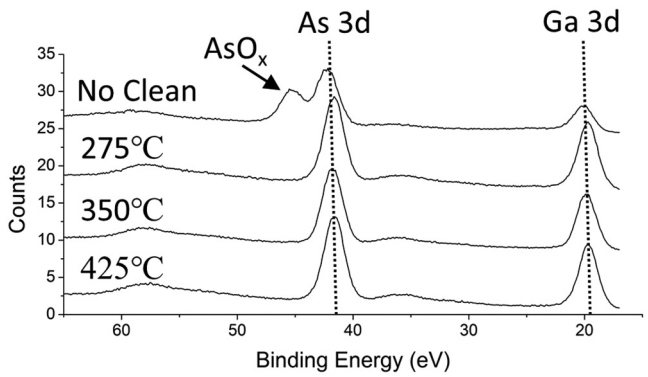

FIG. 3. XPS measurements of prepared GaAs surfaces following hydrogen cleaning at variable temperatures. The vanishing of the high binding energy shoulder on the As 3d peak indicates the reduction of the surface oxide.

characterization cluster tool equipped with atomic hydrogen cleaning, RHEED, and x-ray photoelectron spectroscopy (XPS), which was used to study the surface structure and chemistry.

RHEED and XPS measurements taken before hydrogen cleaning confirm the presence of an amorphous oxide on the surface indicated by a diffuse RHEED pattern along with the presence of a prominent oxygen 1s peak observed in XPS. After RHEED and XPS measurements, samples were sequentially exposed to an atomic hydrogen flux provided by a thermal cracker source operated at 1700 °C. The hydrogen flux was kept the same for all samples which was controlled by adjusting a leak valve to obtain a set pressure of 1e−6 Torr in a chamber having a base pressure <1e−9 Torr. Samples were cleaned for 1 h at variable temperatures of 275, 350, and 425 °C. XPS measurements taken before and after hydrogen cleaning are included as Fig. 3.

One of the potential drawbacks of using atomic hydrogen for surface cleaning is the possible incorporation of interstitial hydrogen

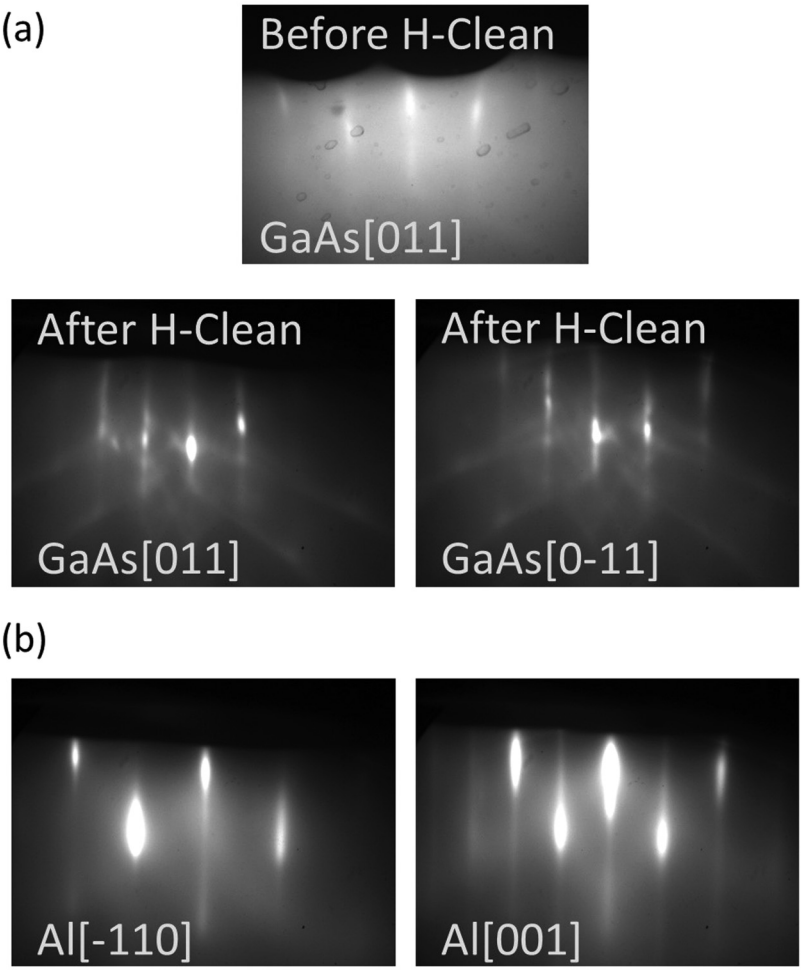

FIG. 4. (a) RHEED patterns of the wafer-bonded GaAs (100) surface before and after atomic hydrogen cleaning. (b) RHEED images taken from the same sample after growth of 50 nm (110)Al showing the expected epitaxial relationship Al[−110]||GaAs[011]. The direction of the RHEED beam is indicated in each image.

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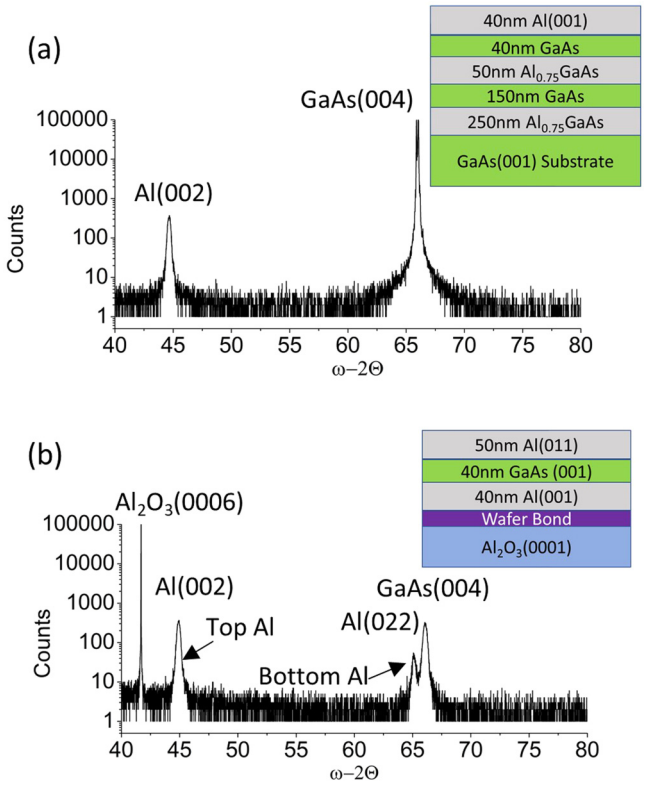

FIG. 5. XRD measurement (a) before and (b) after the wafer bonding and regrowth process along with layer schematics of the structures.

in the GaAs dielectric layer. While the effects of hydrogen incorporation on device performance are unknown, interstitial hydrogen in III–V semiconductors is known to passivate dopants and impurities.[41,42] For qubit applications, interstitial hydrogen has been shown to act as a two-level system (TLS) in sapphire,[43–45] which is detrimental to qubit performance. The amount of hydrogen incorporated from the process discussed here is unknown, but could be quantified by secondary ion mass spectroscopy (SIMS) and potentially reduced with thermal annealing.[46] A clear reduction of the O 1s (not shown) as well as the high binding energy shoulder on the As 3d XPS peaks indicates removal of surface oxides by hydrogen cleaning. Similar XPS scans were observed for all temperatures tested, which demonstrates a large substrate temperature window for oxide removal using atomic hydrogen in this case. RHEED measurements transform from a diffuse background before oxide removal to a bright and clear diffraction pattern after oxide removal indicating a single-crystal surface following hydrogen cleaning.

In order to complete the tri-layer process, samples were hydrogen cleaned at a substrate temperature near 300 °C using a hydrogen flux similar to that just described. Following hydrogen cleaning, samples were allowed to cool to room temperature for >4 h and then transferred under UHV to an MBE chamber for Al regrowth. 50 nm of Al was grown at room temperature at a rate of 0.8 Å/s, completing the Al/GaAs/Al structure. RHEED was observed before and during Al growth. RHEED of the GaAs(100) following hydrogen cleaning resulted in a (1 × 1) RHEED pattern. The twofold symmetric RHEED pattern of the Al was found to be consistent with Al(110) having a single in-plane rotational domain. RHEED images before and after Al regrowth are shown in Fig. 4.

VI. STRUCTURAL CHARACTERIZATION OF TRI-LAYERS

X-ray diffraction (XRD) was performed before and after the wafer-bonding/Al regrowth process. Data taken from a sample having a 40 nm thick GaAs layer are shown in Fig. 5. The omega-2 theta measurement taken before wafer bonding shown in Fig. 5(a) shows prominent peaks from the GaAs substrate and the AlGaAs etch stop layers and confirms that the first Al-layer is (100) oriented indicated by the presence of an (200) Al diffraction peak and the absence of any other peaks. Figure 5(b) shows the same measurement taken on the same sample after the wafer-bonding and

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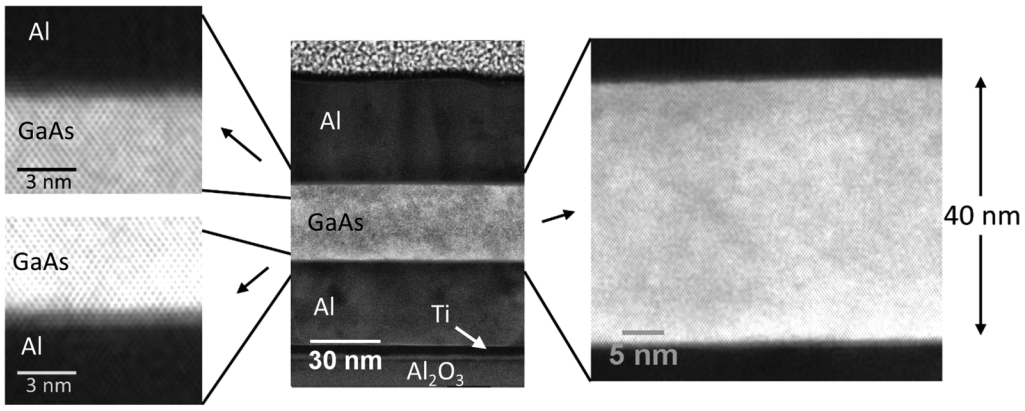

FIG. 6. TEM images of the wafer-bonded tri-layer structure and Al/GaAs interfaces. Both interfaces are abrupt and epitaxial, and the GaAs is crystalline throughout its thickness.

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Al-regrowth process. There are three prominent differences between the two measurements: the appearance of the Al_2O_3(0006) peak from the substrate that the tri-layer is bonded to, the reduction of the GaAs substrate peak to a smaller peak from the 40 nm thick GaAs layer, and the appearance of an Al(220) peak from the regrown Al epi-layer.

Cross-sectional high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) was performed on the same Al/GaAs/Al tri-layer structure having a 40 nm thick GaAs layer and images are included as Fig. 6. The images show that the GaAs layer is structurally uniform and crystalline throughout its thickness. Both Al/GaAs interfaces are observed to be abrupt and epitaxial.

AFM and optical microscopy was conducted routinely throughout the process development in order to establish the suitability of the material for device fabrication. Figure 7(a) shows that the GaAs surface following etch-stop removal and atomic hydrogen cleaning is smooth with RMS roughness below 1 nm in the 2 μm scan window shown. Figure 7(b) shows the AFM measurement of a separate sample after hydrogen cleaning and Al regrowth along with an optical Nomarski or differential interference contrast (DIC) micrograph. The optical micrograph shows large ($1 \times 1\,mm^2$) defect free regions suitable for device fabrication separated by holes in the tri-layer, which are the result of small particles present on the wafer surfaces during wafer-bonding.

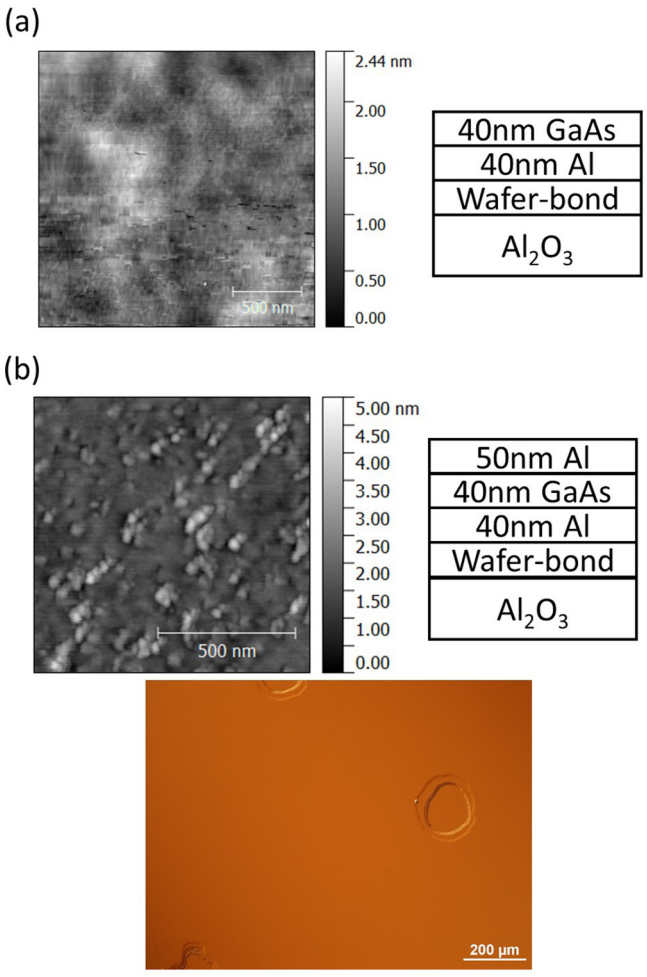

FIG. 7. (a) AFM image of the wafer-bonded structure after H-cleaning procedure showing a smooth surface. (b) AFM and optical (DIC) image of wafer-bonded tri-layer after atomic hydrogen cleaning and Al regrowth.

VII. DISCUSSION

Among the potential applications for epitaxial super/semi/super tri-layers is their use in quantum information processing applications such as employing tri-layer capacitors and Josephson junctions in transmon circuits. Epitaxial tri-layers could replace large area planar capacitors and AlO_x based JJs used in transmons, increasing scalability and coherence times, but the loss associated with the interfaces as well as the semiconductor itself need to be quite low in order to improve upon current transmon technology. This work has demonstrated that clean epitaxial interfaces may be formed which are expected to result in low loss. The loss inherent to the GaAs itself, however, is not known and the obvious next step following this work is to measure the loss tangent and transport properties of the tri-layers and JJs.

The intrinsic loss tangent of III–V semiconductors including GaAs is expected to be higher than elemental semiconductors such as Si and Ge owing to their piezoelectricity as was discussed by Casparis *et al.*[4] for InP(100) substrates and Scigliuzzo *et al.*[47] for GaAs substrates. Thus, super/semi/super tri-layers utilizing Si or Ge are expected to show superior performance for this application as compared to GaAs or other III–V materials.

Though this work has presented a process for GaAs-based tri-layers, it is expected that this process may be extended to Si-based structures. Si epi-layers could be grown on III–V substrates and etch stop layers such as the lattice matched GaP/AlGaP system. Much of the remaining process would remain the same and similar selective wet etchants may be used. One disadvantage of using III–V substrates (especially GaP) is their high cost relative to silicon or sapphire. While a complete substrate etch was presented in this paper, epitaxial liftoff (ELO), where epi-layers are etched from the native substrate leaving the reusable substrate intact, could also be employed in a similar process.[48,49]

Extending the wafer-bonding process to semiconductor heterostructures is another potential application. The voltage-tunable gatemon qubits presented by Casparis *et al.*[4] were fabricated using InAs quantum well heterostructures grown on InP(100) substrates. While the initial results are promising, the remaining qubit components such as resonators and readout cavities were deposited directly on the lossy InP substrate which limited performance. These limitations could be overcome by bonding structures to low loss substrates such as sapphire or silicon with epitaxial superconductor contacts potentially being regrown after wafer bonding.

VIII. SUMMARY

Epitaxial Al/GaAs/Al tri-layer structures have been made using a novel wafer-bonding and regrowth technique. Because the GaAs layer is initially grown on AlGaAs using standard MBE growth procedures, it is a high quality semiconductor that can be

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made with arbitrary thickness. The crystal orientation of both aluminum layers may be controlled by GaAs(100) surface termination and growth temperature, where (100), (110), and (111)Al all may be grown on GaAs(100). The presented process may be extended to other semiconductors and semiconductor heterostructures, which could be used to improve transmon and gatemon technology beyond state-of-the-art.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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