Single-Flux-Quantum Multiplier Circuits for Synthesizing Gigahertz Waveforms With Quantum-Based Accuracy

Manuel A. Castellanos-Beltran, D. I. Olaya, A. J. Sirois, C. A. Donnelly, P. D. Dresselhaus, S. P. Benz, and P. F. Hopkins

***Abstract*—We designed, simulated, and experimentally demonstrated components for a microwave-frequency digital-to-analog converter based on single flux quantum (SFQ) circuits and an amplifier based on superconducting-quantum-interference-device (SQUID) stacks. These are key components for a self-calibrated programmable waveform reference for communications metrology capable of synthesizing high-frequency signals with quantum-based output accuracy. The amplifier is an SFQ voltage multiplier circuit that consists of a network of SFQ-splitters and SQUID transformers that provides output signals consisting of quantized pulses. The circuits were fabricated using our Nb/Nb$_x$Si$_{1-x}$/Nb Josephson-junction (JJ) fabrication process, which produces self-shunted JJs with Nb-doped silicon barriers. In order to demonstrate quantum-based reproducibility, stability and performance at 4 K, we synthesized single-tone and multitone waveforms at gigahertz frequencies and demonstrated their operation over a range of synthesizer output and experimental bias parameters. We also propose circuit designs for achieving higher synthesis frequencies and higher output power with improved power accuracy and spectral purity, and discuss the potential limitations of these circuits.**

***Index Terms*—Digital-analog conversion (DAC), Josephson junctions (JJs), signal synthesis, superconducting devices, superconducting integrated circuits.**

I. Introduction

THE development of a primary standard waveform source at gigahertz and higher frequencies would provide an important calibration tool for the telecommunication industry for emerging applications, such as 5G wireless communications (see [1] and references therein). The Josephson arbitrary waveform synthesizer (JAWS) is a cryogenic superconducting digital-to-analog converter (DAC) [2] that has been developed at NIST as a programmable waveform source and primary standard for dc and ac voltage metrology with rms output amplitude of 4 V and flux-quantum-based accuracy for frequencies up to 100 kHz [3], [4]. A new implementation of JAWS, which we call RF JAWS, is being developed for synthesizing RF frequencies up to ∼5 GHz for use in a variety of applications including calibration of receiver chains, power meters, measurement electronics, and sources of single-tone and multitone amplitudes, as well as characterization of nonlinear responses in transmitter and receiver chains and measurement electronics [4]–[7]. Accurate, high-performance signals have been synthesized by the RF JAWS circuits at frequencies up to 1 MHz and rms amplitudes of 162.5 mV [8] and more recently to drive a 50 Ω load up to 1 GHz with output of −49 dBm (∼0.8 mV rms amplitude) [1].

Quantum-based, high-frequency JAWSs operating at even higher frequencies, including the millimeter-wave band (>30 GHz), are needed to provide new quantum-SI-referenced RF calibration tools for 5G communications. For example, high-purity, stable, quantum-based, and multitone signals can be used to characterize the nonlinear behavior of electronic components and circuits [5] and will allow higher resolution measurements of intermodulation distortion products. These synthesizers could be used to provide traceability in modulated signal measurements among a variety of other applications [1], [9], [10].

However, the maximum synthesis frequency of existing RF JAWS designs is limited to a few gigahertz due to clock speeds, timing issues, and low Josephson junction (JJ) switching speeds (set by the characteristic voltage I_cR_s of the JJs, where I_c and R_s are the critical current and intrinsic shunting resistance of the junctions, respectively). In order to achieve higher synthesis frequencies and to meet 5G performance needs, we are developing a single flux quantum (SFQ) JAWS based on SFQ voltage multipliers and rapid single flux quantum (RSFQ) logic circuits. RSFQ superconducting logic has been shown to process digital data at hundreds of GHz with low dynamic power dissipation [12], [13].

The development of SFQ circuits for quantum-based arbitrary waveform synthesis has been actively pursued. Most of this work has been for synthesizing dc or audio frequency ac signals [11],

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[14]–[16] although there have been a few proposed designs for generating signals at gigahertz frequencies [17], [18]. One of the most challenging parts of these systems is the design of an amplifier that preserves the quantum-based accuracy of the synthesized waveform. With JAWS and RF JAWS, this amplification is accomplished using series arrays of JJs, with each JJ generating a small voltage signal, which add together coherently across the array to create a larger voltage signal at the output of the device. The accuracy of this summation is dependent on timing, load, and array length for higher RF frequencies [1], [19], [20]. There also has been significant progress in amplifying SFQ signals, for example to generate nonreturn-to-zero data that can drive semiconductor logic, but these amplifiers do not conserve the quantized nature of the SFQ pulses [21]–[23]. Examples of quantized-pulse-conserving amplifiers are voltage multiplier circuits originally developed for dc- and audio-frequency voltage standards [15], [24]–[26]. The amplifier presented in this article is based on the AIST stacked-SQUID design with modifications to generate faster output signals [24], [25].

This article demonstrates gigahertz waveform generation using SFQ circuits. Since SFQ circuits are based on the quantization of the flux in superconductors, this system has the potential of quantum-based stability and accuracy. In Section II, we first describe the concept of the synthesizer-on-a-chip we plan to build in the future, including the on-chip cryogenic memory that will be necessary for storing the input pulse code sequence used to generate the quantized-pulse-based signal. Then in Sections III and IV, we give an overview of the experimental setup and describe measurements of the most important subcircuit of that synthesizer, the voltage multiplier stack, including measured data and error analysis of the generated signals. Results and future steps are discussed in Section V.

II. SFQ JAWS System Description

Fig. 1 shows our conceptual design for a full SFQ JAWS synthesizer-on-a-chip, operated at 4 K [27]. We use delta-sigma ($\Delta - \Sigma$) encoding based on pulse density modulation to generate the "input digital code" that defines the analog waveform, as described in [2]. This code is stored in an RSFQ-based circular shift register (CSR), which serves as the input buffer, such that the zeroes and ones of the code are represented by the presence or absence of flux quanta stored as circulating currents in various CSR cells. Using room-temperature electronics, the CSR is initially loaded at low speed with the input drive pulse sequence pattern that encodes the signal we want to generate. The stored pattern will be clocked at high speed (HF-CLK) and sent to an SFQ pulse-splitter (S) network of M stages, which multiplies each SFQ input pulse from the CSR by 2^M. The output pulses of each of the final stages of splitters are coupled to separate Josephson transmission lines (JTLs), each of which is inductively coupled to a SQUID [Fig. 2(a)]. These SQUID transformers (STs) are connected in series so that the pulses can be added together coherently. Thus, the series array of STs sum the pulses from the final stage, and the entire circuit acts as a voltage multiplier (VM) that converts each input SFQ pulse into a multiSFQ pulse with time-integrated voltage area of $2^M h/2e$, where h is the Planck constant, e is the electron charge, and $h/2e$ is the magnetic flux quantum (Φ_0).

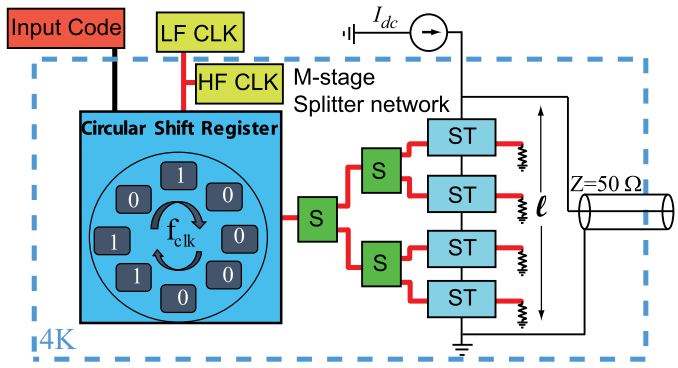

Fig. 1. Block diagram of our proposed SFQ JAWS system on a chip. We use a low-frequency room temperature clock (LF CLK) to load the encoded digital input pattern into the CSR buffer. In order to generate the high-frequency signals, an on-chip high speed clock (HF CLK) will be used to send the encoded digital pattern to an SFQ pulse-splitter (S) network of M stages (M = 2 is pictured), which multiplies each SFQ input pulse from the CSR by 2^M. Combination of the SFQ pulses from each arm of the SQUID transformer (ST) network yields a multiSFQ pulse output with a time-integrated voltage area of $2^M h/2e$. In this schematic, the ST block represents both the SQUID transformer as well as the JTL inductively coupled to it.

Based on simulations, we expect that the network will remain time-synchronized for the generation of signals below 10 GHz. To synthesize higher frequency signals with sufficient amplitude accuracy and spectral purity, it will be necessary to include a synchronization procedure before the pulses are extracted from the ST in order to compensate for delay imbalances on the different arms of the splitter network. This would keep the multiSFQ pulse shape as narrow as possible and support a fast pulse rate with minimal pulse distortion caused by overlap of successive pulses in time. However, for the physical size of the VM and the frequencies of the generated signals discussed in this work, this is not yet necessary. Finally, a bandpass filter (not shown) can be used to remove the out-of-band harmonics and quantization noise, yielding the desired synthesized waveform.

The eventual target memory depth of the CSR buffer is determined by the parameters of the $\Delta - \Sigma$ encoding including the oversampling ratio, bandwidth, and desired noise floor. To generate a 10 GHz sine wave with spurious-free dynamic range (SFDR) of less than -70 dBc over a 0.1 GHz bandwidth, we estimate that a 4096-bit CSR clocked at a minimum of 40 GHz will be required. The three most challenging parts of this device are a CSR with enough memory depth and speed [28], a high-frequency clock source with low cycle-to-cycle jitter [29] (especially for the synchronous clocking of the last stages), and the voltage multiplier with large multiplication. In this article, we will discuss only the challenges of implementing the voltage multiplier.

The SFQ circuit for an $M = 3$ stage voltage multiplier ($\times 8$ VM) was fabricated at NIST using our process for self-shunted junctions with niobium-doped silicon (Nb_xSi_{1-x}) barriers [30]. The measured characteristic voltage $I_c \times R_s \simeq 250\ \mu$V. Note that we do not use explicit shunting resistors due

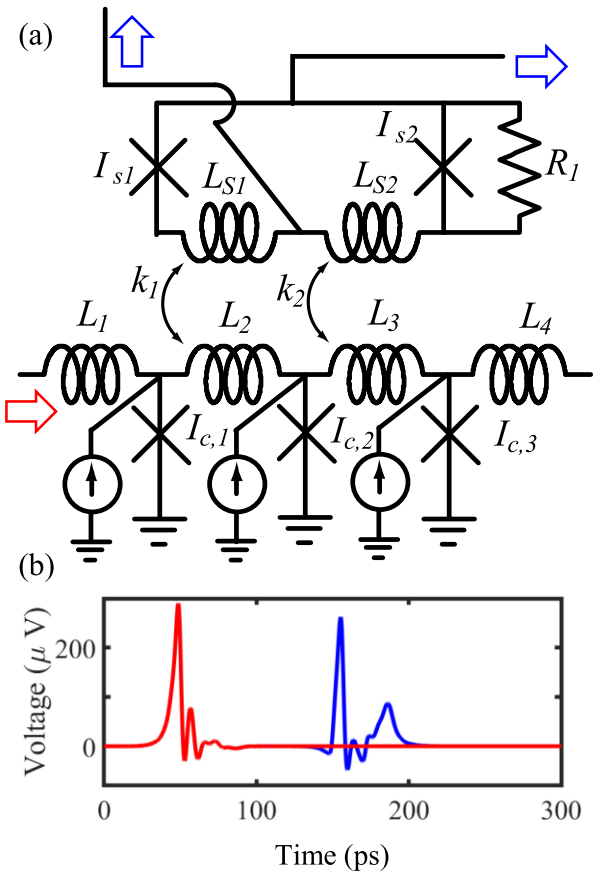

Fig. 2. (a) SQUID transformer schematic used for simulations. The circuit values are $I_{s1} = 137\ \mu$A, $I_{s2} = 246\ \mu$A, $L_{s1} = 3.75$ pH, L_{s2}=3.75 pH, $R_1 = 0.44\ \Omega$, $L_1 = 1.2$ pH, $L_2 = 3.32$ pH, $L_3 = 3.31$ pH, $L_4 = 1.13$ pH, $I_{c,1} = 373\ \mu$A, $I_{c,2} = 405\ \mu$A, $I_{c,3} = 430\ \mu$A, $k_1 = 0.41$, and $k_2 = 0.41$. (b) Simulated pulses at the input (red) and differential output (blue) of the ST. The output SFQ pulse is produced when both junctions in the SQUID pulse, with a small delay between each junction. This causes the pulse to have a larger spread than a traditional SFQ pulse and increases the output sensitivity to synthesis frequency and current bias. The damping factors for the junctions in the SQUIDs were designed to be different ($\beta_c = 1$ and $\beta_c = 0.1$ for $\mathrm{JJ_{s1}}$ and $\mathrm{JJ_{s2}}$, respectively) in order to enforce the correct switching sequence of the SQUID and increase the operating margin [11]. The voltage-time area for the red input pulse and the blue combined output pulse are each equal to Φ_0.

to our barrier material, except for one junction in the SQUID transformer to introduce an asymmetry in the damping [R_1 in Fig. 2(a)]. The simplified device used to test the voltage multiplier section of our SFQ JAWS design is shown in Fig. 3. The input drive signal (upper left) is launched into a 50 Ω coplanar waveguide transmission line terminated with a 50 Ω resistor (R_{in}) at the input of a dc-to-SFQ (dc-SFQ) converter. The output of the dc-SFQ cell is transmitted by a JTL into a network of splitters (S). The output of this network goes to eight different JTLs, all with the same length, that are inductively coupled to eight STs in series. Thus, for every pulse generated by the dc-SFQ, eight quantized SFQ pulses are added at the output of the ST array. This array is then connected to a 50 Ω CPW,[1] and the multiSFQ pulse is transmitted out the cryoprobe through a 50 Ω coaxial cable. At room temperature, the generated signal is analyzed using a spectrum analyzer or a 50 GHz high-speed oscilloscope.

A time-dependent voltage waveform is synthesized by implementing a $\Delta - \Sigma$ digital-to-analog conversion algorithm [2], using a 65×10^9 samples-per-second Keysight M8195a RF arbitrary waveform generator (RF AWG) that has an analog bandwidth of 25 GHz.[2] The desired waveform is first digitized using a two-level bandpass $\Delta - \Sigma$ modulation algorithm that yields a binary output and reduces quantization noise by pushing it out of the band of interest [1]. Using the RF AWG, this digital code is then converted into a pulse sequence that provides the input drive to the dc-SFQ cell. The dc-SFQ cell produces the SFQ pulses that are then transmitted to the splitter network and ST array to create the desired output waveform.

We studied the operating quantum-locking ranges (QLRs) of this DAC circuit during the generation of signals when applying these pulse-density modulated $\Delta - \Sigma$ codes. When the voltage multiplier operates within the QLR, the output and input are locked so that for every input pulse into the dc-SFQ there is one and only one composite output voltage pulse from the ST array with time-integrated voltage area of $2^M h/2e$. This occurs over a range of input parameters and environmental conditions, including dc bias current and temperature, that we call the QLR [4]. In the context of SFQ circuits, the QLR is often simplified to the span of one specific parameter, such as dc bias current (I_{dc}), where correct circuit operation is observed; the range of values is referred to as the "margins" or "margin range" with all other input parameters and environmental conditions fixed.

An advantage of our circuit compared to the traditional JAWS [31] circuit is that there is no direct transmission path of the input AWG drive signal to the output line from the SQUID array, dramatically reducing "feedthrough" signal (residual input drive current signal at the synthesis frequency that reaches the DUT output) which is a significant source of error in RF JAWS circuits [1]. However, we still measure a small amount of parasitic coupling between the input and output lines. To reduce this unwanted contribution to the output waveform, we used the "zero-compensation" technique described in [8] to shape, and effectively high-pass filter, the individual input drive pulses. We have tested that the dc-SFQ circuit properly operates when driven by this type of pulse. With the zero-compensation pulse shape as a baseline, we then optimized the pulse-shape to minimize feedthrough at the synthesized tone by varying the RF AWG finite-impulse-response tap values, as explained in [31].

Simulations and parameter optimizations were performed on the entire circuit using WRspice [32] and MALT [33]. For the simulations, we used a simple resistively and capacitively shunted junction model that matched both the $I_c R_s$ and $\beta_c \approx 1$ of our junctions. We simulated both the dc and RF outputs as explained in their respective sections below.

[1]The transition between the ST array and the pink output CPW is visible at the extreme right of Fig. 2(b). This transition is not ideal for high frequencies but simulations indicate that it shows negligible pulse distortion below 10 GHz.

[2]Commercial instruments and software are identified in this article in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the equipment identified is necessarily the best available for the purpose.

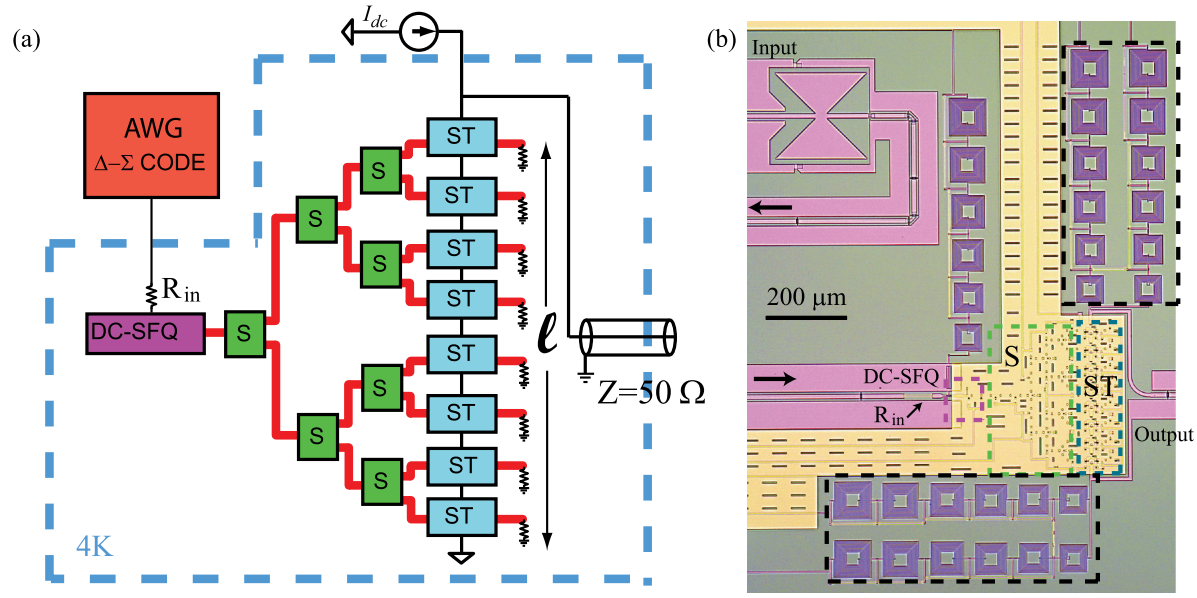

Fig. 3. (a) Simplified schematic of the ×8 voltage multiplier (VM) device under test (DUT) described in this report. (b) Picture of a portion of the fabricated DUT chip. The dc-SFQ converter and the splitter (S) and SQUID transformer (ST) network appear in yellow and are labeled. The purple spiral inductors enclosed in the black-dashed boxes are used as low-pass filters for bias lines of the device and to perform the dc measurements, i.e., current voltage characteristics and quantum-locking ranges. At both the input (left) and the output (right) of the VM, the signal is launched into the pink CPW transmission lines. Simulations show these microwave launches introduce negligible error in the generated amplitude at the relevant frequencies.

The chip was mounted on a cryogenic probe immersed in liquid helium at 4 K. Connections to room-temperature electronics were made using cryogenic-compatible semirigid coax for the high-frequency input and output lines. An on-chip dc block was used to isolate the SFQ input from low-frequency noise in the input pulse drive. Connectorized dc-blocks were placed at room temperature on the cryogenic probe to avoid introducing ground loops. We chose modulator algorithms and digital codes that produced SFQ pulses of a single polarity (positive) for all waveforms reported in this work. This is necessary for positive dc-biased SFQ circuits and also avoids deterministic jitter due to the timing shift between positive and negative polarity JJ pulses [19].

III. DC Characterization

We monitored several metrics to confirm that the voltage multiplier functions properly for a specific input drive pulse pattern. The simplest metric is a dc measurement of the output voltage as a function of dc bias current. When the voltage multiplier circuit is within QLR, each pulse in the input sequence, or period in the case of a continuous wave (CW) signal, produces one SFQ pulse from each SQUID. This yields a constant voltage step in the average dc output voltage versus applied bias current, given by

$$V_{out} = 8 \times \Phi_0 \times f$$

where f is the frequency of the applied CW signal and 8 corresponds to the number of parallel STs. Fig. 4(a) shows current-voltage characteristics of the ×8 VM obtained by applying high-frequency CW signals to the dc-SFQ converter. Constant-voltage steps are observed, independent of the bias current and equal to the expected quantized value, confirming that the system is operating within the QLR. The step widths, defined as the range of bias current where the voltage is constant within $\pm 1 \mu$V, are as wide as 65 μA at 20 GHz (20% of the SQUID critical current). The maximum tested input frequency of 40.0 GHz results in the expected output dc voltage of 662 μV. The dashed line in Fig. 4(a) shows the observed 2-dimensional extent of the QLR at 4 K for the dc bias current and CW input frequency for this VM circuit. Even though we observe the expected quantized voltage steps of the voltage multiplier at dc bias currents higher than $I_c \approx 330$ μA for higher input frequencies, we do not expect the voltage multiplier to work appropriately at those higher bias values when operated as a DAC at fixed bias current and with a broadband frequency distribution of input pulses. Thus, we exclude that area in our definition of QLR. The observed QLR is smaller than what we expected based on measured device parameters. Fig. 4(b) compares the observed QLR (dashed black line) to simulations with (dashed red line) and without (solid cyan line) Johnson noise at $T = 4$ K. A possible cause for the reduction of the QLR is larger than expected fabrication variation in the circuit parameters. Another known issue that can reduce the QLR is the parasitic capacitance between the JTL and ST which can affect the operation of the voltage multiplier as explained in [34]. The degree to which all these sources of error can affect the QLR is under investigation.

IV. RF Characterization

We characterized the synthesized RF signals by measuring the fundamental tone power and the total noise power, integrated over the bandwidth of the band-pass $\Delta - \Sigma$ code, as a function of dc bias current and determined the bias range where the output

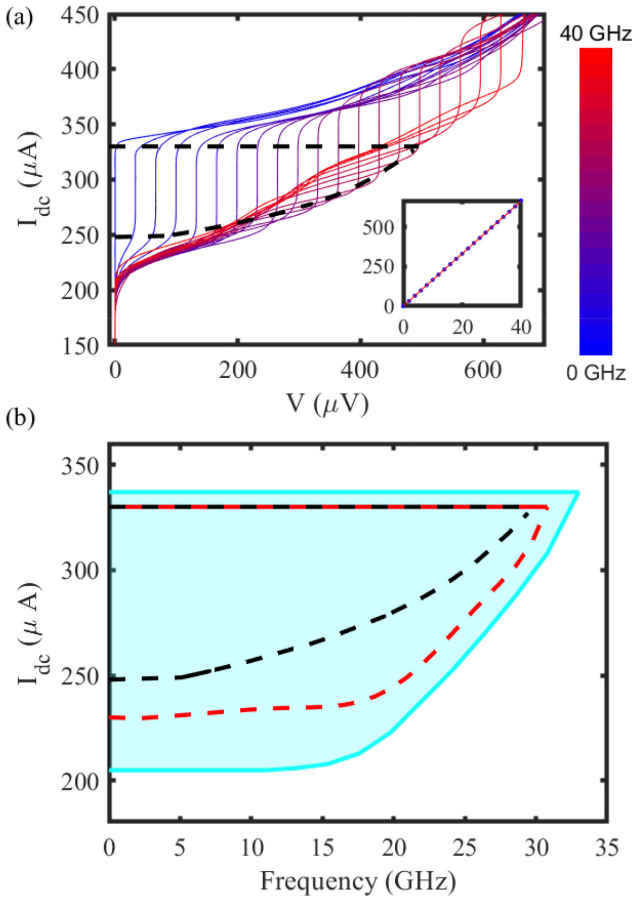

Fig. 4. Measurements at 4 K of constant voltage steps for a ×8 VM. (a) DC *I–V* characterization with increasing CW input signal frequency from 0–40 GHz in 2 GHz steps applied at the dc-SFQ converter. The dashed line is the observed area that is within the QLR, as defined in the text. Inset: Output voltage step amplitude (μV) versus input frequency (x-axis, GHz) showing expected linearity. (b) Simulations and comparison with observed behavior. Cyan is the expected QLR at T = 0. Red is the expected QLR at T = 4 K and black is the experimentally measured QLR from (a).

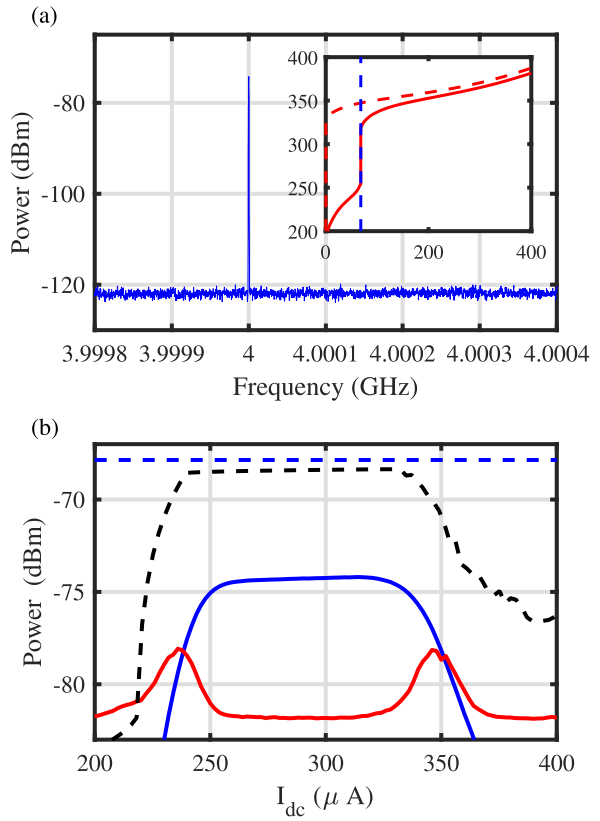

Fig. 5. (a) Power spectrum of a 4 GHz sine wave synthesized using a band-pass $\Delta - \Sigma$ digital code. The measurement was performed with a spectrum analyzer using a resolution bandwidth of 100 kHz and averaged 64 times. Inset: dc *I–V* curve (y-axis in microamperes, x-axis in microvolts) showing the expected constant voltage step at ∼66.2 μV [dashed blue line, from (1)] associated with the digital code sent to the DUT. Dashed-red curves show the *I–V*-characteristic when the $\Delta - \Sigma$ is both on and off. (b) Measured variation at 4 K of the fundamental tone power (blue line) and the calculated variation using a WRspice simulation (dashed black line) as a function of dc bias. The dashed blue line represents the expected ideal power assuming infinitely narrow output pulses. In red, we plot the noise power integrated over a 1 MHz range around the fundamental tone. Given that the fundamental has an expected variation as a function of bias, this integrated noise is a more sensitive metric to define the QLR [1].

power was nearly constant. Although minor variation in the fundamental tone power with respect to bias is both expected and observed within the QLR at gigahertz synthesis frequencies due to the bias-dependent width of the SFQ pulses [1], the dependence of fundamental tone power on bias is far larger once the circuit is biased outside of the bias QLR. However, we found that the integrated in-band noise power is a more sensitive metric for determining bias QLR. This metric is constant with respect to current bias to within the resolution of our measurement electronics if the circuit remains in the QLR. However, any erroneous output behavior causes a sharp jump in noise power, defining the QLR.

As one demonstration of the SFQ JAWS VM circuit's ability to synthesize gigahertz-frequency signals, we have synthesized a 4 GHz sine wave, as shown in Fig. 5(a). The figure shows the power spectrum as measured with a spectrum analyzer. To confirm that the circuit was operating within the QLR, the dc voltage was monitored through the low-pass taps on the circuit output (as in Fig. 4) and confirmed to be constant within ± 1 μV at the expected quantized value over a range of input dc bias currents. This is shown in the inset of Fig. 5(a).

We also measured the variation of the fundamental tone power as a function of dc current bias and compared it with the calculated variation using a WRspice simulation [Fig. 5(b)]. Because the pulses have a finite width, the value of the generated signal at finite frequencies deviates from the low frequency limit [1], [35]. This bias dependence of the output power is due to the bias dependence of the pulse shape generated by the voltage multiplier (see Section IV-A).

In separate measurements using a low-noise amplifier (LNA), we observed that the SFDR is −70 dBc over a 10 MHz bandwidth consistent with the $\Delta - \Sigma$ code used. The expected 4 GHz output voltage amplitude of this sine wave at the chip, assuming infinitely narrow output pulses, is given by $2^M \left(h/2e\right) f_s/2$, where f_s is the maximum input pulse rate (here 16 GHz). Using this formula, the on-chip expected output amplitude is ∼132 μV

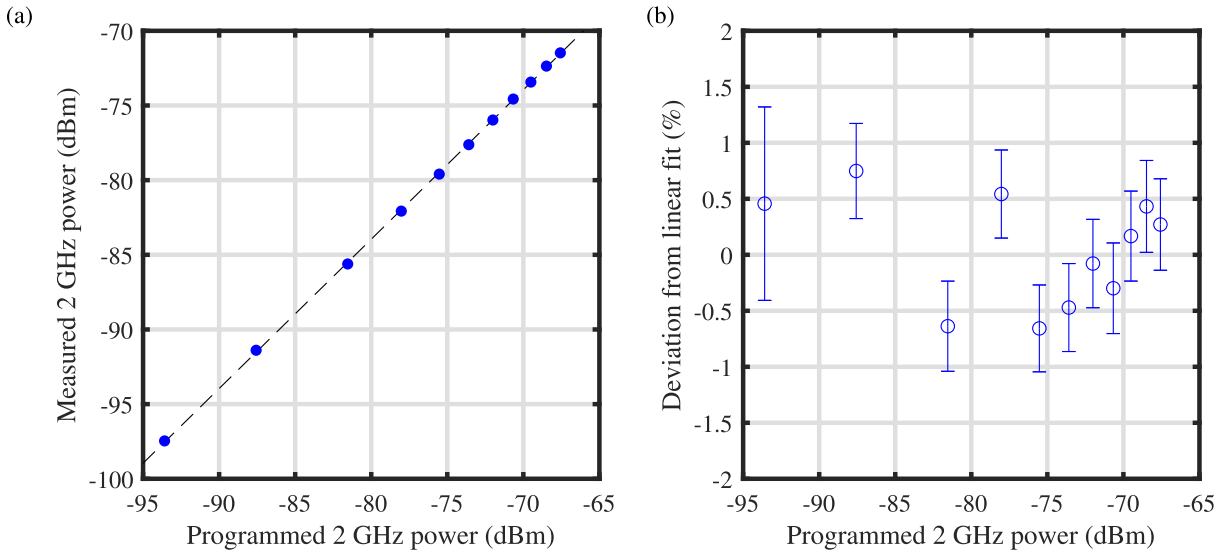

Fig. 6. (a) Measured output power versus programmed power for a synthesized 2 GHz sine wave. The curve is linear with unity slope and an offset of −4 dBm due primarily to attenuation in the output transmission path. (b) Percentage deviation of the data in (a) from the linear fit.

and the expected output power at the 50 Ω CPW is −68 dBm. The observed output power is 6 dB lower than expected due primarily to attenuation in the output line [36]. More accurate measurements in the future require a calibrated measurement at the chip in order to determine losses from impedance mismatches and cabling [37], [38].

In order to demonstrate the dynamic range of the synthesizer, we measured the output power as a function of the $\Delta - \Sigma$ code programmed power, as shown in Fig. 6(a). The input-to-output power transfer function is linear with unity slope and a constant offset of −4 dB, which again we attribute mostly to cable losses and impedance mismatches; this test was performed with an output tone of 2 GHz, instead of 4 GHz, so less attenuation is expected. The small deviation in the curve from a linear fit is shown in Fig. 6(b). Verifying the linearity of the system is an important step in developing a traceable RF power reference source.

We have also generated more complex signals such as multitones (Fig. 7), which are useful in the characterization of the nonlinearity of microwave components [5], and microwave pulses (Fig. 8), similar to the ones used in the preparation of qubits [39]. For the time traces shown, a room-temperature microwave LNA with a gain of 36 dB was used to amplify the output signal to a 50 GHz high-speed oscilloscope. To confirm that the circuit was within QLR, the dc voltage was monitored through the low pass taps on the circuit and confirmed to be fixed within ± 1 μV of the expected value over a range of input current biases. In both time-domain examples shown, only the envelope of the signals is visible in the figures since their output frequency is too fast compared to the time-scale shown.

A. *Sources of Error*

We have identified several sources of error in the VM circuit and measurement system that result in differences between the

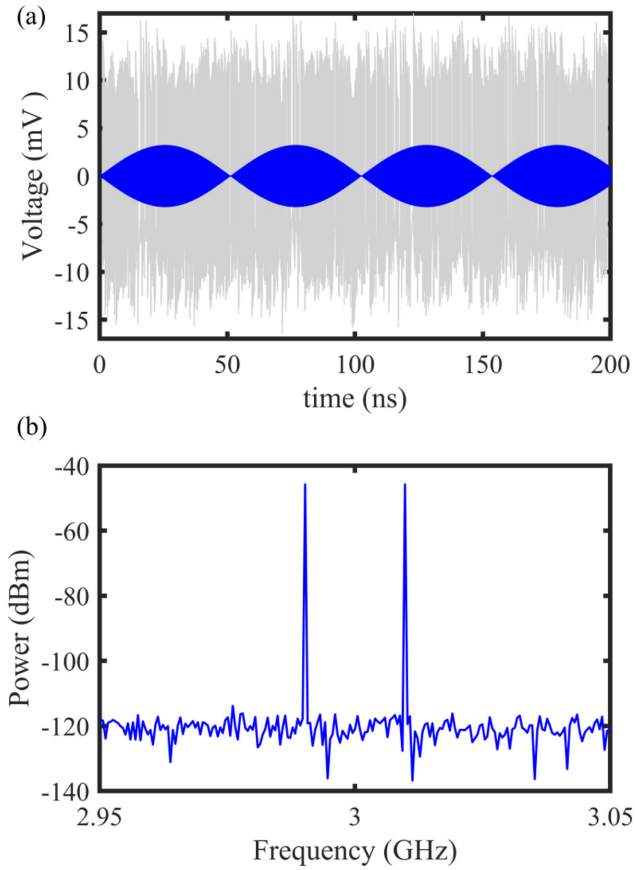

Fig. 7. Demonstration of a two-tone multisine signal synthesized at 3.00 GHz ± 10 MHz using the ×8 VM circuit. The raw output signal was amplified by a room-temperature LNA with a gain of ∼36 dB and captured with a 50 GHz oscilloscope. (a) Time-domain signal. In gray, the raw data contains the signal as well as the out-of-band quantization noise. In order to easily observe the data showing the voltage amplitude envelope, we apply a software band-pass filter to remove this out-of-band quantization noise (blue). (b) Measured spectral density of the signal.

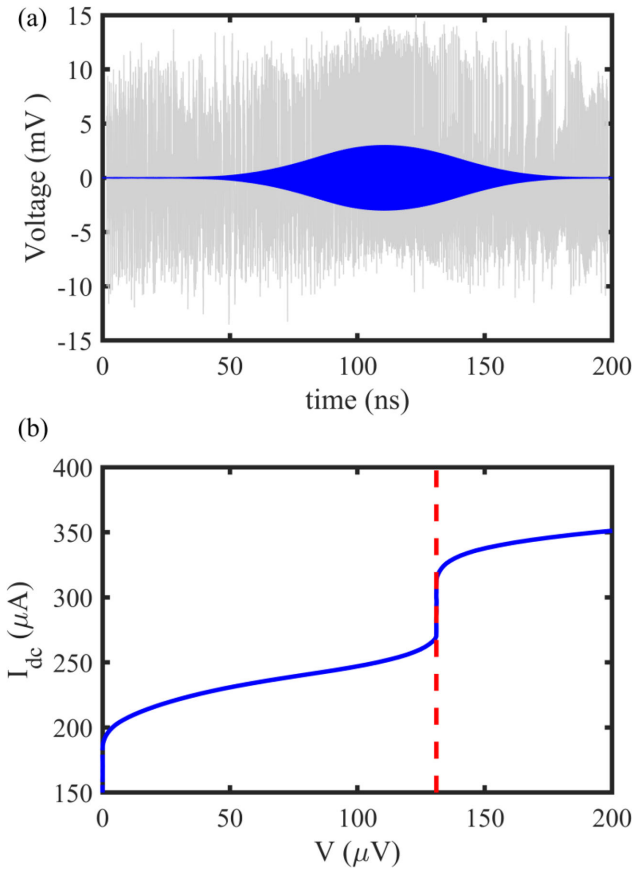

Fig. 8. (a) Synthesized Gaussian-shaped pulse of a 3 GHz signal showing the voltage amplitude envelope. As in Fig. 7(a), the raw output signal was amplified, captured with the scope (gray), and digitally band-pass filtered (blue) to remove the out-of-band quantization noise. (b) DC *I–V* curve of the $\times 8$ VM circuit showing the constant voltage step when the system is within the QLR.

measured output signal and the accurate quantum-based value desired for a primary metrological standard. The main source of error in the output power is due to attenuation from the off-chip measurement components, including the coaxial cable and SMA connectors that are responsible for 3–6 dB of attenuation, which increases with the frequency of the signal generated. Impedance mismatches between the different microwave components also affect the observed value. To accurately quantify these sources of error, our group is working on establishing a protocol for calibrating gigahertz signals generated inside the cryostat [38]. Another source of error is feedthrough, i.e., input signal reaching the output [1]. In the presented data, feedthrough was measured at < -50 dB, which was confirmed with complementary measurements using a network analyzer. The origin of this parasitic feedthrough has not been experimentally identified but should be further reduced by eliminating the large ($\sim$ 10 mV) input drive signal that is transmitted from room temperature and terminated on chip [see Fig. 3(a)] and instead using the planned on-chip memory to drive the voltage multiplier circuit using SFQ pulses, with significantly lower amplitudes, transmitted only on-chip (see Fig. 1). Another possible source of feedthrough could be due to the small parasitic capacitance between the JTL and ST which introduces a direct transmission of a finite part of the input signal to the output [34]. A full characterization of these parasitic couplings will be further investigated.

A more fundamental source of error originates from the finite width of the output pulses and is responsible for the slope in the nearly constant region of the fundamental tone power with respect to bias visible in the solid blue and dashed black lines in Fig. 5(b). As shown in [1], the DAC output waveform $v_{\text{out}}(t)$ is described by the convolution of the output pulse $p(t)$ from the ST array with the input digital code

$$v_{\text{out}}(t) = p(t) \otimes \sum_n w_n \delta(t - nT)$$

where the symbol $\otimes$ refers to convolution, T is the sampling period defined by the pattern generator, t is time, and n is the bit index of the input code w_n. In the frequency domain, this expression becomes

$$V_{\text{out}}(f) = P(f)W(f)$$

where $V_{\text{out}}(f)$, $P(f)$, and $W(f)$ are the Fourier transforms of the output waveform, the quantized pulse $p(t)$, and input $\Delta - \Sigma$ code $w(t)$, respectively. The only constraint we have is that the time integral of $p(t)$ is quantized, which means that the dc component of $P(f)$, $P(0)$, is exactly known and equal to $8 \times \Phi_0$. However, because the pulse $p(t)$ has a finite width, the value of $P(f)$ at frequencies other than zero will deviate from $P(0)$ [1], [35]. In our case, this effect is more pronounced given the expected behavior of the ST output pulses [see Fig. 2(b)], which depends on the pulsing of both junctions in each dc-SQUID. This effectively increases the pulsewidth by a factor of two compared to a single JJ pulse. Simulations predict the decrease in output power due to this increased pulsewidth to be less than 0.6 dB at 4 GHz. However, at frequencies as low as 10 GHz, this effect can cause a 2 dB reduction at the center of the margin range. This error can be reduced by increasing the $I_c R_s$ of the JJs.

In a lumped-element model of the ST network, the emitted pulse from each ST cell propagates instantly across the network to the common output creating a multiSFQ pulse with no additional increase in pulsewidth. This simplification is appropriate for a short chain but breaks down as the total length ℓ of the chain, as defined in Fig. 3(a), approaches the wavelength λ of the generated signal, effectively setting a limit of $\lambda/8 > \ell$. At shorter wavelengths (higher synthesis frequencies) the network acts as a distributed element, distorting the output pulse shapes [40], [41]. As explained previously, the wider output pulses will decrease the output amplitude below the expected quantized value. Simulations that include our estimate of the layout size of the ST network using the present NIST fabrication process put the maximum synthesis frequency at $\sim$10 GHz for a $\times 64$ VM ($M = 6$ stage) circuit.

Finally, random timing jitter could also introduce some broadening in the combined multiSFQ pulses due to the different time delays each SFQ pulse acquires as they travel across the splitter network. However, the expected single stage jitter is less than 1 ps ([42]) thus for a $\times 8$ VM where the pulses travel a total of less than 10 stages of JTLs before reaching the array of STs, this effect does not represent a meaningful source of error. Random timing jitter of the input drive pulses to the dc-to-SFQ

converter does not broaden the multiSFQ pulses but will result in a decrease in the JAWS output at the synthesized tones and an increase in the in-band noise [19].

V. Discussion and Future Experiments

There are multiple improvements needed for this system to become relevant for general metrological applications, starting with increasing the output power. Increased output can be achieved by increasing the number (M) of splitter stages. We have designed a circuit with $M = 6$ that will increase the voltage amplitude by an additional factor of 8 but will be limited to synthesis frequencies < 10 GHz due to the layout size. Improvements in the fabrication process to reduce ℓ will enable synthesis frequencies above this limit. Higher output is also possible by increasing the input pulse rate, with the goal of 120 GHz or higher, but additional system design improvements are required to enable these higher rates, such as increasing the speed of the STs with faster JJs (higher I_cR_s) and integrating the CSR and high-frequency clock on-chip [29] to drive the VM circuit as shown in Fig. 1.

In addition to the ST layout size, another limitation to synthesizing higher frequencies with the VM subcircuit is the effect of the 50 Ω load resistance (R_L) on the behavior of the junctions; this becomes particularly important when increasing the number (N) of ST cells. The parallel load resistance R_L effectively lowers the JJ shunting resistance and I_cR_{eff}, therefore decreasing the effective characteristic frequency of the SQUIDs [41]. In the case of N identical ST cells with $N \gg R_L/R_s$, where R_s is the intrinsic shunt resistance of the junctions, R_{eff} is given by

$$R_{\text{eff}} \approx \frac{R_L}{N}.$$

Based on WRspice simulations, we expect that a $\times 64$ VM would have a large enough QLR for synthesized signal frequency of 10 GHz assuming $R_L = 50\ \Omega$ and $I_cR_s = 1$ mV.

We are also investigating applications for our SFQ JAWS circuit designs that do not require significant improvements in output power or synthesis frequency but could benefit from the quantum-based stability and reproducibility of this microwave reference source. One such application is cryogenic quantum computing, where a low-power cryogenic microwave synthesizer is needed to enable the scalability required to construct an error-corrected quantum computer with thousands (or more) qubits [39], [43]. Coherent control of superconducting qubits is achieved by applying microwave pulses such as the one shown in Fig. 8. A full system like the one described in Fig. 1 could provide an in-cryostat, energy-efficient approach for the proximal generation of control, and readout signals in cryogenic quantum computing experiments [39], [44].

VI. Conclusion

We described a prototype SFQ-based design for a high-frequency quantum-based DAC for use as an RF reference source for communications metrology. This design has the potential to be integrated as a complete waveform synthesizer-on-a-chip and operated at high clock speed while delivering stable and reproducible quantum-based output with low feedthrough. We have demonstrated a key subcircuit of that design, a voltage multiplier amplifier that consists of a network of splitters and SQUID-based transformers and outputs quantized pulses with the flux-quantum accuracy preserved. Driving the x8 VM circuit with an input pulse rate of 16 GHz, we demonstrated synthesized waveforms with stable, reproducible, quantum-based output, including a 4 GHz sine wave with output power of -68 dBm and SFDR of -70 dBc, a two-tone wave centered at 3 GHz, and a Gaussian-shaped pulse of a 3 GHz signal.

Our near-term goals for expanding the capabilities of the SFQ JAWS system for gigahertz waveform synthesis include the following:

1) achieving higher output power (at least -30 dBm);

2) improving SFDR and output power accuracy by reducing feedthrough;

3) reducing loss in output power due to dependence of the pulsewidth with bias; and

4) synthesizing higher output frequencies.

The device has room for optimization that should allow us to accomplish these short-term goals. Based on simulations, increasing the I_cR_s product to 1 mV and incorporating a clocked CSR on-chip will provide an increase in the intrinsic clocking speed to more than 100 GHz and a gain of 14 dB in output power. This improvement combined with an increase in the number of ST to $\times 64$, will get us close to the desired output of -30 dBm for signals up to 10 GHz.

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