The effect of strain on tunnel barrier height in silicon quantum devices

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Semiconductor quantum dot (QD) devices experience a modulation of the band structure at the edge of lithographically defined gates due to mechanical strain. This modulation can play a prominent role in the device behavior at low temperatures, where QD devices operate. Here, we develop an electrical measurement of strain based on the I(V) characteristics of tunnel junctions defined by aluminum and titanium gates. We measure relative differences in the tunnel barrier height due to strain consistent with experimentally measured coefficients of thermal expansion (α) that differ from the bulk values. Our results show that the bulk parameters commonly used for simulating strain in QD devices incorrectly capture the impact of strain. The method presented here provides a path forward towards exploring different gate materials and fabrication processes in silicon QDs in order to optimize strain.

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I. INTRODUCTION

Gate-defined silicon-based quantum dot (QD) devices are some of the world's most sensitive devices[1,2], have been demonstrated as qubits[3–5] and are promising as quantum current standards[6–8]. Fulfilling these applications ultimately requires a large number of well-defined, reproducible devices. Unfortunately as of this writing, unintentional QDs, those dots inconsistent with the electrostatics of the gate design, are quite common in silicon MOS devices. Along with disorder, gate-induced strain can produce unintentional QDs[9,10] and affect the tunnel coupling between dots or to the leads[7]. In contrast to unintentional QDs due to disorder unintentional QDs due to gate-induced inhomogeneous strain should be reproducible and systematic in nature. Since the strain from the gate dielectric is homogeneous on the length scale of the QD, the main two sources of inhomogeneous strain are: 1) the coefficient of thermal expansion (α) mismatch between the gate material and the silicon and 2) the intrinsic strain of the gate. The resulting conduction band modulation, ΔE_c, derived from this strain is potentially as large as the electrostatic modulation in the device and, therefore, important in determining device characteristics[9]. Thus, to obtain devices which perform as intended, strain must be assessed and factored into device design and fabrication. Properly considered, strain could also provide an exciting avenue toward simplifying device design by reducing the number of necessary gates. Strain simulations may be used to guide QD design, but the lack of experimental measurements confirming their results at low temperatures limits their usefulness. Thus, the ability to measure the effects of strain at low temperatures will be extremely valuable in making improvements to QD simulations, fabrication, and performance.

The strain landscape in a silicon QD depends heavily on the operating conditions and fabrication process. This suggests the most applicable measurement of strain is one that can be performed under the same operating conditions (T$\approx$1 K) and adhering to the same fabrication constraints. The gate-induced inhomogenous strain is typically $\frac{\Delta x}{x} \approx 10^{-4}$ and varies over the minimum feature sizes in gate layout, of order 10's of nanometers. It is challenging to find a method for measuring strain with the necessary sensitivity and spatial resolution which can be performed at low temperature. For instance, transmission electron microscope (TEM)-based methods[11] can meet the spatial and sensitivity requirements but are typically not performed at low temperatures, destroy the sample, and may alter the strain through sample preparation[12]. High resolution electron back-scatter detection[12,13] is a non-destructive method that could be used to meet the spatial and sensitivity requirements, but similar to TEM-based techniques, is not typically performed at cryogenic temperatures. X-ray diffraction (XRD)[14] and Raman[15] techniques can perform a non-destructive measurement but have difficulty achieving the necessary spatial resolution while also not approaching cryogenic temperatures. Electrical measurements of strain are advantageous because the necessary sensitivity can be achieved at cryogenic temperatures. Piezo resistive sensors[16,17] have been demonstrated to meet both of these requirements but only in micron scale devices. Ref 18 measured strain via a shift in the electron spin resonance frequency of Bi donors at T=20 mK with a sensitivity of 10^{-7} but the results cannot be easily translated to gate-defined QDs.

The goal of this manuscript is to present a comparison between simulations and measurements of the effect of strain on the tunnel barrier height of devices shown in Fig. 1. Our strategy is to first perform transport measurements on separate tunnel junction devices made with aluminum and titanium gates. A tunnel barrier is formed in the gap between the gates where, for a range of gate voltages, inversion layers form at the Si-SiO_2 interface under the gates but not in the gap between them (see Fig. 1). We then fit the conductance as a function of bias voltage and extract the barrier height, ϕ_{tot}, as a function of gate voltage. When properly controlled, the difference between these barrier heights gives a measure of the change in strain due to the change in gate material in otherwise identical devices. We further characterize the metal films by measuring the coefficient of thermal expansion, α, at room temperature. Then, using the measured geometry for the device, we simulate the α-induced strain difference using bulk values of α, and our experimentally measured values of α. We find that our tunnel junction measurement of the strain difference agrees with simulations provided we use our experimentally measured values of α.

II. METHODOLOGY

The device layout is designed to enable four-terminal measurements and independent tuning of the electron density on either side of the barrier. As a consequence of the four-terminal design, the left (right) gate, source (drain) and one of the voltage probes can be used as a transistor to measure threshold, V_T on either side of the barrier. As with QD devices, our tunnel junction (TJ) device platform easily lends itself to future work exploring deposition parameters and anneals to manipulate inhomogeneous strain. Our method for measuring relative strain satisfies the sensitivity, spatial resolution and low-temperature requirements noted above. Moreover, the fabrication and measurements are similar to those for QDs so that this method is directly relevant for QD devices.

Our data provide an important step forward in assessing gate-induced strain in QD devices in-situ while highlighting the need for further experimental work and a greater theoretical understanding of the electrostatics.

Deformation potential theory, originally laid out by Bardeen and Shockley[19], shows that the silicon band structure distorts in the presence of applied strain. For the case of inversion layers in silicon, we need only consider the z-valleys[20], but strain affects all six valleys in an analogous manner. Here, the z-axis is the direction perpendicular to the Si-SiO_2 interface. The modulation of the conduction band (ΔE_c) can be written as[21]:

$$\Delta E_c = \Xi_u \varepsilon_z + \Xi_d (\varepsilon_x + \varepsilon_y + \varepsilon_z) \tag{1}$$

where ε_i is uniaxial strain in i-direction. Ξ_u and Ξ_d, are the uniaxial and dilation deformation constants, respectively. For the device in Fig. 1, the strain along the length of the channel (dashed yellow line) will be inhomogeneous between the gates. For most metal gates, α of the gate material is significantly larger than silicon, so that at cryogenic temperatures, the gate material contracts significantly more than the silicon substrate. The relative rate of expansion/contraction between the substrate and gate materials will be determined by the various mechanical properties of each material such as alpha, Young's modulus, and poisson's ratio. In this case, the gate material is under tensile strain due to the silicon and the silicon is under compressive strain due to the metal. In silicon $\Xi_u, \Xi_d > 0$ so that compressive strain ($\varepsilon_i < 0$) of the silicon corresponds to $\Delta E_c < 0$ in the region directly under the gate. In the region near the edges of the gate and in the gap, the strain in silicon shifts such that $\Delta E_c > 0$. For this reason, in our TJ devices, we expect that a larger α difference between the gate material and the silicon leads to a larger barrier height (see supplemental Fig. S1).

For bulk silicon, experimental values of Ξ_u range from 8.7 eV[22–24] to 9.6 eV[25] with theoretical values in the range of 8-10.5 eV[21]. In contrast, Ξ_d ranges from 1.1 eV[22,25] to 5.0[21]. In this manuscript, we use the values from Ref 22 ($\Xi_u = 8.7$ eV, $\Xi_d = 1.1$ eV). Using Eq. 1, we can develop a feel for the potential sensitivity for our strain measurement. Since Ξ_u is roughly eight times larger than Ξ_d, the dominant contribution to deformation potential will be from $(\Xi_u + \Xi_d)\varepsilon_z$. A strain in the z-direction of $\varepsilon_z = 10^{-4}$ corresponds to approximately 1 meV, a measurable change in our devices.

We model the total tunnel barrier height, ϕ_{tot} in a single device at zero bias as,

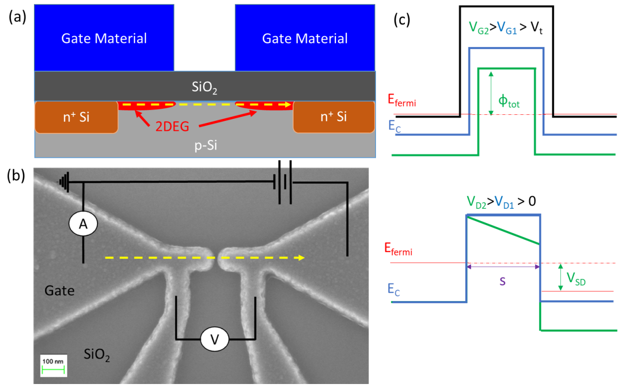

FIG. 1. (a) Schematic cross-section of the metal-oxide-semiconductor (MOS) tunnel barriers used in this work. The barrier is formed by modulation of the conduction band in the gap between the gates. (b) SEM image of a titanium-gated tunnel barrier device similar those used in this manuscript. For the data presented in the manuscript Ti-gated devices have 500 nm wide gates and Al-gated devices have 100 nm wide gates. (c) Schematic of the expected electrostatic dependence in the trapezoidal barrier model, where the barrier height (labeled ϕ_{tot}) and width (labeled s) will both decrease with increasing gate voltage and the source-drain bias has the effect of tilting the barrier.

$$\phi_{tot} = \phi_{\varepsilon} + \phi_0 + \phi_{ES}(V_G - V_T) \tag{2}$$

where ϕ_{ε} is the strain-induced portion of the barrier, ϕ_0 is the electrostatic portion of the barrier at threshold, V_T, $\phi_{ES}(V_G - V_T)$ describes the gate voltage dependence of ϕ_{tot}, and V_G is the gate voltage. To extract the absolute value of ϕ_{ε} in a single device requires a model which predicts both ϕ_0 and $\phi_{ES}(V_G - V_T)$ from the geometry, semiconductor physics, and defect charge densities. Our attempts to model ϕ_0 and $\phi_{ES}(V_G - V_T)$ using COMSOL to solve the Poisson and drift-diffusion equations fail to produce a tunnel barrier over any appreciable range of gate voltage above threshold for the leads, contradicting the experimental data. We speculate this is due to a larger density of states which overestimates the charge density in the barrier, however, we cannot rule out a lack of lateral confinement[26]. We, therefore, do not extract an absolute value of ϕ_{ε}. We can, however, extract changes in ϕ_{ε} between devices with different gate materials, if $\phi_0^1 \approx \phi_0^2$ and $\phi_{ES}^1(V_G - V_T) \approx \phi_{ES}^2(V_G - V_T)$ so that $\phi_{tot}^1 - \phi_{tot}^2 \approx \phi_{\varepsilon}^1 - \phi_{\varepsilon}^2$ where the superscripts 1 and 2 refer to different materials. ϕ_0 is determined by the metal semiconductor work-function difference and defect charge densities. Controlling ϕ_0 requires we reproducibly minimize the unwanted charge density at the interface and in the oxide. To control for the inevitable work function difference in our analysis, we will compare ϕ_{tot} from different devices on a $V_G - V_T$ axis. In addition to charge density and the work-function difference $\phi_{ES}(V_G - V_T)$ is also determined by the geometry (gate and gap dimensions). We control for this effect by comparing devices with the same geometry. Thus, our analysis assumes 1) that the work function difference between the two materials is accounted for by subtracting off the threshold voltage; 2) using standard fabrication methods, variations in the amount of charge in the gate oxide have been reduced to a negligible level; and 3) any effect other than strain which would produce a difference in barrier height in nominally identical devices, save for the gate materials, is negligible. We examine whether our experiment satisfies these assumptions later.

III. DEVICE FABRICATION

All the devices discussed here were fabricated as identically as possible to reduce the impact of the device-to-device variation. The starting point is boron-doped silicon <100> wafers with a resistivity of 5 Ω·cm to 10 Ω·cm. First, ohmic contacts are formed by phosphorus implantation. Following this, a 120 nm thick field oxide is grown in a wet oxidation furnace at 900 °C, and etched away in the regions where final devices will be written. Next, a 25 nm gate oxide is grown in a dry oxidation furnace at 950 °C. The gates are patterned using a positive tone e-beam lithography liftoff process with a PMMA bi-layer resist stack. We chose to fabricate devices with aluminum and titanium gates. These metals were chosen because there is a large separation in their bulk α values, they have quite similar work-functions[27], and the fabrication process is nearly identical. The gate metals are deposited via e-beam evaporation at ambient temperature at a rate of roughly 0.1 nm/s to respective thicknesses of 80 nm and 60 nm[28]. Finally, aluminum is sputtered to form contacts and an anneal is performed in 10 % forming gas (H_2/N_2) at 425 °C for 30 minutes. The devices are then cooled to $T = 2$ K where DC-$I(V_D)$ are measured for different V_G, where V_D refers to device bias (typical device resistances are in excess of 1 MΩ). We have filtered the devices we present to show only those which exhibit relatively weak disorder, with little to no oscillations in the turn-on $I(V_G)$ or 2d $I(V_D,V_G)$ data (see Fig. S2)[29]. This is done to ensure that disorder does not significantly affect ΔE_c and lead to spurious results with respect to strain (assumption 3 above).

IV. RESULTS

Figure 2 shows typical transport data extracted from our devices for three different gate voltages. The parabolic dependence of the conductance, $G(V_D) = dI/dV_D$, indicates that our tunnel

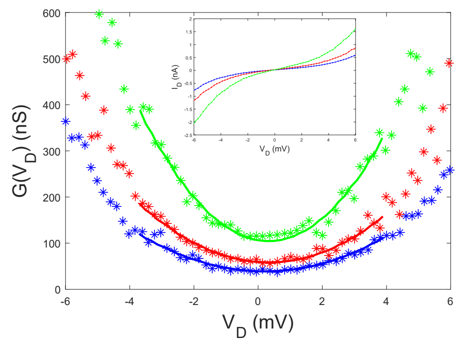

FIG. 2. 4-terminal DC transport data for a tunnel junction device. The inset shows the measured $I(V_D)$ used to obtain the conductance (dI/dV_D) through numerical differentiation that is plotted in the main panel. The blue, red, and green curves are taken at gate voltages of 0.87 V, 0.88 V, and 0.89 V, respectively. The lines are quadratic fits to equation 3 (see text). All data are taken at $T = 2$ K.

junctions exhibit a single barrier at each value of V_G shown. The data also show a clear change in the curvature of $G(V_D)$ indicating that the barrier parameters change with gate voltage. In our devices ϕ_{tot} and the barrier width, s, will be a function of V_G. $\phi_{tot}(V_G)$ and $s(V_G)$ should decrease with increasing V_G (see schematics in Fig. 1(c)). This arises from two sources: the increase of $E_{fermi} - E_c$ in the leads with increasing gate voltage and the deformation of the barrier due to fringing fields. The former only depends on the oxide thickness, while the latter also depends on the gate geometry.

To extract $\phi_{tot}(V_G)$ and $s(V_G)$ from the data of figure 2, we assume a trapezoidal barrier[30] and fit the tunneling conductance, $G(V_D)$ to[31]:

$$\frac{G(V_D)}{G_0} = 1 - \frac{\sqrt{2m}s\Delta\phi_{tot}}{12\hbar\phi_{tot}^{3/2}} eV_D + \frac{ms^2}{4\phi_{tot}}(eV_D)^2 \tag{3}$$

where s, ϕ_{tot}, and $\Delta\phi_{tot}$ are the barrier width, barrier height, and barrier asymmetry respectively. Here, $G_0 = \frac{eW_g t_{inv}}{h}\frac{\sqrt{2m_e^* e\phi}}{s}$ where $t_{inv} = 4$ nm is the inversion layer thickness[20], W_g is the gate width, e is the elementary charge, m_e is the effective mass, and h is Plank's constant. It is worth noting that there is no clear mechanism in our devices for $\Delta\phi_{tot} \neq 0$ and fits including the linear term reveal it to be small.

The extracted $\phi_{tot}(V_G)$ are shown in Fig. 3(a) for both gate materials. ϕ_{tot} is similar in magnitude in the two sets of devices and decreases approximately linearly with $V_G - V_T$. The slope of $\phi_{tot}(V_G - V_T)$ is similar in Al and Ti devices, 0.014 ± 0.005 eV/V and 0.022 ± 0.002 eV/V, respectively. Previous results on similar gate defined tunnel barriers[32–36] have shown an approximately linear dependence on gate voltage over higher voltage ranges and an approximately exponential dependence at lower gate voltages[26]. The linear dependence is evocative of a simple capacitive model[32] discussed more below. In general, there is good agreement between the extracted barrier width at its maximum and the lithographic dimensions as measured through FE-SEM (see supplemental Fig. S3). This suggests that our barrier model and fitting procedure are reasonable. The uncertainty in the total barrier height is the 2σ statistical uncertainty in the fit parameters.

Before moving on to extract any effect of strain from the data in Fig.3a, we check the validity of our assumptions regarding the electrostatics of the devices (assumptions 1 and 2 above). We use three aspects of the data as indicators of the degree of electrostatic similarity between devices: 1) agreement between $\phi_{tot}(V_G - V_T)$ in different devices with the same gate material; 2) V_T uniformity in the leads of different devices and gate materials; and 3) agreement of the electrostatic lever arm, β, between devices with different gate materials. Figure 3a clearly shows $\phi(V_G - V_T)$ in devices made with the same materials agree to within the uncertainties. This supports our assumptions and provides evidence the electrostatics of the barrier are not changing from device to device through, for instance, variations in the defect density in the tunneling gap. V_T for the devices are obtained by averaging the left and right lead values. For the two Al devices V_T is 0.62 V and 0.61 V, respectively. V_T for the two Ti devices is 0.52 V, and 0.60 V, respectively. We consider these values to be in good agreement. Finally, the first column of table I shows $\beta = \Delta\phi_{tot}/e\Delta V_G$ as measured through 2D conductance plots for different gate materials (see supplemental). These values agree to $\approx$10 %. Considering these indicators together, we regard our assumptions as satisfied.

We calculate the difference in strain between Ti and Al-gated devices from the data in Fig. 3a as $\phi_\varepsilon^{Ti} - \phi_\varepsilon^{Al} = \phi_{tot}^{Ti}(V_G - V_T) - \phi_{tot}^{Al}(V_G - V_T)$, where superscripts Al and Ti refer to the different gate materials. $\phi_{tot}^{Ti}(V_G - V_T) - \phi_{tot}^{Al}(V_G - V_T)$ is averaged over $0.4 \leq V_G - V_T \leq 0.46$ and appears as the right-most data point in Figure 3b. Based on bulk α values of the gate materials, we would expect $\phi_\varepsilon^{Al} > \phi_\varepsilon^{Ti}$, however, our data show that $\phi_\varepsilon^{Ti} > \phi_\varepsilon^{Al}$. We can make this comparison more quantitative by performing COMSOL simulations of the mechanical effects only using the bulk values of the α for each gate material ($\alpha_{Ti} = 8.9 \pm 0.1 \times 10^{-6} K^{-1}$, $\alpha_{Al} = 23.0 \pm 1.0 \times 10^{-6} K^{-1}$)[37]. This value appears as the leftmost data point in Fig. 3b and strongly disagrees with our data. To resolve this disagreement we perform simulations using experimentally measured values of the α for each material ($\alpha_{Ti} = 16.2 \pm 2.0 \times 10^{-6} K^{-1}$, $\alpha_{Al} = 23.0 \pm 2.8 \times 10^{-6} K^{-1}$). The α_i are measured from the slope of film stress, $\sigma(T)$, while stepping temperature, T, of blanket films processed in the same way as the tunnel junctions using a Flexus 2320 wafer curvature measurement tool. α_i was

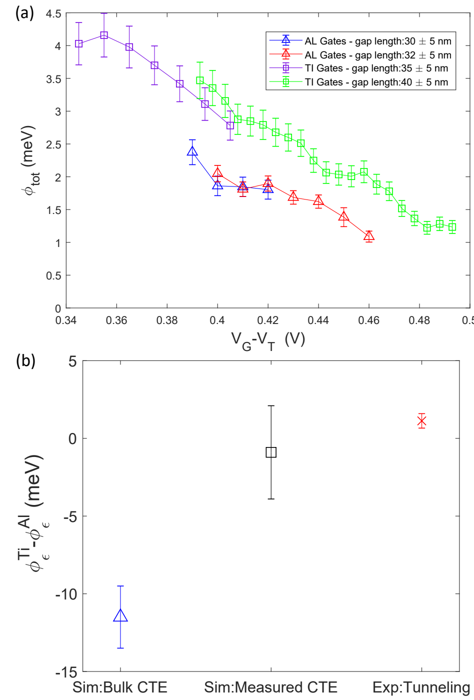

FIG. 3. (a) Barrier height as a function of gate voltage for different MOS tunnel junctions. The barrier heights for metal devices show a consistent trend of decreasing height. The uncertainty on the barrier height represent a statistical uncertainty for a 95 % confidence interval. (b) Comparison of the barrier height difference between Ti and Al devices using the data from (a) and the expected barrier height due solely to strain from COMSOL simulations (see supplemental). The experimental data point is calculated from the average difference over $0.4 \leq V_G - V_T \leq 0.46$ V. The uncertainty in bulk simulations corresponds to the range of differences obtained by assuming an uncertainty of one in the last digit of the values of α in Ref 37. The uncertainty in the measured α simulations corresponds to the 1σ uncertainty in our measurements of α. The uncertainty in the tunneling data corresponds to the propagated uncertainties in (a).

determined by measuring the wafer curvature over a range of 40 °C to 100 °C and performing a linear fit to that data. The result of simulations using these experimental values as inputs appears as the middle data point in Fig.3b and agrees with our experimentally measured value to within our uncertainties.

While there is good agreement between our measured α_{Al} and the bulk value, our measured α_{Ti} is significantly larger than the bulk value. This is likely the result of the deposition process which impacts the film morphology so that $\alpha_{film} \neq \alpha_{bulk}$[38]. It is important to note that the simulations only consider strain due to the α mismatch between the materials generated by cooling to $T = 2K$, and treat α as a constant equal to its room temperature value. Since α decreases toward zero with decreasing temperature[39], the simulated barrier height is likely an upper bound on $\phi_\varepsilon^{Ti} - \phi_\varepsilon^{Al}$.

Finally, while a detailed electrostatic model to predict ϕ_0 and $\phi_{ES}(V_G - V_T)$ is beyond the scope

Material	β from 2D $G(V_D, V_G)$ (eV/V)	β from $\phi_{tot}(V_G)$ (eV/V)
Al	0.067 ± 0.02	0.014 ± 0.005
Ti	0.073 ± 0.02	0.022 ± 0.002

TABLE I. Comparison of the lever arm, β (in uits of eV/V), obtained from 2D conductance data by performing a linear fit at constant conductance following Ref 32 (column 1) and by calculating the slope of the data sets in Fig. 3(a) (column 2). The uncertainty on the lever arm represents a statistical uncertainty for a 95 % confidence interval.

of this paper, we investigate whether a simple model can predict the slope of ϕ_{tot} in Fig. 3a. Motivated by the linear dependence of ϕ_{tot} on V_G, we apply the linear gate voltage model from reference 32 to $\phi_{ES}(V_G - V_T)$ from equation 2 as $\phi_{ES}(V_G - V_T) = -e\beta(V_G - V_T)$. Here, e is the elementary charge and β is the lever arm of the gate on the barrier. We can now compare the value of β determined in two different ways: 1) the slope of the data in Fig. 3a, 2) linear fits to 2D conductance data (see supplemental). The result of this comparison is shown in Table I. The values obtained from the 2D conductance data agree to within a factor of five with those determined by the slope of ϕ_{tot}. Considering the simplicity of the model and that the range of V_D considered for the 2D conductance value of β corresponds to Fowler-Nordhiem tunneling, while β from $\phi_{tot}(V_G - V_T)$ is at $V_D = 0$, we believe the agreement is reasonable.

V. DISCUSSION

Our results underscore the need for further experimental studies to realize the goal of ameliorating or controlling strain in silicon QDs. Figure 3b indicates that simulations of strain, which often use bulk values of α, can lead to erroneous conclusions if not coupled with experimental results. Moreover, while our data agree with continuum mechanics simulations, it is unclear why agreement can be reached while neglecting the intrinsic stress of the gate. A series of measurements of TJ devices which span the range from α-dominated to intrinsic dominated strain could shed light on this question. This could be achieved with TJ devices made with the same gate material but deposited under different conditions or subject to differing anneals to tune the film stress.

In addition, there is a lack of research on the overall benefits of adjusting the fabrication process to control strain. In particular, deposition and annealing parameters are typically chosen with goals other than mechanical properties in mind. For example, the gate depositions and forming gas anneals in this work were not optimized for control of the mechanical properties, but rather for the lithography process and to reduce oxide charge defects. Smaller grain sizes are usually preferred for making small structures via liftoff but this most likely leads to mechanical properties different from the bulk[40,41]. Additionally, there is tension between performing the anneal in a way that minimizes the impact of defects or minimizes the change in mechanical properties[42]. These very common choices may not be optimal. As a result, it is still unknown how large a role strain plays in design fidelity and reproducibility.

Finally, the framework for studying strain introduced here is quite flexible and can be applied to a wide variety of potential gate materials. A limitation of the present measurement of strain is that it relies on a comparison between different devices which requires considerable effort to reduce device-to-device variations. This burden may be lessened by making tunnel junctions with different materials on each side of the junction or the same material with different deposition parameters. Fabricated this way, the strain difference is encoded in the barrier asymmetry which can be directly measured. While still a relative measure of strain, this method would allow measurement within the same device and cooldown, reducing the effect of device-to-device variations.

SUPPLEMENTARY MATERIAL

See supplementary material for simulations of the strain induced barrier height and the determination of lever arms from 2d conductance data. It also includes additional data not presented in the main text.

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DISCLAIMER

Certain commercial equipment, instruments, and materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supplmentary Material- The effect of strain on tunnel barrier height in silicon quantum devices

	Material parameters used in COMSOL simulations		
Material	$\alpha(10^{-6}K^{-1})$ at 300 K	$[E_x, E_y, E_z]$(GPa)	$[\nu_{xy}, \nu_{xz}, \nu_{yz}]$
Aluminum	23	[70,70,70]	[0.35,0.35,0.35]
Titanium	8.6	[116,116,116]	[0.321,0.321,0.321]
Silicon dioxide	0.49	[73,73,73]	[0.17,0.17,0.17]
Silicon	2.6	[169,169,130]	[0.064,0.28,0.36]

TABLE S1. Elastic material constants used for strain simulations in COMSOL. The silicon is treated as an orthotropic material and the formatting for material parameters are $[E_x, E_y, E_z]$ and $[\nu_{xy}, \nu_{xz}, \nu_{yz}]$ for Young's modulus and Poisson's ratio respectively.

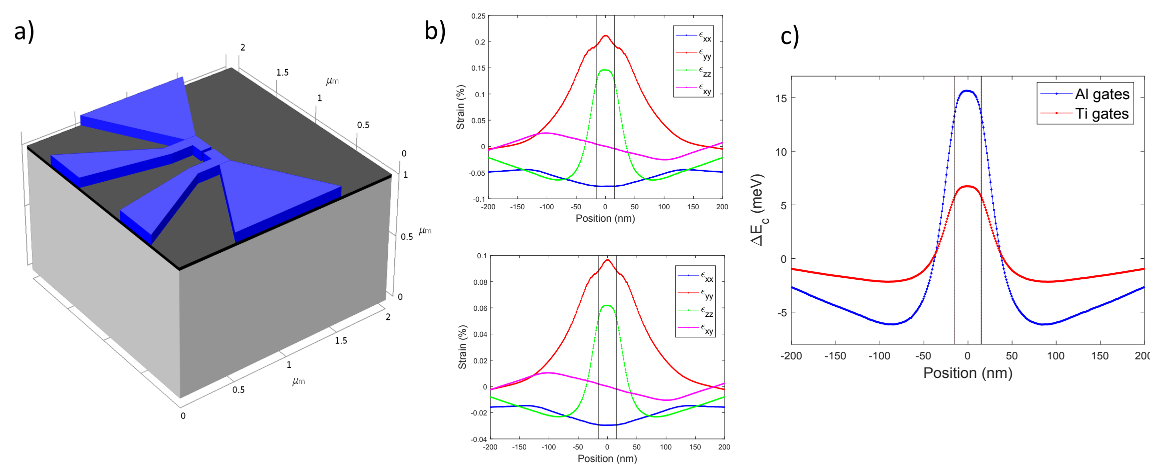

FIG. S1. (a)Schematic of the 3-dimensional device model used in COMSOL simulations for a device with a 25 nm thick gate oxide, 30 nm wide tunnel gap, and 100 nm wide gates. (b) Plot of various strain components Al (upper plot) and Ti (lower plot) gated devices at 2 K. (c) Plot of the conduction band modulation along the channel using the strain components in (b). The vertical black lines in (b) and (c) denote the edges of the gates.

The strain induced modulation of the conduction band in our devices has been simulated using finite-element modeling (FEM) in COMSOL using the linear elastic module. The simulations consider the effects of thermal strain from the α mismatch of the different materials only. The calculated strains in the 3-dimensional device structure are used with the deformation potential to determine the local modulation in the silicon band energies. Using the material parameters listed in Table S1, we simulate the resulting inhomogeneous strain at cryogenic temperatures in our tunnel junctions. The device model in Fig. S1 (a) is fixed at the bottom of the silicon block with a zero displacement boundary condition such that all strain components are zero at that interface for all temperatures. The crystal axes are set using the orthotropic elasticity matrix for silicon applicable to silicon (100) wafers used in our devices, where $x = [110]$, $y = [\bar{1}10]$,$z = [001]$. The poly-crystalline gate materials and the amorphous gate oxide are treated as isotropic materials. For these simulations, we have used the room temperature value α for all materials. The results of the COMSOL simulation are strongly dependent on the choice of parameters such as the tunnel junction dimensions and oxide thickness. The results in the Fig. S1 are calculated for parameters most relevant to the experimental data in this manuscript (25 nm oxide and 30 nm wide gap length). Based purely on the bulk α values, the expected difference in the barrier height in the gap is about 11 meV as shown in S1c.

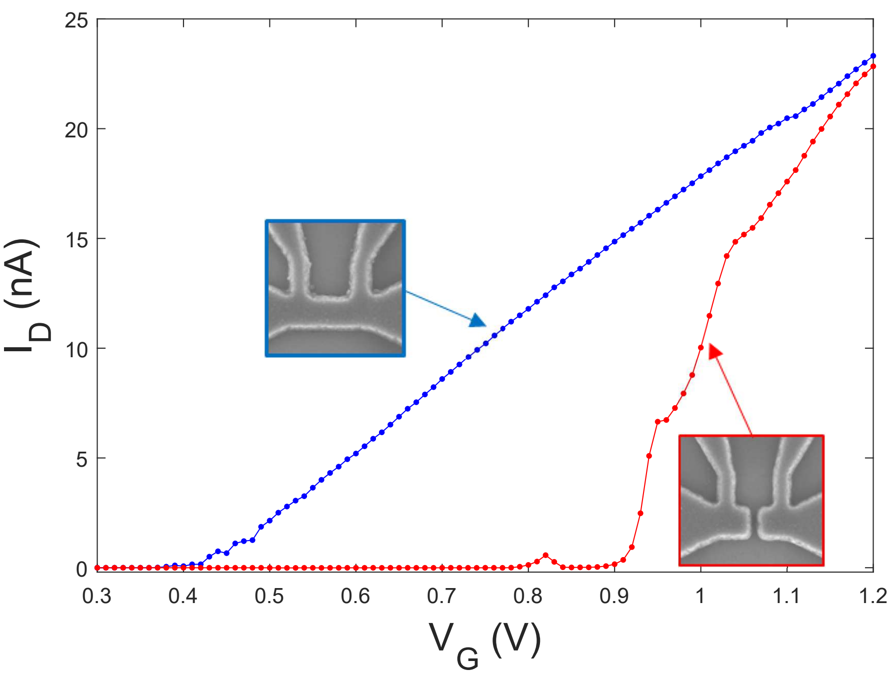

FIG. S2. $I(V_G)$ for titanium-gated devices at 2 K and $V_D = 1$ mV . The blue data is from a wire device with no gap in the gates and the red data is from tunnel junction device. The large gate voltage delay between the two devices is due the presence of the tunnel barrier.

After fabrication and initial tests at room temperature, tunnel barrier devices are cooled down to 2 K for electrical measurements. Using the different combinations of ohmics discussed in the main text, we measure turn-on for the leads on each side of the tunnel junction and turn-on through the junction. If the device does not have unintentional dots induced by disorder, strain, or some other mechanism the turn-on through the tunnel junction should be a smooth curve. A turn-on curve which shows strong spikes in the current (resonances) indicates a device with unintentional dots. All devices with significant resonances have been excluded from the results presented. A rough yield with respect to this quality is 25 %. An example satisfactory turn-on curve is shown in Fig. S2 for a titanium gated device. There we show turn-on behavior for a tunnel junction device (red curve) and a wire device (blue curve). The wire device is identical to the tunnel junction device but has no gap.

Device	Left V_t	Right V_t
Ti	0.52 ± 0.05	0.52 ± 0.05
Ti	0.60 ± 0.05	0.61 ± 0.05
Al	0.60 ± 0.06	0.62 ± 0.06
Al	0.62 ± 0.06	0.62 ± 0.06

TABLE S2. Left and right side threshold voltages used to produce the averaged threshold voltage for the data in Fig. 3 of the main text. The uncertainty on the threshold voltage represents a statistical uncertainty for a 95 % confidence interval from a linear fit of the $I(V_G)$ data.

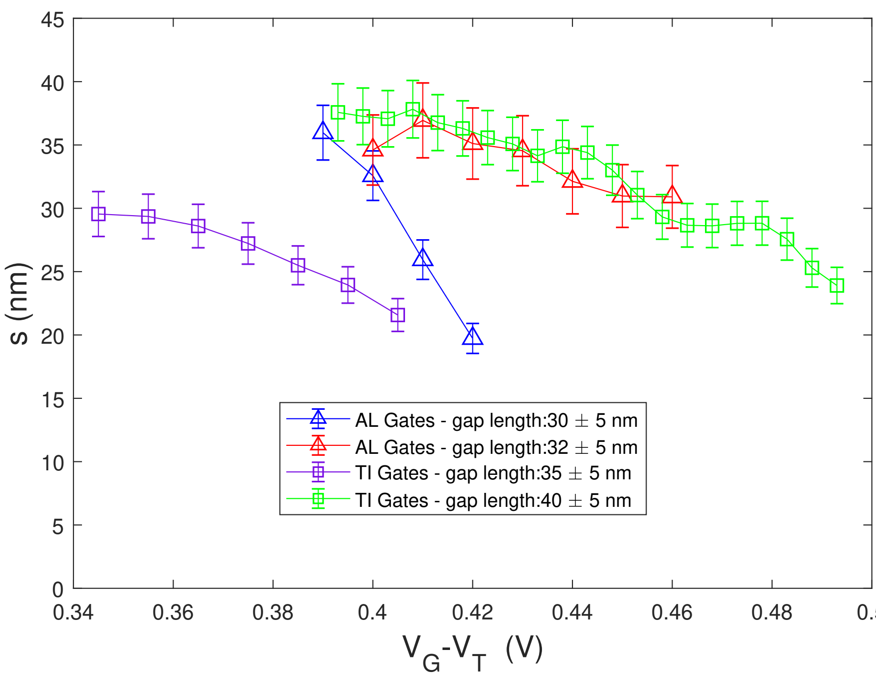

FIG. S3. Barrier widths, s, as determined from fitting to equation 3 of the main text and corresponding to the data presented in Figure 3 of main text.

As mentioned in the main text, in our model the barrier width, s, is a function of V_G, which we expect should decrease with increasing gate voltage due to fringing fields. This relationship is seen in all of the tunnel junction data shown, in Fig. S3. The barrier width

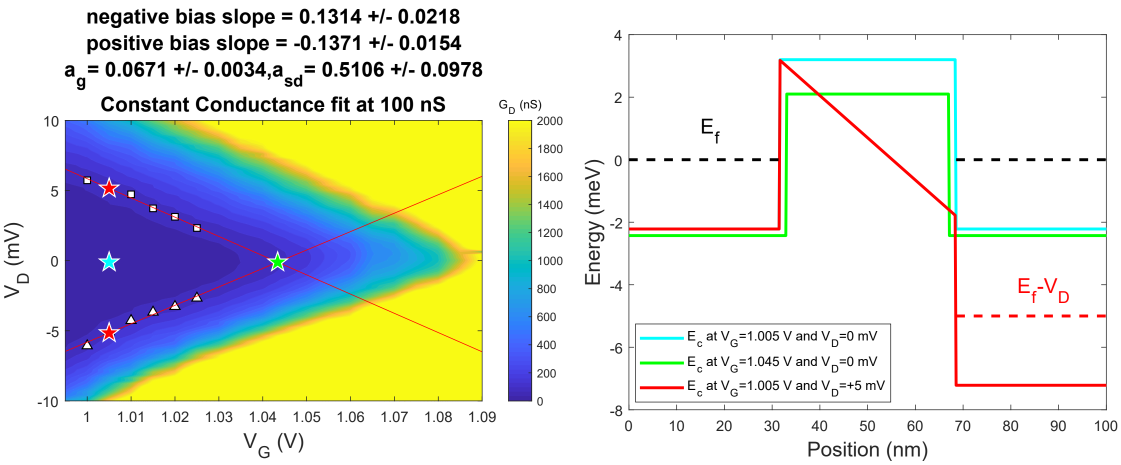

FIG. S4. (a) Determination of gate and source-drain lever arms from 2-dimensional conductance map for a titanium-gated device at 2 K based on the work in Ref S1. The red lines are a fit to constant conductance points (white squares) at 100 nS. The choice of the conductance value doesn't significantly impact the results for the slopes. (b) Trapezoidal barrier profile based on equation 3 of the main text and values for conductance in (a), where the color of the star corresponds to color of band profile ($E_{Fermi} = 0$). The band profile illustrates the qualitative difference in the tunneling between the case of a trapezoidal barrier (fits to equation 3 in the main text) and Fowler-Nordheim tunneling (2-d conductance data) which may impact our determination of β.

does not directly impact our measurement of strain but it serves as a consistency check for the electrostatic behavior of the tunnel junctions. The maximum $s(V_G)$ agrees well with the lithographic widths measured in a FE-SEM (dimensions listed in plot legend). We use devices in our analysis which show consistent behavior in the barrier parameters as a function of $V_G - V_T$. Here, this means we exclude the 30 nm wide Al device when extracting relative strain because the slope of the $s(V_G - V_T)$ deviates significantly from the others.

The linear model from Ref S1 was used in the main text to extract gate and source-drain lever arms from 2-d conductance maps for tunnel barrier devices. An example of one such set of conductance data and linear fits is shown in Fig. S4 (a) for a titanium gated device. The red and green stars occur at the same conductance $G(V_D) \approx 100$ nS. From Fig. S4 (b), it can be seen that for the trapezoidal barrier these two points represent qualitatively different physical pictures for the barrier. In the case of the green star, the transport is only via direct tunneling (since $V_D = 0$) with a width and height of 34.4 ± 2.1 nm and 2.1 ± 0.2 meV respectively. In the case of the red star, the barrier has tilted such that the right edge of the barrier has dropped below the Fermi level on the left side. This is known as Fowler-Nordheim tunneling and significantly decreases the effective width of the barrier.

The determination of β from 2D conductance plots corresponds to V_G and V_D on the line connecting the red and green stars. This line represents a change in both ϕ_{tot} and s such that the product $s\sqrt{\phi_{tot}}$ results in constant $G(V_D)$ over the range of V_G and V_D. In contrast, the determination of β from fits to equation 3 of the main text corresponds to $V_D = 0$ and V_G connecting the blue and green stars. Therefore, this line corresponds to the change in ϕ_{tot} purely due to V_G and a non-constant $s\sqrt{\phi_{tot}}$ product. These differing pictures likely limit the agreement of β as determined by these two methods in the main text.

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