Memory update characteristics of carbon nanotube memristors (NRAM®) under circuitry-relevant operation conditions

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***Abstract*— Carbon nanotubes (CNT) resistance-change memory devices were assessed for neuromorphic applications under high frequency use conditions by employing the ultra-short (100 ps -10 ns) voltage pulse technique. Under properly selected operation conditions, CNTs demonstrate switching characteristics promising for various NN implementations.**

***Index Terms*-- Neuromorphic computing, CNT, RRAM.**

I. INTRODUCTION

Mobile neuromorphic computing systems impart specific requirements to memristors for microelectronic "synapses". Carbon nanotube (CNT) nano-switch devices are a promising class of resistive memory technologies due to excellent retention and endurance, and low operating current. A CNT memory cell (Fig. 1) consists of TiN electrodes sandwiching a ~30 nm layer of a conductive fabric representing a disordered network where CNTs are bound to each other via van der Waals forces [1]. Rearrangements of the CNT contacts, Fig. 2, results in higher (~1-10 MΩ) and lower (~10-100 kΩ) cell resistance states. Due to asymmetry of the CNT fabric engineered by varying nanotubes density, orientations, doping, etc., an applied to the bottom electrode positive voltage increases a number of nanotubes connections resulting in higher cell conductance, while negative voltage decreasing conductance of a NRAM device.

To assess the suitability of CNT nano-switch technology for neural network applications, we investigate stability of NRAM responses to program signals under the conditions, which are close to high frequency circuitry operations. For that purpose, an ultra-short (100 ps -10 ns) voltage pulsed technique [2] was employed. Here we focus on deep neural network (DNN) applications where cell resistance (representing synaptic weight) is required to increase/decrease gradually and quasi-linearly depending on the polarity of the programming pulse [3]. To evaluate how synaptic weight is modulated by incoming signals, we investigated dependency of memristor resistance on pulse durations, voltages, and sequences of SET (program operation increasing conductivity) and ReSET (program operation decreasing conductivity) pulses.

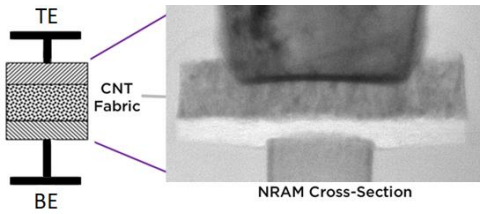

Figure 1. *SEM image of an NRAM cell.*

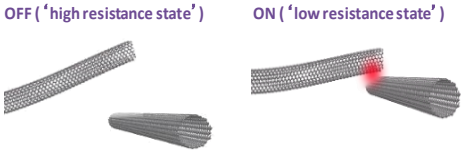

Figure 2. *Schematics of resistance switching between high and low resistance states on a single-point contact.*

II. EXPERIMENTAL SETUP

The ultra-short pulse (USP) technique [2,4-8] has several advantages over traditional memristor evaluation methods:

(i) Pulse duration are relevant to actual circuitry operating conditions, and allow realistic assessment of memristor characteristics;

(ii) Short pulses allow precise control of switching energy delivered to devices, which was shown to improve switching stability and reduce variability [2];

(iii) USVP removes the need for a current compliance circuitry because this technique delivers well-controlled small conductance changes.

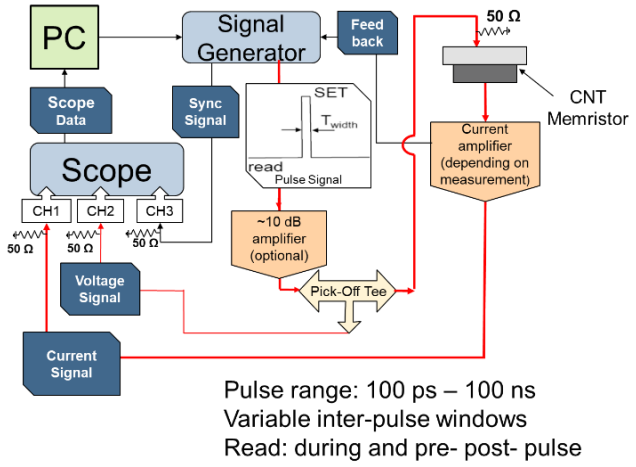

Figure 3. *Experimental setup.*

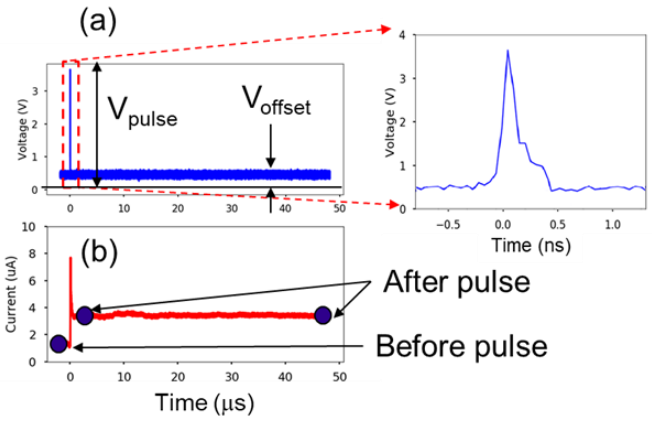

Figure 4. *Applied voltage pulse (a) and resulted current (b) through the NRAM cell, monitored using small DC offset. V_{offset} = 100 – 500 mV.*

Schematic of the experimental setup is shown in Fig. 3. Current through the memristors is monitored using a current amplifier and by applying a constant small DC offset (below the switching voltage threshold) coupled to the programing signals, Fig. 4. Pulses of positive (SET) or negative (ReSET) polarities change conductance to higher and lower values, respectively. Note that CNT memristor devices can operate in a wide conductance range: here we show data on the switching current in the 1 μA and 100 μA range.

III. Results and Discussion

To verify switching stability of NRAM devices, trains of 50 SET pulses followed by 50 ReSET pulses were applied. Pulse duration was fixed at T_{pulse} = 100 ps, and low (1 Hz) repetition rate was used to eliminate cross-correlation (energy-wise) between program pulses. The conductance response to short programing pulses is shown in Fig. 5a,b. both SET and ReSET operations include abrupt and gradual phases of strong and smaller conductance changes, respectively. The first pulse in the 50 SET pulses tends to induce a large conductance increase followed by smaller increases under subsequent pulses; conductance eventually saturates with minimal continuous increase. The current saturation value, $I_{SET,}$ linearly depends on the pulse amplitude, Fig. 6. ReSET typically features an initial gradual conductance decrease followed by an abrupt drop towards the target HRS. In subsequent SET/ReSET switching cycles (performed with sequences of multiple SET and ReSET pulses), stronger initial SETs correlate to larger final steep ReSET drops, Fig. 5c. This indicates that the same sites within the CNT fabric (connections between specific CNTs) control SET-ReSET switching steps: the inter-CNT contact which was activated first (e.g., easier to connect) is the last to be de-activated (harder to disconnect). These sites in the NRAM cell, which are responsible for the initial (SET) - final (ReSET) abrupt conductance changes may represent a cluster of connected CNTs in the film fabric: higher current through the contact in a single CNT pair may assist (via energy dissipation and temperature increase) with bending of surrounding CNTs and promoting contact. Indeed, higher SET voltage results in higher saturation current accompanied by a larger conductance change in both initial SET and final ReSET, Fig. 7 a, b. This is consistent with the proposed understanding that saturation is due to the fact that most (if not all) of available CNT sites capable to connect under a given condition are activated; higher voltage and longer pulse time (i.e. higher emitted energy) increases a pool of activatable sites that leads to both greater initial SET transition and a higher saturation level. To identify operation conditions contributing to conductance saturation in memory updates, we applied program pulses of various durations and variable sequences.

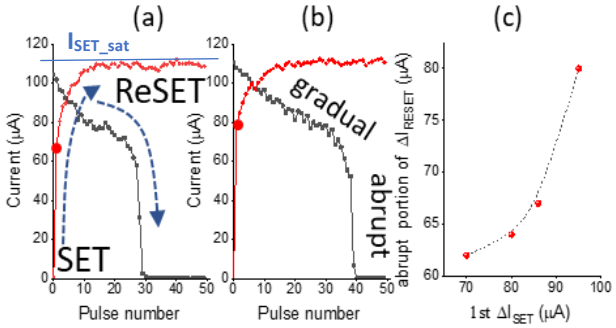

Figure 5. *(a,b) – Example of NMRAM cell response to 50 SET + 50 ReSET pulses in 10th and 20th switching cycles (T_{pulse} = 100 ps). Red circles indicate conductance increase after the 1st SET pulse; (c) correlation between abrupt SET/ReSET phases (multiple cycles on same device): intial SET and final ReSET.*

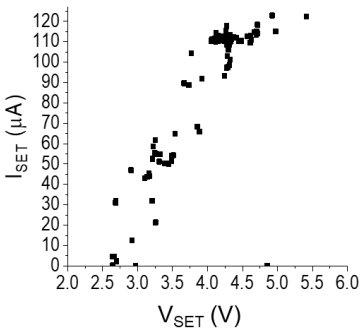

Figure 6. *LRS current after SET operation vs. amplitude of the SET pulse in multiple SET/ReSET cycles (on the same device).*

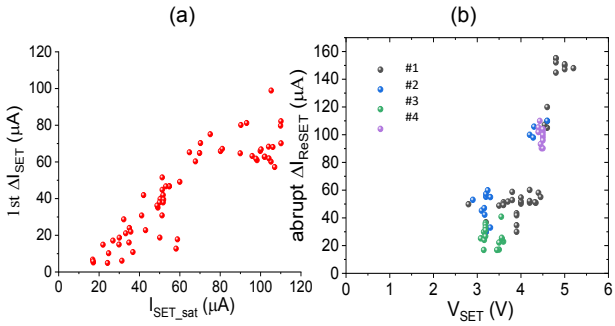

Figure 7. *(a) Correlation between ΔI after 1st SET pulse and saturated conductivity after 50 SET pulses. (b) Abrupt portion of the conductivity update in ReSET operation vs. amplitude of the preceeding train of SET pulses (data for 4 different samples are combined).*

Oscillograms of voltage and current through the NRAM device under 10 ns SET/ReSET pulses are shown in Figure 8. This relatively long voltage pulses of slow rise and fall times allow to directly measure a current during NRAM switching, thanks to low parasitic capacitance of tested devices. Collected data demonstrates strong SET/ReSET asymmetry, Figure 8 c,d. Comparison of switching characteristics of a single SET/ReSET pulse of 10 ns and a train of 5 Set/5 Reset pulses of 2 ns width (separated by 200 ns) further emphasizes the asymmetry between SET and ReSET processes, Fig. 9.

A longer ReSET pulse induces a runaway-like increase of the NRAM cell resistance. In SET, on the other hand, the conductance change is primarily determined by total duration of the applied voltage, either continuous (10 ns pulse) or interrupted (5 x 2 ns).

To assess the possible contribution of temperature increase, SET is performed by applying sequences of short or long pulses separated by a long time-window, Fig. 10. The sequence of 200 ps pulses demonstrates that conductance increase saturates within a short time (covering duration of several initial pulses) contrary to longer 2 ns pulses. This suggests that the energy released during the "short" pulse limits the size of the affected (heated) region of the CNT fabric that reduces possible CNT connections.

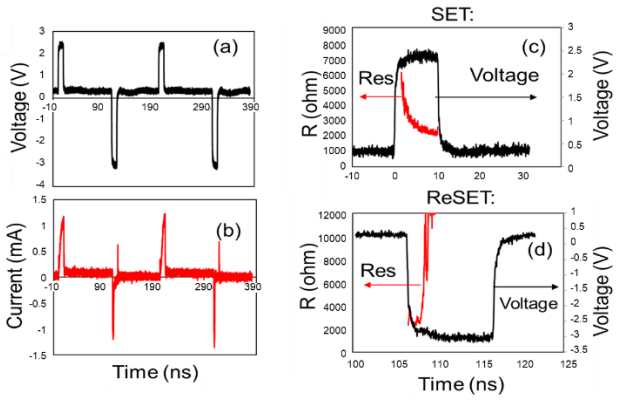

Figure 8. *Oscillograms of voltage (a) and current (b) under 10 ns SET/ReSET pulses; Resistance and voltage evolutions during individual pulses in SET (c) and ReSET (d) operations.*

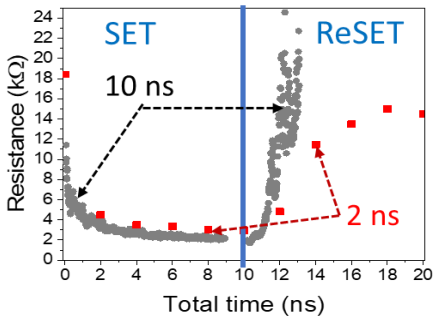

Figure 9. *Comparison of the resistance update in SET and ReSET operations during an applied train of five 2 ns pulses (red dots) and continuous single 10 ns pulse x-axis corresponds to the total time of applied pulse votage. RESET runaway in 10 ns pulse is observed.*

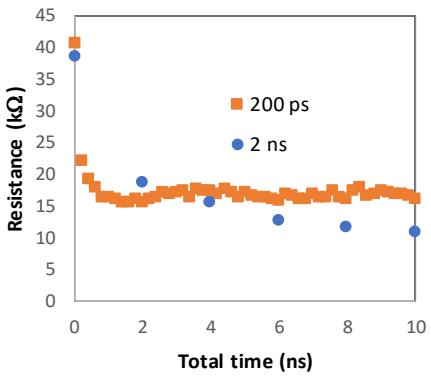

Figure 10. *Comparison of the resistance update in SET operations during applyed trains of five 2 ns pulses (circles) and fifty 200 ps pulses. X-axis corresponds to the total time of the applied pulse voltage.*

This understanding is verified by reducing the time window between the pulses, enabling heat buildup during the pulse sequence. SET cycles are performed by applying repeated pulse sequences of 5 pulses of 200 ps duration; each SET cycle had a specific inter-pulse time window, Fig. 11. The shortest inter-pulse time resulted in higher conductance increase within a given overall pulse cycle duration, while inter-pulse times longer than 200 ps had no effect (consistent with the longer

pulses in Fig. 10). This indicates that no heat build-up "around" the forming conductive paths occurred under longer pulses since the emitted energy had sufficient time to dissipate throughout the film. Thus, extremely short pulses (< 200 ps) restrict the SET process by limiting energy supply. This suggests that SET is likely associated with a growing number of CNT contacts gradually establishing a conductive CNT cluster under applied voltage. In ReSET, however, a longer pulse results in drastic resistance increase, Fig. 9, suggesting that a dissociation of CNTs contacts is assisted by the local temperature increase driven by energy released around the conductive paths.

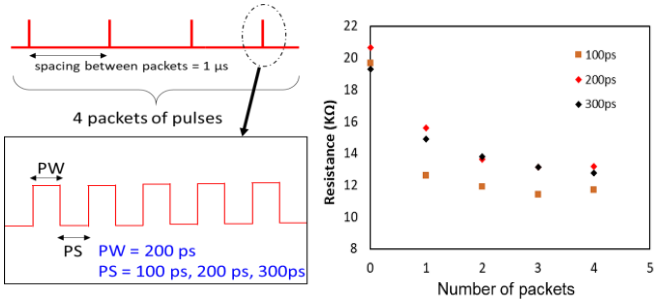

Figure 11. SET: *Resistance updates (r.h.s. graph) under four different pulse sets, each contains five 200 ps pulses. intervals between pulses (PS): 100ps, 200 ps, 300 ps (as marked in l.h.s. graph).*

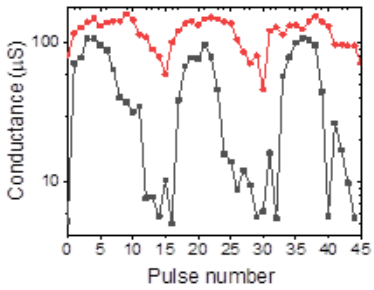

Figure 12. *Conductance switching under 400 ps SET/ReSET pulses Red curve: Vset = 2.5 V and Vreset = -2.4 V; black curve: Vset = 2.3 V Vreset = -2.0 V. . Switching stability and repeatability strongly depends on the pulse amplitude.*

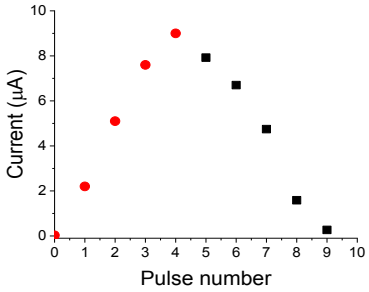

Figure 13. *Quasi-linear and symmetrical gradual conductance update achieved through optimization of switching conditions.*

I. CONCLUSION

Assessing device operations employing picosecond-range pulses is essential since characteristic time constants in both SET and ReSET processes are found to be on the order of a few hundred picoseconds. NRAM cell shows a stable switching characteristic under sequences of SET/ReSET pulses of 400 ps width at 200 ns intervals, Fig. 12, exhibiting higher resistance under lower pulse voltages. Under properly selected conditions, NRAM demonstrates symmetric quasi-linear memory updates, Fig. 13, making it a promising technology for DNN implementation. Future development of NRAM technology for neuromorphic applications may proceed with the focus on continuous improvements of switching stability and operational current range.

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