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DARPA Organic Interposer Characterization

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Abstract

We report on a study of interconnects fabricated on organic and silicon interposers used to connect state-of-the art digital, analog and RF chiplets commissioned by the U.S. Defense Advanced Research Projects Agency (DARPA). The interconnects were characterized with state-of-the-art on-wafer measurement methods developed at the National Institute of Standards and Technology (NIST) and then simulated with the Cadence® Sigrity™ simulation software package. The two-port, four-port and eight-port measurements and calibrations were performed to frequencies as high as 110 GHz using custom on-wafer calibrations to improve accuracy. We discuss the measurement and simulation methodologies and present detailed comparisons of the measurement and simulation results.

Commercial brand names are used only to better explain the experiments and analysis. The National Institute of Standards and Technology does not endorse commercial products. Other products may work as well or better.

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Biographies

Dylan F. Williams received a Ph.D. in Electrical Engineering from the University of California, Berkeley in 1986. He joined the Electromagnetic Fields Division of the National Institute of Standards and Technology in 1989 where he develops electrical waveform and microwave metrology. He has published over 80 technical papers and is a Fellow of the IEEE. He is the recipient of the Department of Commerce Bronze and Silver Medals, the Astin Measurement Science Award, two Electrical Engineering Laboratory's Outstanding Paper Awards, three Automatic RF Techniques Group (ARFTG) Best Paper Awards, the ARFTG Automated Measurements Technology Award, the IEEE Morris E. Leeds Award, the 2011 European Microwave Prize and the 2013 IEEE Joseph F. Keithley Award. Dylan also served as Editor of the IEEE Transactions on Microwave Theory and Techniques from 2006 to 2010 and as the Executive Editor of the IEEE Transactions on Terahertz Science and Technology.

Richard A. Chamberlin graduated from the University of California (Santa Barbara, CA) with a B.S. in physics in 1984, and obtained his Ph.D. in physics from the Massachusetts Institute of Technology (Cambridge, MA) in 1991. In 1995 he was the first winter-over scientist with the pioneering Antarctic Submillimeter Telescope and Remote Observatory which he helped design, build, and test while at Boston University. From 1996 to 2010 he was the Technical Manager of the Caltech Submillimeter Observatory located on the summit of Mauna Kea on the Island of Hawaii. Currently he is working in the High Speed Electronics Group at the National Institute of Standards and Technology in Boulder, Colorado.

Jerome Cheron received the Ph.D. degree in electrical engineering from the University of Limoges, France, in 2011. His research project was led at XLIM laboratory and Thales Air Systems, France. In 2012, he was Postdoctoral Fellow with the Fraunhofer IAF, Freiburg, Germany. In 2013, he joined NIST in Boulder, Colorado. His research interests include the design and optimization of microwave and millimeter-wave circuits in III-V technology.

Brent DeVetter received his Ph.D. in Electrical Engineering with a focus on plasmonic materials from the University of Illinois at Urbana-Champaign in 2016. He was a postdoctoral researcher at NIST working in the High-Speed Electronics Group performing high frequency measurements and electromagnetic simulations. He also completed a postdoctoral appointment at the Pacific Northwest National Laboratory focusing on infrared and terahertz spectroscopy of crystalline materials.

Sam Chitwood has focused on signal and power integrity analysis for 17 years. He has been a product engineer at Cadence Design Systems and an application engineer with Sigrity. He contributed to the DARPA CHIPS project through October 2019 while at Cadence. He has BSEE and MSECE degrees from Georgia Institute of Technology.

Ken Willis is a Product Engineering Group Director focusing on system-level analysis solutions at Cadence Design Systems. He has over 30 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, technical marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

Brad Butler is a Senior Application Engineer at Cadence Design Systems, focused on enabling advanced electronic systems design in the Aerospace and Defense sector. Prior to joining Cadence, he worked on vehicle dynamics, autonomous driving, and LIDAR applications at a small automotive startup. Brad earned B.S. degrees in Mechanical Engineering and Economics from North Carolina State University.

Farhang Yazdani is the President and CEO of BroadPak Corporation. Through his 20 years with the industry, he has served in various technical, management, and advisory positions with leading semiconductor companies worldwide. He is the author of the book "Foundations of Heterogeneous Integration: An Industry-Based, 2.5D/3D Pathfinding and Co-Design Approach". He is the recipient of 2013 NIPSIA award in recognition of his contribution to the advancement and innovations in packaging technologies. He has numerous publications and IPs in the area of 2.5D/3D Packaging and Assembly, serves on various technical committees and is a frequent reviewer for IEEE Journal of Advanced Packaging. He received his undergraduate and graduate degrees in Chemical Engineering and Mechanical Engineering from the University of Washington, Seattle.

I. Introduction

Large, monolithic ICs are being replaced by arrays of chiplets mounted on advanced interposers (passive integrated circuits supporting complex interconnects between the die mounted on them) in wide ranging applications of our industry. A few high-profile examples are Intel's "Foveros" and EMIB interposers [1, 2] and AMD's latest Ryzen processors [3, 4]. Chiplet-to-chiplet interconnects with micron and sub-micron widths pose new design, analysis and implementation challenges for digital and analog designers.

DARPA has supported work in heterogenous integration at RF frequencies though the Diverse Accessible Heterogeneous Integration (DAHI) Program [5-9] and this has helped lead a larger push for heterogenous integration at higher frequencies [10]. The National Institute of Standards and Technologies (NIST) performed work under this program characterizing heterogenous interconnects between several different technologies [11].

More recently DARPA has expanded this thrust to digital and analog integrated circuits with the Common Heterogeneous Integration and IP Reuse Strategies (CHIPS) Program [12, 13] under which this work was performed. In this paper, we report on a study of interconnects fabricated on build-up and silicon interposers used to connect state-of-the art digital, analog and RF chiplets supported by this program.

The study performed under the DARPA CHIPS Program focused on two interconnect types, an organic interposer supporting an Ajinomoto GX-92 build-up film (ABF) interconnect [14] covered with Hitachi SR7300 solder resist [15] and an inorganic silicon interposer with through-substrate vias (TSVs) supporting a silicon-dioxide (SiO_2) thin-film interconnect. The organic interposer provides an inexpensive but high-performance solution for integrating chiplets while the inorganic silicon interposer represents the state-of-the-art in interposer technologies. The interposers, and the calibration kits and test structures required to accurately characterize them, were designed and fabricated under the program for the purpose of obtaining the most accurate technology characterization possible to frequencies up to 110 GHz.

The goal of this paper is to study the accuracy of the Cadence® Sigrity™ simulation software package, which includes an efficient hybrid solver for efficient S-parameter extraction of large interconnect structures and a slower but more accurate full-wave solver for more complicated 3-D structures. We first performed the simulations of the test structures on the interposer with the Sigrity hybrid solver using dimensional and other measurements performed by the manufacturer. Then, we compared the measurement and hybrid-solver simulation results and assessed the ability of the hybrid solver to predict interconnect performance in the two technologies we studied. Finally, in cases where we observed significant disagreement, we re-ran the simulations using the Sigrity full-wave solver. This allowed us to better assess when the faster hybrid solver was sufficient and when the slower but more accurate full-wave solver was needed.

II. Measurements

Most on-wafer measurements are calibrated with an "impedance-standard substrate" fabricated by the probe manufacturer. These are usually referred to as "probe-tip" calibrations. Probe-tip calibrations are performed under the assumption that the interaction between the probe tips and the contact pads on the wafer can be safely ignored. This is generally the case at lower microwave frequencies. However, the electrical parasitics associated with the interaction between the probe tips, contact pads, and even the device under test, increase roughly linearly with frequency [16-18]. For example, the admittance associated with the capacitance of the contact pads used to connect to a device will typically increase linearly with the frequency, causing measurement errors to increase with frequency as well [16-18]. There are more subtle errors introduced into probe-tip calibrations as well. For example, the inductance associated with a short bar printed on an impedance-standard substrate increases with the probe pitch, making it difficult to define the impedance of the short fabricated on the impedance-standard substrate. As the errors introduced into the calibrations are smooth and roughly linear, these errors are often not immediately apparent, but can nevertheless grow quite large at higher frequencies. For these reasons, the most accurate microwave calibrations are performed in transmission lines.

II.1. The Thru-Reflect-Line Calibration

The goal of a probe-tip calibration is to place the calibration and measurement reference planes at the tips of the probes, again with the assumption that the electrical parasitics associated with the interaction of the probe tips, contact pads and device under test can be ignored. The goal of an on-wafer thru-reflect-line (TRL) calibration, on the other hand, is to place the calibration and measurement reference planes in a transmission line fabricated on an integrated circuit or interconnect. In this environment, voltages, currents, scattering parameters and other electrical quantities can be rigorously defined (and measured) even at microwave frequencies [19-23], something that cannot be said of probe-tip calibrations. Furthermore, the result of cascading devices at these reference planes can be predicted with rigor from measurements performed at these reference planes [19]. Finally, the calibration and measurement reference plane can be moved to very close to the device under test, eliminating many parasitics in the measurement of the device. This generally proves more effective than conventional parasitic-extraction techniques used in transistor modeling, for example, as parasitics are first minimized before being estimated [24, 25].

An on-wafer microstrip TRL calibration kit fabricated in the interconnect stack of a silicon die is illustrated in Fig. 1 below. The TRL calibration kit includes a short "thru" line between the port 1 and port 2 contact pads, a number of longer lines, and a symmetric reflect (usually a short section of transmission line on each port terminated with an electrical open or an electrical short). These calibration standards are enough to perform a calibration in the transmission lines with a reference plane at the center of the thru line [19, 23].

Figure 2 illustrates the standards, their definitions (*i.e.* their properties), and their functions in the TRL calibration. The thru sets most of the calibration coefficients. The

symmetric reflect allows the calibration to set the reference plane in the center of the thru. The lines set the reference impedance of the calibration to the characteristic impedance Z_0 of the transmission line and provide a measurement of the propagation constant γ of the transmission line.

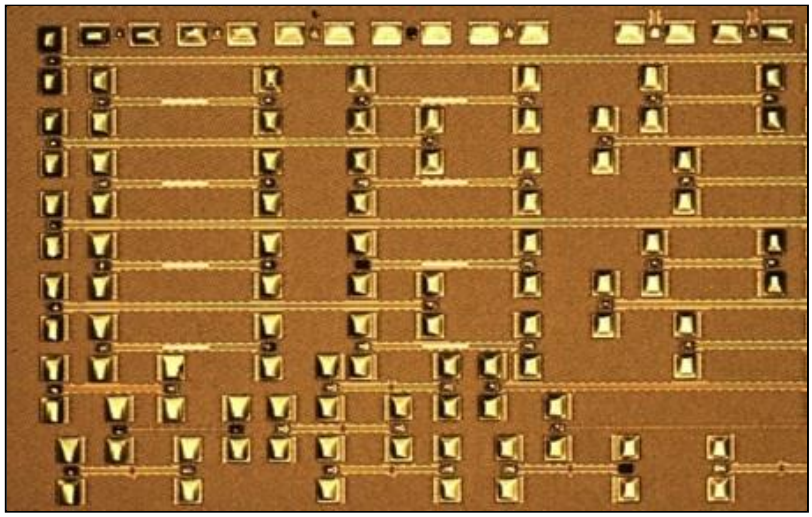


Figure 1. TRL calibration kit fabricated on a silicon die.

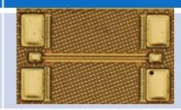
Standard		Definition	Function
Thru		$S_{21}=S_{12}=1$ $S_{11}=S_{22}=0$	Set most of the calibration coefficients
Reflect		$S_{11}=S_{22}$	Set reference plane position
Line		$S_{11}=S_{22}=0$ $S_{21}=S_{12}$	Set reference impedance to Z_0 Measure γ

Table 1. TRL calibration standards.

II.2. SiO_2 Transmission-Line Characteristic Impedance

Calibrations with a reference impedance equal to the characteristic impedance of a transmission line are not usually very useful, as the characteristic impedance is generally complex and frequency dependent [23]. Thus, the next step of the TRL calibration is to determine the characteristic impedance of the calibration.

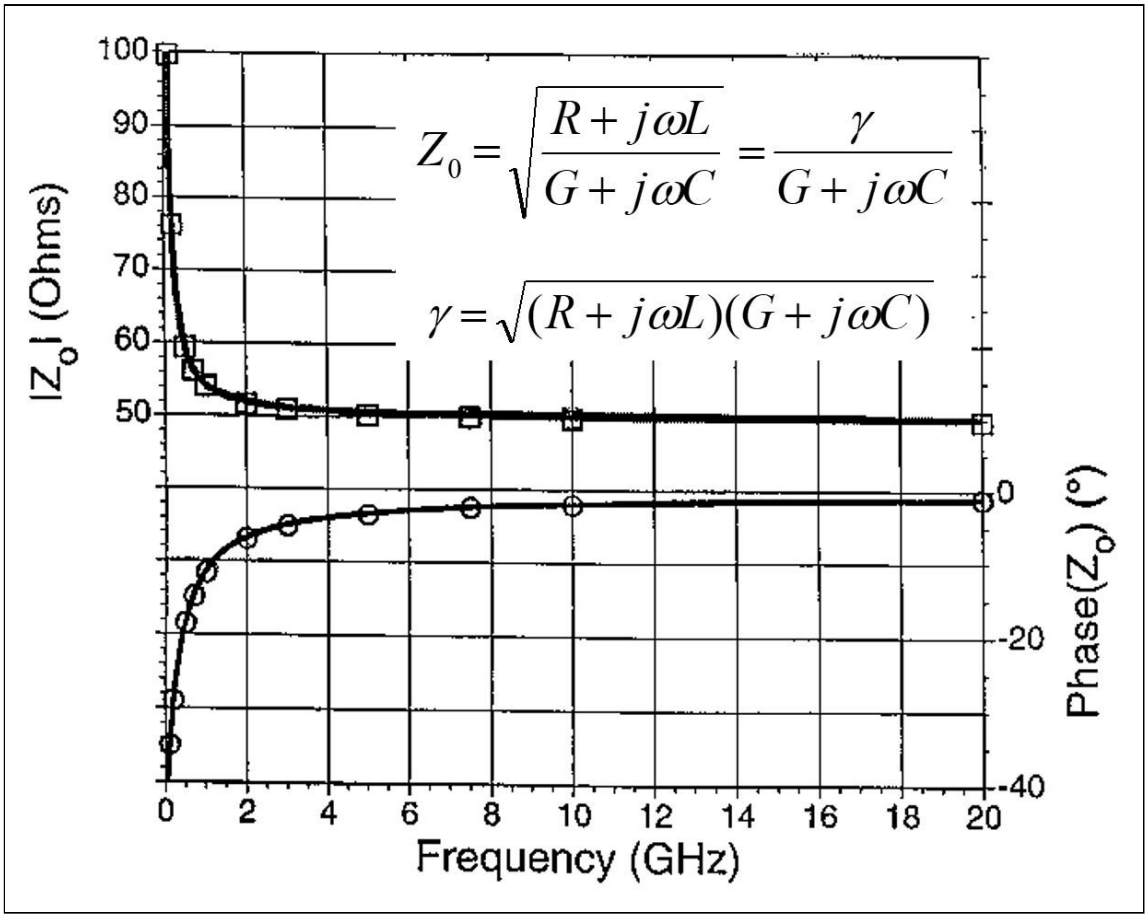


Figure 2. Measurement of the characteristic impedance Z_0 of a coplanar waveguide transmission line compared to calculation. The measurements are shown in solid lines. The calculated magnitude of Z_0 is shown in squares and the calculated phase of Z_0 is shown in circles. The formulas in the upper right were used to calculate Z_0. From [27].

We had two interconnect types to consider, the organic interconnect fabricated on a woven fiberglass core and the inorganic SiO_2 interconnect fabricated on a bulk silicon interposer. The SiO_2 has a roughly frequency-independent dielectric constant and a small loss tangent while the electrical behavior of the organic ABF is complicated by low-frequency dielectric relaxation. With this in mind, we start with the more straightforward analysis of the characteristic impedance of the microstip and stripline transmission lines fabricated in the SiO_2 interconnects.

Finding the characteristic impedance is quite straight forward in quasi-TEM transmission lines constructed from low-loss dielectrics, as the per-unit-length capacitance of the transmission line is very nearly frequency independent and the per-unit-length conductance of the transmission line is small. In this case, the capacitance of the transmission line can be determined from the measurement of a small resistor or the measurement of the per-unit-length DC resistance of the line and knowledge of the propagation constant γ estimated by the TRL calibration algorithm [26]. For these quasi-TEM lines fabricated on well-behaved dielectrics, the per-unit-length capacitance of the lines can even be easily determined by field solvers [26].

Once the per-unit-length capacitance C of the quasi-TEM transmission line has been determined, the characteristic impedance of the transmission line can be determined from the formulas in the upper-right of Fig. 2 [27]. In essence, the per-unit-length capacitance C and conductance G and the propagation constant γ of the transmission line are enough to determine the per-unit-length resistance R and inductance L of the transmission line. Once R and L have been determined, everything is known about the line, and the characteristic impedance Z_0 of the transmission line can be calculated directly with the upper formula in Fig. 2.

Figure 2 compares measurements (solid lines) of the magnitude and phase of the characteristic impedance Z_0 of a coplanar waveguide line to simulations (squares and circles) calculated with the full-wave method of [28], which includes field penetration into the metal in a rigorous way. As can be seen from the figure, the agreement is excellent. We used this approach to determine the dielectric constant of the microstrip and stripline transmission lines we used in our TRL calibrations on the SiO_2 interconnects fabricated on the bulk silicon. We determined the per-unit-length capacitance of the transmission lines from measurements of a small resistors fabricated in the interconnects, as described in [26].

II.3. ABF Transmission-Line Characteristic Impedance

The approach to determining the capacitance and conductance of transmission lines fabricated on low-loss inorganic dielectrics described in the last section cannot account for low-frequency transmission-line behavior due to dielectric relaxation. Therefore, the approach described in the last section is not applicable to the microstrip and stripline transmission lines we fabricated on the organic ABF interconnects. Instead, we first estimated the frequency-dependent dielectric constant and loss tangent of the ABF and then estimated the capacitance and conductance of the ABF transmission lines from their dimensions. Finally, we used capacitive parallel-plate test structures to check our result.

We estimated the frequency-dependent dielectric constant and loss tangent of the ABF from measurements of the ABF film performed at 1 GHz by the manufacturer and the low frequency and high frequency limits of the dielectric constant. We then applied the Djordjevic-Sarkar algorithm to extract a dielectric-relaxation model [29]. This model was independently suggested by Svensson in [30]. Figures 3 and 4 on the next page compare the extracted model to the measurements provided by the manufacturer.

We then estimated the capacitance and conductance of the ABF transmission lines from the model for the dielectric constant we determined and from the dimensions of the transmission lines provided by the manufacturer. This was enough to estimate the characteristic impedance Z_0 of the ABF transmission lines using the formulas in Fig. 2.

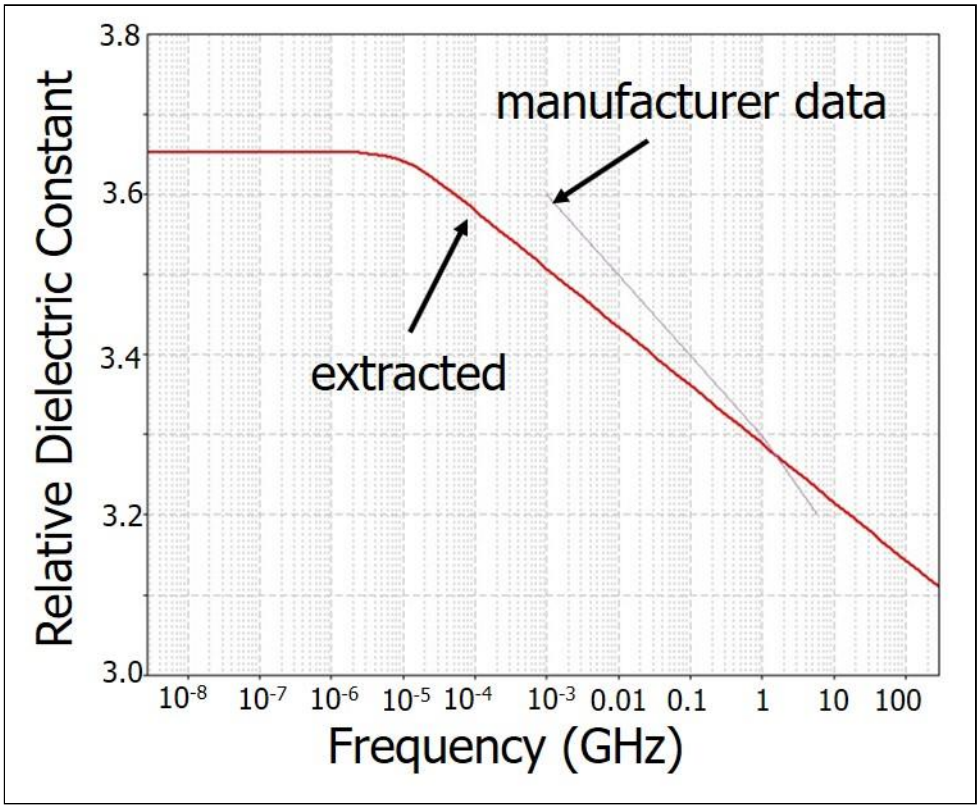


Figure 3. Comparison of the extracted relative dielectric constant and the measurements provided by the ABF manufacturer.

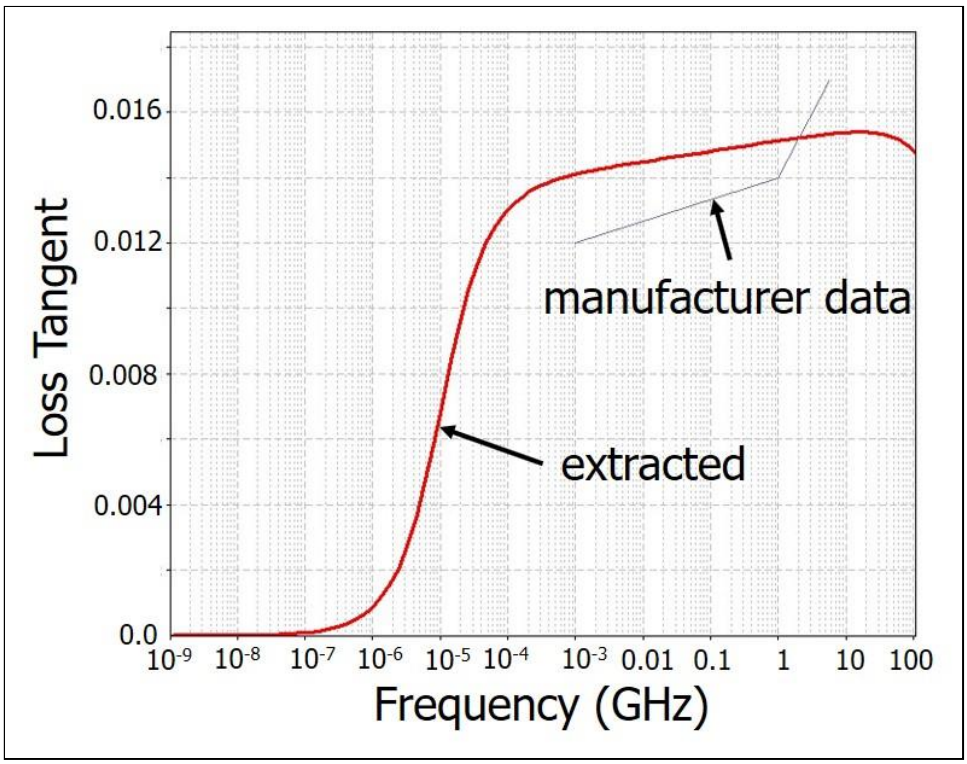


Figure 4. Comparison of the extracted loss tangent and the measurements provided by the ABF manufacturer.

Finally, we verified the dielectric constants and loss tangent we extracted for the organic ABF with large parallel-plate capacitors similar to those routinely created in the power distribution network of the interconnect. The positive plate of each capacitor was sandwiched between an upper and lower ground plate in the interconnect stackup. The two ground plates were stitched together periodically with vias that passed through small holes in the positive plate of the capacitor. We also used via stacks to connect the capacitor's positive plate and the two ground plates to contact pads on the top surface of the interconnect stackup with vias.

To test the capacitors, we first performed a TRL calibration on a fused silica wafer and moved the reference plane of the calibration back to the probe tips. A comparison of the measured and simulated magnitudes of the impedance of the capacitor at the measurement reference plane on the top surface of the ABF interconnect is shown in Fig. 5. While the calibration and extraction approach were both somewhat approximate, they clearly proved adequate for this purpose.

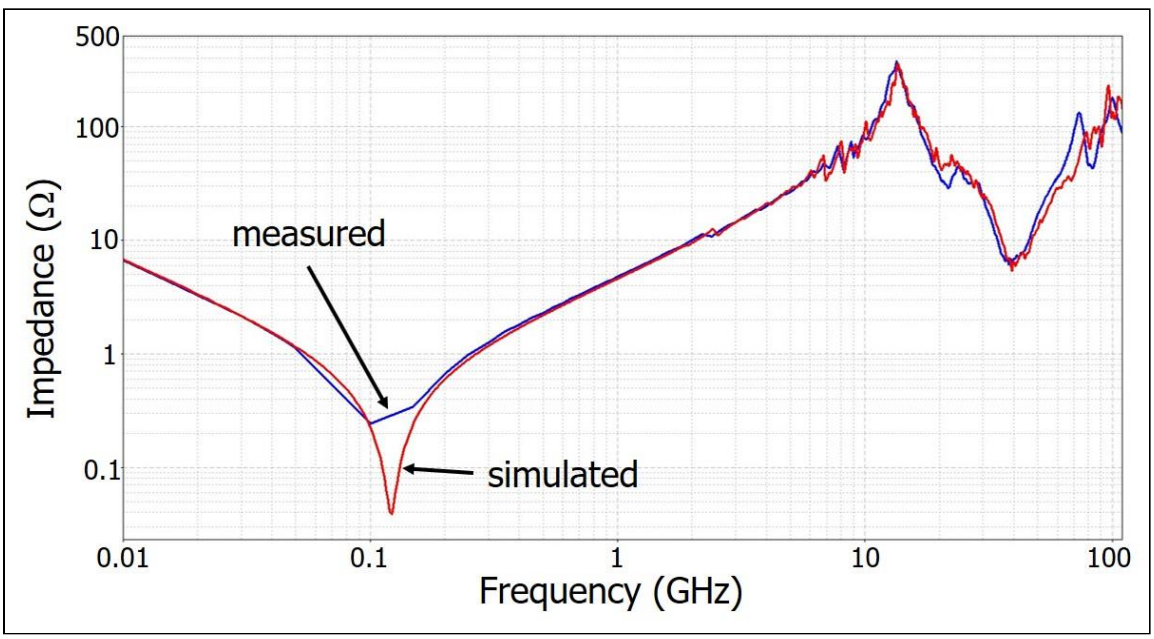


Figure 5. The measured and simulated impedances of one of the parallel-plate capacitors we used to verify extraction procedure we used, as implemented in the Cadence Sigrity software package.

III. Correlation Between Measurements and Simulations

We performed hundreds of TRL measurements and Sigrity hybrid-solver and full-wave solver simulations of test structures fabricated on the organic and silicon interposers and carefully examined the correlation between measurement and simulation. In most cases we were able to perform five or more independent calibrations and measurements of each test structure on different die, which allowed us to gauge the degree of correlation we obtained with the TRL measurements and Sigrity simulations. Here we present a few of these results on the organic ABF interposer performed with the Sigrity hybrid solver to illustrate the high degree of correlation we found between the two.

III.1. Coupled Lines on Organic ABF Interposer

Figure 6 below shows the layout of the organic ABF interposer. The design included microstrip and stripline TRL calibration kits shown in the upper and right-most sections of the layout, as well as a number of 2-port, four-port and eight-port test structures on other parts of the designs. Only the microstrip test structures fabricated in the top-metal levels are visible, but many more stripline test structures are buried in the interconnect stack and were also available for test.

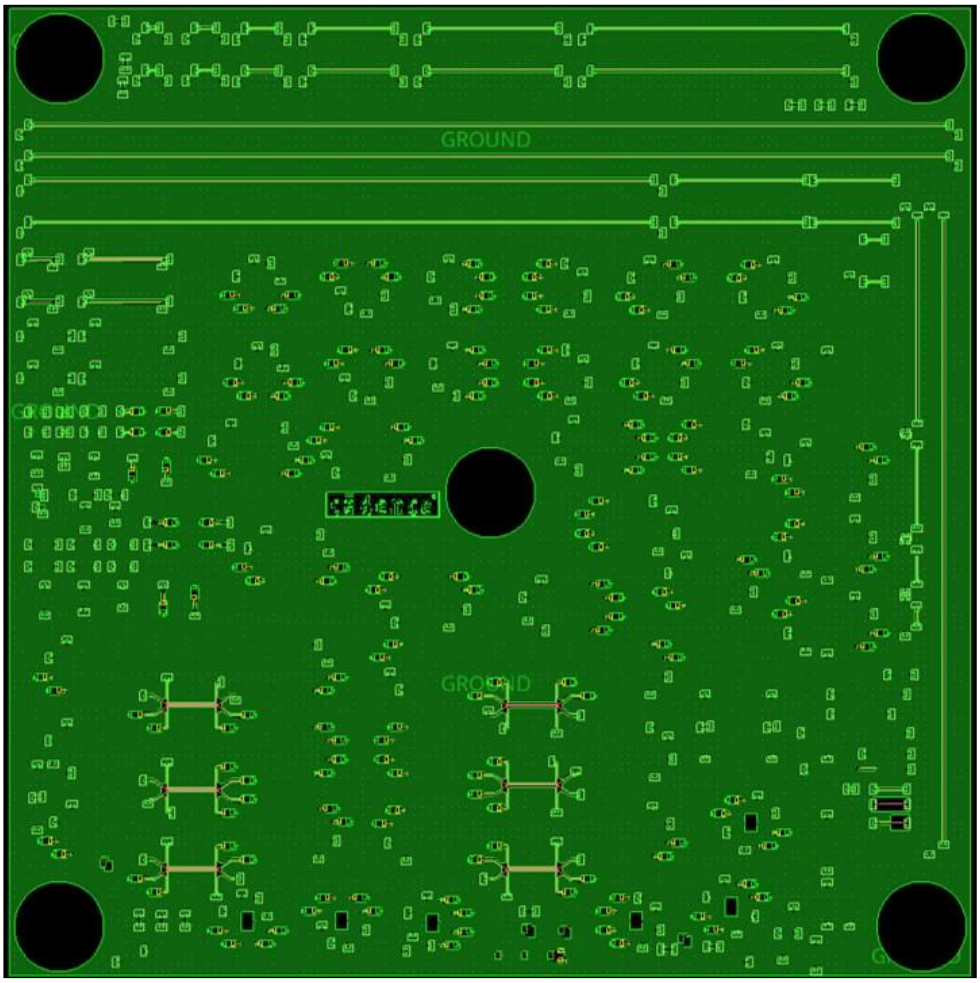


Figure 6. Top layer of the organic ABF Interposer layout.

Table 2 shows the twelve-metal ABF interposer stackup. The first column in the table lists the layer names and materials, the second column lists the layer thicknesses measured by the manufacturer and the last column lists the manufacturer's specifications. The photos in the right of the figure are of actual cross sections of the interposers we designed and tested.

Dimension	Measured (μm)	Specification (μm)
FSR Thickness	25.4	21±7.5
L1 Cu Thickness	16.2	15±5
L1-2 ABF Thickness	34.5	30±6
L2 Cu Thickness	17.3	15±5
L2-3 ABF Thickness	32.5	30±6
L3 Cu Thickness	17.3	15±5
L3-4 ABF Thickness	34.5	30±6
L4 Cu Thickness	18.3	15±5
L4-5 ABF thickness	33.5	30±6
L5 Cu Thickness	19.3	15±5
L5-6 ABF thickness	34.5	30±6
L6 Cu Thickness	25.4	25±7
Core thickness	821.3	820±80
L7 Cu Thickness	25.4	25±7
L7-8 ABF Thickness	32.5	30±6
L8 Cu Thickness	19.3	15±5
L8-9 ABF Thickness	31.5	30±6
L9 Cu Thickness	19.3	15±5
L9-10 ABF Thickness	32.5	30±6
L10 Cu Thickness	19.3	15±5
L10-11 ABF thickness	34.5	30±6
L11 Cu Thickness	18.3	15±5
L11-12 ABF thickness	34.5	30±6
L12 Cu Thickness	17.3	15±5
BSR Thickness	19.3	21±7.5

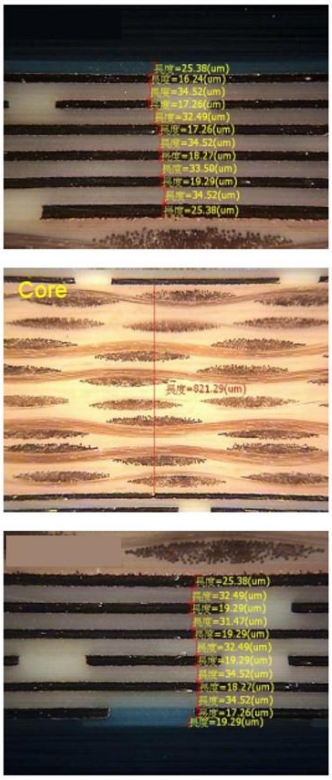


Table 2. ABF interposer stackup with measured layer thicknesses, specifications and cross sections. FSR = front-side solder resist, L*n* = metal layer *n*, L*n*-*m* = ABF layer thickness between L*n* and L*m*, BSR = back-side solder.

Table 2 shows some additional cross sections and width measurements performed by the manufacturer. As can be seen in the tables in Tables 2 and 3, the tolerances on the dimensional specifications were quite large and many of the measured transverse dimensions differed significantly from the nominal specifications. Because of the large variations in manufactured line width and no way to measure physical line widths for specific signals under test, this parameter was used as a "tuning parameter" in simulations. That is, with all other material and geometry parameters held constant, the line width was varied across the tolerance to observe the best match against the measured results. We optimized all of the simulated results we will present below in this way.

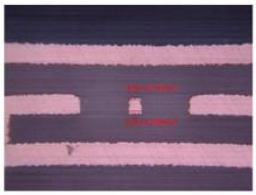
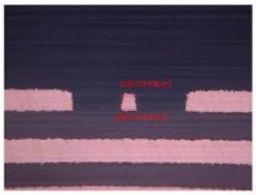
Layer	Specification (μm)	Measured (μm)	X-section
L3	12±5	12.2um	
L2	9±5	12.6um	
L1	9±5	10.2um	
L1	12±5	14.0um	

Table 3. Trace widths for selected structures fabricated on the ABF interposers. Spec = designed width for selected structure. X-section data = measured width for selected structure.

Correlations between the 2-port, 4-port and 8-port test structures we designed and tested, and simulations performed with the Sigrity hybrid solver (the faster of the two Sigrity solvers), were generally excellent. We present data here only for a single four-port and a single eight-port device.

III.2. Four-Port Coupled Lines on Organic ABF Interposer

Figure 7 shows the 4-port layout we used to assess measurement and simulations of coupled microstrip and striplines. We used the NIST Microwave Uncertainty Framework [31] to perform the four-port calibrations. This software package allows a lateral "east-west" two-port TRL calibration and a vertical "north-south" two-port TRL calibration to be combined with the use of an additional unknown bend to form a rigorous four-port calibration. We also took advantage of the Uncertainty Framework to move the calibration and measurement reference planes through the microstrip lines and vias, placing them in the striplines where the coupled structures buried in the ABF interconnect stack began and ended. We did not take advantage of the ability of this software package to evaluate measurement uncertainty in this work.

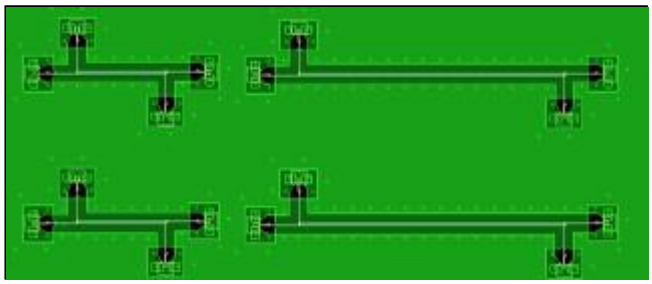


Figure 7. 4-port coupled-line layout.

The following figures illustrate the high-degree of correlation we observed between measurements and simulations performed on two coupled 9 µm wide 1 mm long coupled striplines spaced 9 µm apart apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines.

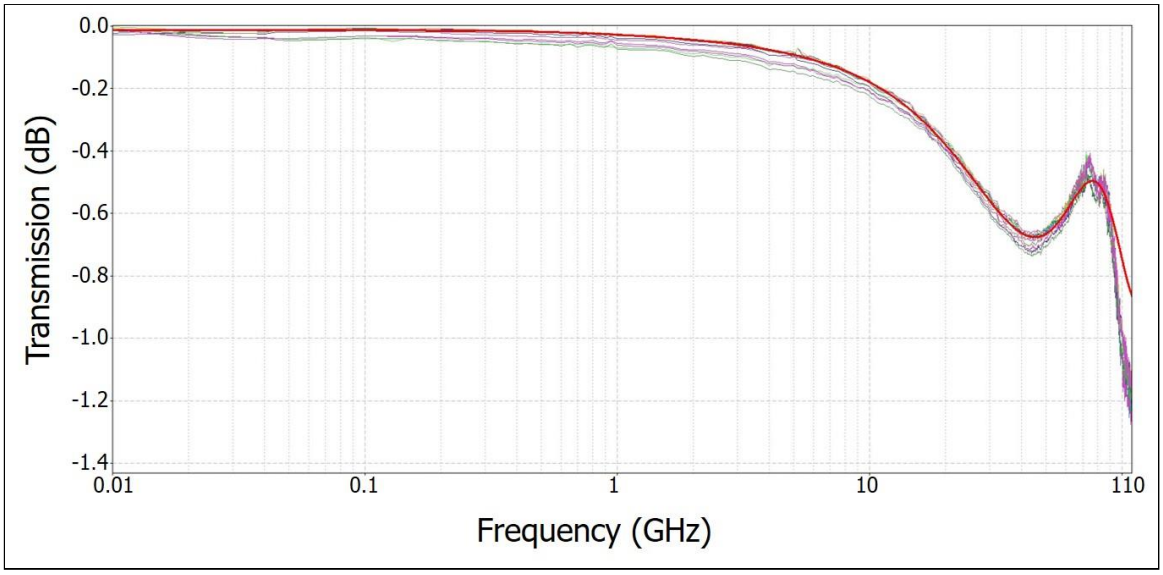


Figure 8. Transmission coefficient through a single 9 µm wide and 1 mm long stripline coupled to an adjacent line 9 µm apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation.

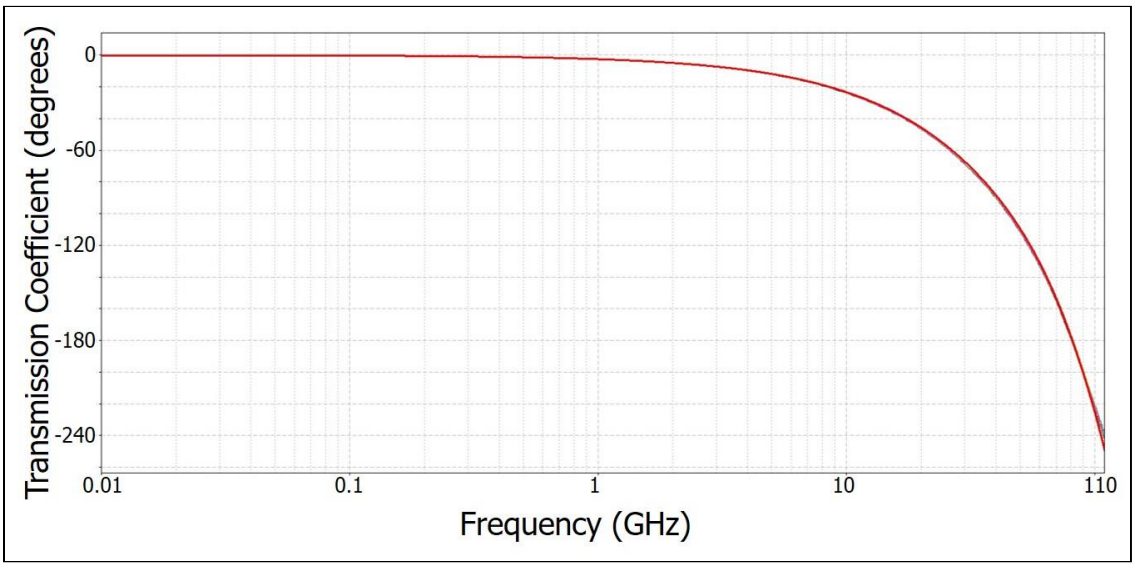


Figure 9. Phase of the transmission coefficient through a single 9 µm wide and 1 mm long stripline coupled to an adjacent line 9 µm apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation. (Deviations of measurements are too small to be seen.)

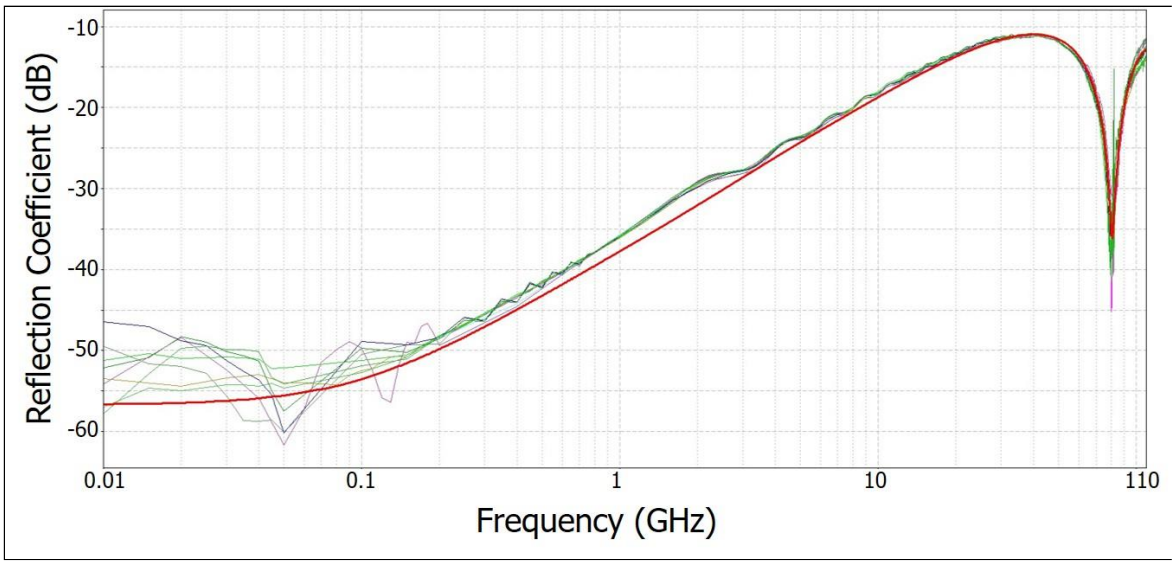


Figure 10. Reflection coefficient of a single 9 µm wide and 1 mm long stripline coupled to an adjacent line 9 µm apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation.

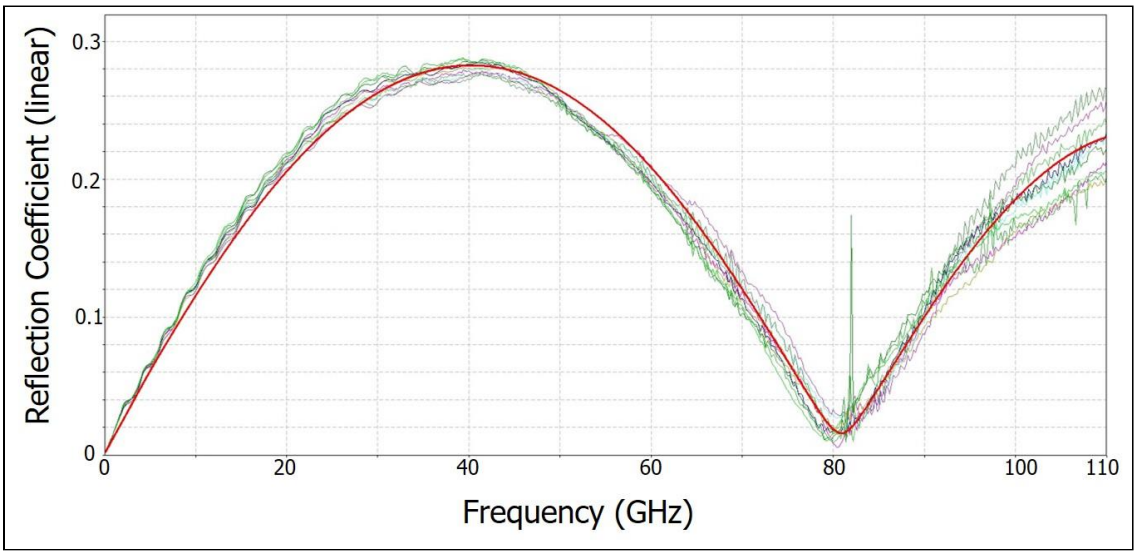


Figure 11. Reflection coefficient of a single 9 µm wide and 1 mm long stripline coupled to an adjacent line 9 µm apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines. We do not believe that there is any significance to the isolated spike in the measurements at 82 GHz. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation.

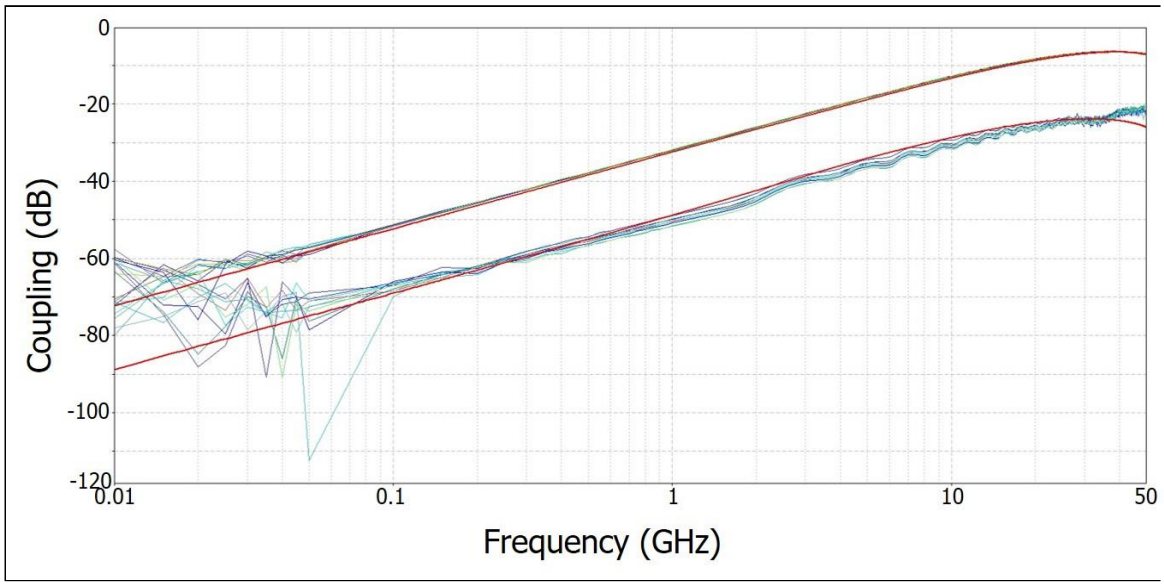


Figure 12. Near-end and far-end coupling between two 9 µm wide and 1 mm long striplines spaced 9 µm apart and buried in the third level of metal in the ABF interconnect stack. Simulations are shown in thick solid lines and measurements performed on other die are shown in thinner lines. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation. The hybrid solver was used for the simulations and only the line width was adjusted in the simulation.

III.3. Eight-Port Coupled Lines on Organic ABF Interposer

Figure 13 shows layouts for two 8-port coupled lines of different lengths. As we did not have access to an 8-port vector network analyzer, we fabricated six versions of each 8-port test structure and connected four of the ports to probe contact pads and terminated the remaining four ports with 50 Ω chip resistors soldered to contact pads on the top of the ABF interposer. These six versions of the 8-port test structures were designed so as to allow us to measure each of the elements of the 8 by 8 scattering-parameter matrix of the coupled lines.

Then we used our four-port analyzer calibrated to a reference plane where the eight-port coupled lines begin and end to measure the various scattering parameters of each of the six test structures. Finally, after compensating for the measured impedances of the chip resistors, we extracted the eight-port scattering parameters of the coupled lines using the Microwave Uncertainty Framework with an algorithm similar to those of [32, 33], except based on a regression fit rather than multiport impedance transformations.

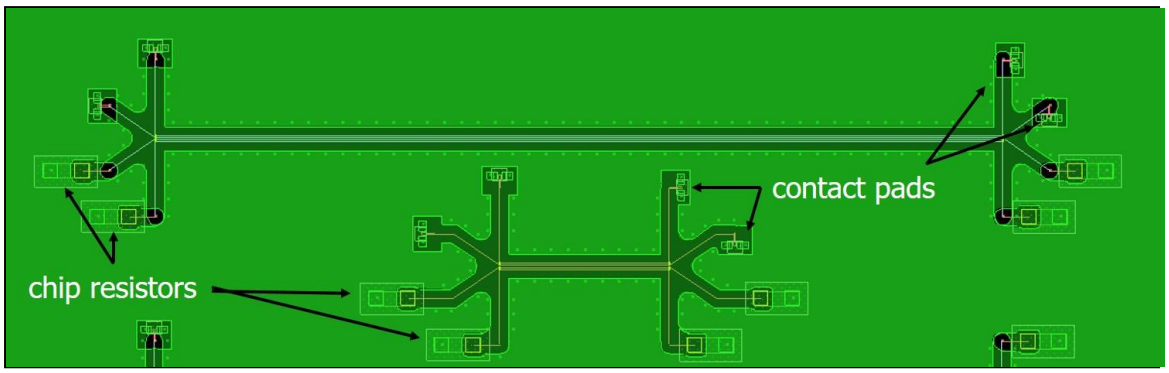


Figure 13. 8-port coupled-line layout.

The manufacturer of the ABF interposer reported much larger variations (as high as ±5 μm) in the line-width measurements performed on the 8-port coupled lines than found on the single-ended and 4-port test structures on the ABF interposer. As a result, we did not expect the level of agreement between the 8-port measurements and simulations as for the other test structures we tested.

In addition, the calibration approach we used was based on the assumption that all of the chip resistors terminating the 8-port coupled lines had an impedance equal to those we measured in a set of chip resistors we characterized separately with a two-port TRL calibration. However, we observed some significant differences between the measurements we performed of the impedances of these chip resistors, possibly due to differences in how each resistor was soldered to the ABF interposer. These measured differences led us to believe that there were also differences in the chip resistors connected to the unmeasured ports of our six 8-port test structures, possibly leading to some additional degradation of the accuracy of the 8-port scattering parameters of the coupled lines we extracted from the measurements.

Despite the variation in the measured 8-port linewidths and the impedance of the chip resistors on the ABF interposer, we found that our eight-port measurements and simulations agreed quite well. For example, Figs. 14 and 15 compare measurements and simulations of first-neighbor and second-neighbor coupling levels in four 10 mm long 12 µm wide coupled striplines fabricated in the third level of metal in the ABF interconnect stack and separated from each other by 12 µm. The agreement is quite good for first-neighbor coupling and still quite reasonable for the smaller second-neighbor coupling.

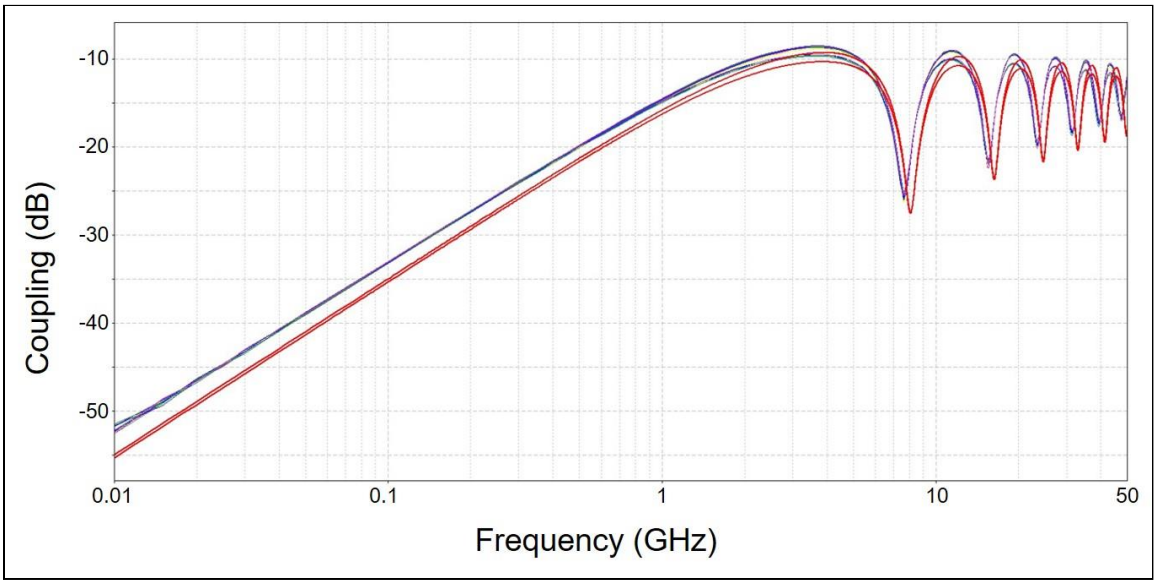


Figure 14. Coupling between first-neighbor 12 µm wide and 10 mm long striplines spaced 12 µm apart and buried in the third level of metal in the ABF interconnect stack. Measurements are shown in thinner lines.

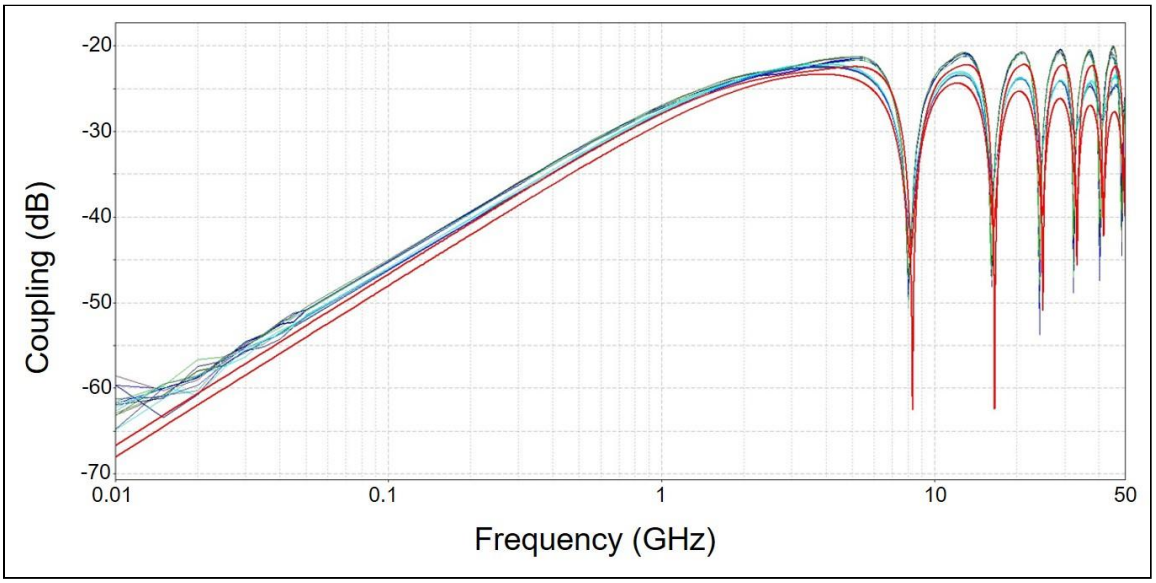


Figure 15. Coupling between second-neighbor 12 µm wide and 10 mm long striplines spaced 12 µm apart and buried in the third level of metal in the ABF interconnect stack. Measurements are shown in the thinner lines.

IV. Conclusion

The measurements and simulations we performed of test structures fabricated in the ABF interconnect stack correlated extremely well, as illustrated by the coupled stripline measurements presented in the last section. We will present more measurements in the conference, including measurements performed on test structures fabricated on the silicon interposer. We will also examine some of the cases we explored on the silicon interposer in which the agreement between the measurements and simulations were not as good as those we observed on the ABF interposer presented here. In general, we found that the slower but more accurate Sigrity full-wave solver was able to provide results that agree closely with the measurements in these cases.

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