Microwave Modeling and Characterization of Superconductive Circuits for Quantum Voltage Standard Applications at 4 K

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***Abstract*—In this article, we characterize the microwave behavior of superconductive circuits for quantum voltage standard applications at 4 K. For that, we develop a cryogenic multiline thru-reflect-line (TRL) calibration procedure to calibrate the microwave measurements at the 4 K on-wafer reference plane. We model superconductive circuits, including a Josephson array transmission line, compare simulated to TRL-calibrated measured results, and find excellent agreement up to 50 GHz.**

***Index Terms*—Dielectric characterization, Josephson arbitrary waveform synthesizer (JAWS), microwave cryogenic measurements, modeling, multiline thru-reflect-line (TRL) calibration, superconductive circuits.**

I. Introduction

THE National Institute of Standards and Technology (NIST) is developing a superconductive microwave waveform standard with quantum-based accuracy for wireless communications metrology. Two approaches based on the Josephson arbitrary waveform synthesizer (JAWS) [1]–[4] and rapid single flux quantum logic circuits [5] are being investigated.

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Studying the behavior of these superconducting circuits at microwave frequencies is an important aspect of the microwave design and requires the following:

1) the development of traceable cryogenic calibration kits;
2) modeling and characterization of passive superconducting circuits;
3) modeling and characterization of active Josephson junction based circuits.

Microwave design for superconductive voltage standards has been addressed in the literature [6]–[8]. Cryogenic calibration has also been reported for high-temperature superconducting and low-temperature superconducting applications [9]–[15]. In [16] and [17], we developed a cryogenic calibration kit and presented preliminary results of calibrated measurements on passive superconducting circuits at 4 K. The key feature of our procedure compared to prior art is the use of a broadband multiline thru-reflect-line (TRL) correction [18], [19] to calibrate the cryogenic microwave measurements at the 4 K on-chip reference plane. This calibration also allows traceability to be included in the measurements.

This article is an extension of the work presented in [16] and [17]. We develop lumped-element and electromagnetic (EM) models of passive superconductive circuits used in the NIST JAWS circuits and compare them to TRL-calibrated scattering-parameter measurements. We also propose a Josephson array transmission line model and compare it to TRL-calibrated measurements. In the future, we will add absolute amplitude and phase correction [20] to the TRL calibration to characterize quantum-accurate microwave waveforms generated at 4 K [3]–[5].

The remainder of this article is organized as follows. Section II presents lumped-element and EM models for passive superconducting circuits and introduces a model for a Josephson array transmission line. Section III describes the experimental cryogenic measurement setup and multiline TRL calibration procedure and validates the developed models against TRL-calibrated measurements. Finally, Section IV concludes this article.

II. Superconducting Circuit Modeling

In this section, we first analyze the superconducting coplanar waveguide (CPW) system used in the NIST JAWS test chip.

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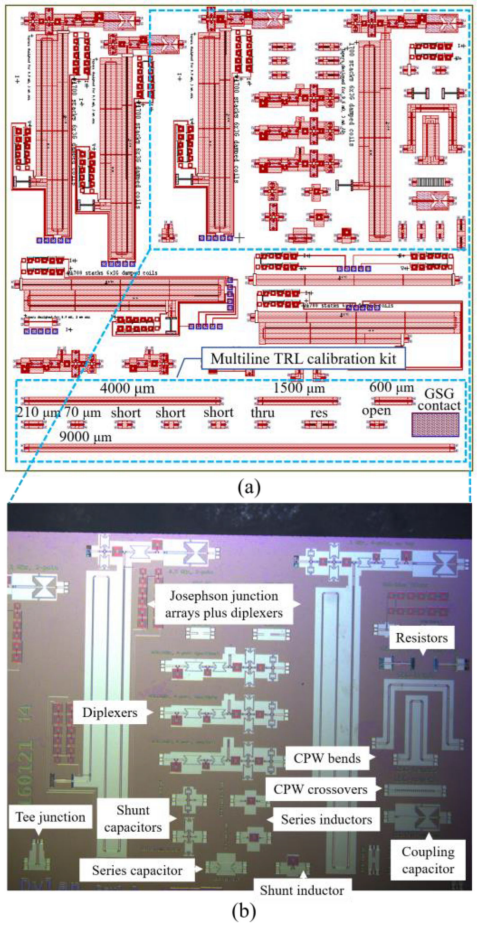

Fig. 1. (a) Layout of the JAWS niobium test chip. (b) Photograph of the superconducting test components.

Then, we develop lumped-element and 3-D EM [21] models for the passive superconducting test circuits. We also propose a model for a Josephson array transmission line.

The lumped-element models can be used in the simulation program with integrated circuit emphasis (SPICE) to support the design of microwave JAWS circuits. The independent EM models (based on the physical geometry of the test structures) help to verify our TRL calibration procedure.

The layout of the NIST JAWS niobium test chip comprising a multiline TRL calibration kit is depicted in Fig. 1(a). Fig. 1(b) shows a photograph of the superconducting test structures, including inductors, capacitors, terminations, bias tees, and CPW bends and crossovers. These components are used in diplexers and Josephson junction arrays.

A. Superconducting CPW Analysis

The magnetic energy stored in a superconducting strip can have two components [22]: 1) a geometry-dependent component proportional to the classical magnetic inductance L_m, and 2) a temperature-dependent component related to the kinetic inductance L_k. Expressions based on the conformal mapping technique [23], [24] have been given for the magnetic and kinetic inductance of a superconducting CPW transmission line [25]. From [25], we define the fractional magnetic and kinetic

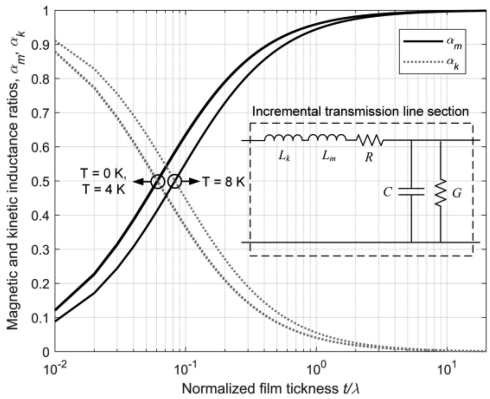

Fig. 2. Magnetic and kinetic contributions to the total inductance of a niobium superconducting CPW line for $s = 8$ μm, $w = 16$ μm, and T = 0, 4 and 8 K. In our case ($t = 600$ nm, $\lambda \approx 40$ nm), the total inductance can be approximated by the magnetic inductance. Note that very small values of t may not be feasible. Inset: equivalent circuit of an incremental superconducting transmission line section, where the kinetic energy storage due to superconducting Cooper pairs is modeled by L_k.

contributions to the total inductance, respectively, as α_m and α_k

$$\alpha_m = \mu_0 K\left(k'\right)\left(\mu_0 K\left(k'\right) + 4K\left(k\right)\frac{\mu_0\lambda^2}{tw}g\left(s,w,t\right)\right)^{-1} \tag{1a}$$

$$\alpha_k = \frac{\mu_0\lambda^2}{tw}\,g\left(s,w,t\right)\left(\frac{\mu_0}{4}\frac{K\left(k'\right)}{K\left(k\right)} + \frac{\mu_0\lambda^2}{tw}\,g\left(s,w,t\right)\right)^{-1} \tag{1b}$$

where μ_0 is the permeability in vacuum, s is the CPW gap, w is the width of the CPW center conductor, t is the film thickness, λ is the magnetic penetration depth [22], $g(s,w,t)$ is a factor that accounts for the geometry of the system [25], and $K(k)$ is the complete elliptical integral of the first kind with argument $k = w/(w+2s)$, $k' = (1-k^2)^{1/2}$.

Equations (1a) and (1b) are plotted in Fig. 2 as a function of the normalized film thickness for temperatures of 0, 4, and 8 K. As can be seen, the kinetic inductance contribution is dominant for $t/\lambda \ll 1$. Conversely, for $t/\lambda \gg 1$, as in our case ($t/\lambda \approx 15$), the magnetic inductance contribution dominates, and the total inductance of the superconducting CPW line can be approximated by the classical magnetic inductance, $L \approx L_m$.

Furthermore, as our operating temperature is well below the critical temperature of niobium (~9 K), the superconducting surface resistance is much smaller than the surface reactance ($R_s \ll X_s$) [26].

For these reasons, we use perfect electric conductor (PEC) boundaries to model the superconducting strips in our EM simulations.

B. Lumped-Element Models

We created lumped-element models in the Advanced Design System (ADS)[1] software [27] for the devices shown in Fig. 1.

[1]We use commercial brand names only to accurately describe our experiments. NIST does not endorse commercial products. Other products may perform as well or better.

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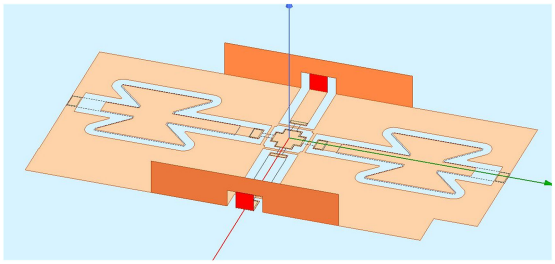
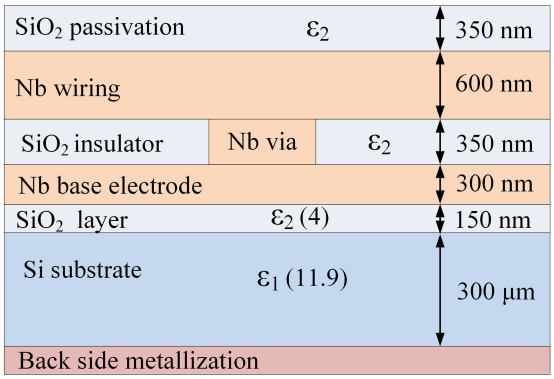


(a)



(b)

Fig. 3. (a) Example of a 3-D EM model of a parallel-plate shunt capacitor used in HFSS. (b) Illustration of the metallization layering of the passive structures.

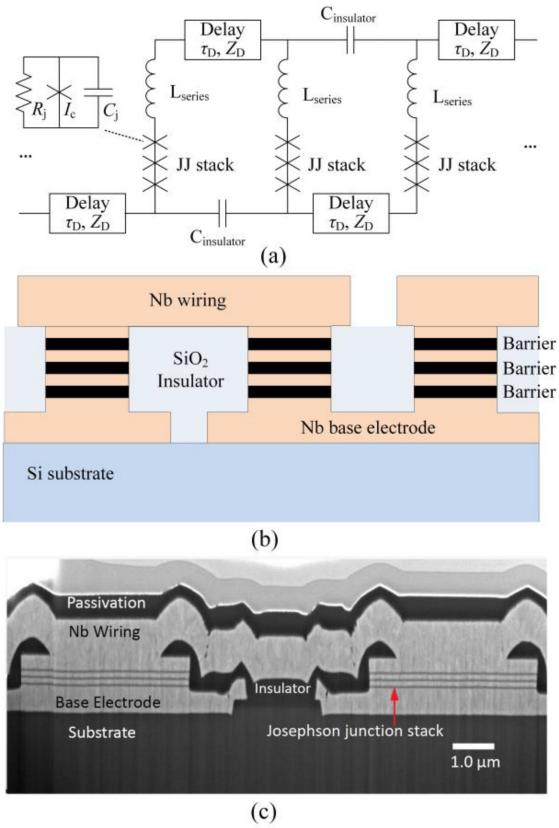


Fig. 4. (a) Proposed model implemented in ADS for Josephson array transmission lines used in the NIST JAWS circuits. (b) Illustration of the metallization layering of these Josephson junction arrays. (c) Cross-sectional photograph of a JAWS chip. Each vertical Josephson junction stack contains three junctions.

For example, the CPW transmission line system was modeled by using *N* identical sections of the lumped-element circuit shown in the inset of Fig. 2. By fitting this model to the calibrated scattering-parameter measurements of the line, we extracted the inductance L_m, capacitance *C*, and resistance *R*. Based on the previous assumptions, we set both the CPW kinetic inductance L_k and conductance G to zero.

Applying this procedure yielded $C \approx 1.4\ \mathrm{pF/cm}$ and $L_m \approx 4.1$ nH/cm. As we show later in Section III-B, this is in good agreement with theoretical values given by the conformal mapping technique [23]–[25] and experimental values extracted from the TRL calibration. A similar procedure was used to create lumped-element models for the other passive test structures. Simulated and measured results are compared in Section III.

C. Passive 3-D EM Models

We used the High Frequency Structure Simulator (HFSS) software [28] to create 3-D EM models for the devices shown in Fig. 1. As an illustrative example, Fig. 3(a) shows the 3-D EM model of a parallel-plate shunt capacitor used in the JAWS circuits [7]. We used PEC boundaries to model the superconductor strips and ideal lumped ports [shown in red in Fig. 3(a)] with PEC ground bridges to excite the CPW feed lines. The metallization layering of the passive structures is illustrated in Fig. 3(b). The CPW structures are designed on the top Nb wiring layer and the parallel-plate structures use both the top Nb wiring and bottom Nb base electrode layers.

D. Active Josephson Transmission Line Model

Fig. 4 illustrates the structure of the Josephson junction arrays used in the NIST JAWS circuits. These arrays comprise vertical stacks containing three superconductor-normal metal-superconductor junctions each, which are connected by short CPW transmission line sections. To model these arrays, we assume negligible propagation delay within each stack and model the interconnecting transmission line sections using ideal delay lines.

To describe the individual junction devices forming each stack, we use a resistively and capacitively shunted junction model [22], given by the differential equation (2). To model the coupling between adjacent stacks, we use coupling capacitors. We implemented this model in ADS using the parameters presented in Table I and validated it against TRL-calibrated measurements in a small-signal regime (see Section III-E)

$$I = \frac{C_j \Phi_0}{2\pi}\frac{d^2\gamma}{dt^2} + \frac{\Phi_0}{2\pi R_j}\frac{d\gamma}{dt} + I_c \sin(\gamma)$$
$$V = \frac{\Phi_0}{2\pi}\frac{d\gamma}{dt} \tag{2}$$

where C_j and R_j are the junction's capacitance and resistance, respectively, I and V are the current and voltage across the junction, γ is the phase difference across the junction, I_c is the

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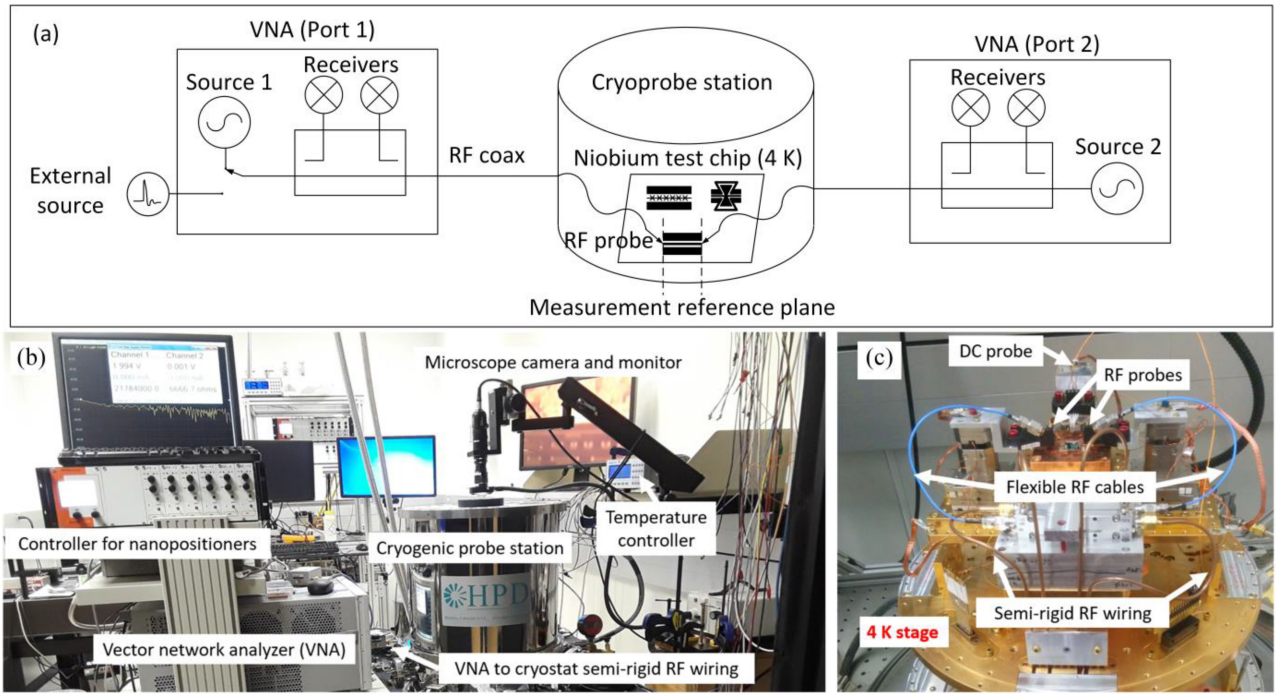

Fig. 5. (a) Simplified diagram of the cryogenic measurement setup. The external source (not used here) is intended for pulse measurements [20]. (b) Photograph of the measurement setup. (c) Photograph of the 4 K stage.

TABLE I
PARAMETERS OF THE MODEL OF Fig. 4 FOR 500 STACKS OF THREE JUNCTIONS

I_c (mA)	R_j (mΩ)	Z_D (Ω)	τ_D (fs)	L_{series} (fH)	$C_{insulator}$ (fF)
14	5	50.1	51	30	250

I_c and R_j are typical parameters of the junctions used in the NIST arrays, Z_D and τ_D define the interconnecting transmission line sections, and L_{series} and $C_{insulator}$ are parasitic components. Z_D and τ_D were tuned from their nominal values, and L_{series} and $C_{insulator}$ were selected to improve the fitting between the model and measurements.

junction's critical current, and Φ_0 is the magnetic flux quantum. For the junctions used in this work, the capacitance C_j is negligible and therefore is ignored.

III. EXPERIMENTAL RESULTS

A. Cryogenic Measurement Setup

The cryogenic measurement setup is shown in Fig. 5. We used a tabletop cryogenic probe station to cool our chip down to 4 K, a vector network analyzer (VNA) to perform microwave measurements on the superconducting test structures through movable RF probes installed in the 4 K stage and a broadband TRL correction to calibrate these measurements at the 4 K on-wafer reference plane.

The tabletop probe station features four positioners with nanometer resolution (nanopositioners) for dc and RF probes and a sample stage cooled by a 1-W Gifford-McMahon cryocooler. To minimize magnetic interference in the superconducting test structures, we used specialized RF probes made of nonmagnetic material and with no RF absorbers.

Large attenuation introduced by the 300 K down to 4 K RF wiring was identified as a major limitation for achieving high-quality measurements over a broad frequency range. Our initial measurement setup presented a round trip loss of 33 dB and was excessively noisy above 25 GHz. By using shorter and higher quality RF cables, we reduced the round-trip loss to 10 dB and were able to extend our measurements up to 50 GHz.

Previous work has shown that *in situ* couplers are effective in dealing with excessive attenuation in millikelvin applications [15]. We experimented with the VNA couplers mounted on the cold stage for scattering-parameter measurements. Although the noise performance improved, the improvement was marginal compared to the shortened-wiring setup and did not justify the extra complexity of couplers mounted on the cold stage. Besides, conventional absolute power and phase calibration techniques cannot be applied with the VNA couplers at the cold stage. The measurements reported in this article were made using the shortened-wiring setup.

B. Cryogenic Multiline TRL Calibration

To calibrate our measurements at the 4 K on-wafer reference plane, we developed a cryogenic multiline TRL calibration kit in the NIST JAWS process [29] [see bottom of Fig. 1(a)]. Advantages of the TRL technique include broadband operation

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TABLE II
SUPERCONDUCTING CPW TRANSMISSION LINE PARAMETERS

CPW parameter	TRL calibration	Lumped-element model	Theoretical [23]-[25]
C (pF/cm)	1.419	1.416	1.426
L (nH/cm)	4.158	4.145	4.137
L_k (nH/cm)			0.007

Note that L_k is three orders of magnitude smaller than L_m, which verifies the approximation made previously ($L \approx L_m$).

and ease of design and modeling of the calibration standards. Additionally, the NIST multiline TRL calibration algorithm used in this work enhances accuracy through measurement redundancy [18], [19]. To perform the measurement correction, we used the NIST Microwave Uncertainty Framework, which allows us to capture correlated microwave measurement uncertainties and transform them between frequency and time domains [30].

The TRL calibration results are typically referenced to the characteristic impedance of the CPW lines of the TRL calibration kit (Z_{LINE}). This impedance often deviates from 50 Ω, which can confuse the results. By using the method presented in [31], we estimated the capacitance per unit length of our CPW system and used it in conjunction with the propagation constant obtained from the TRL calibration algorithm to determine the actual characteristic impedance of the system and renormalize our calibrated measurements to 50 Ω [32].

A technique similar to [31] was used to determine the CPW inductance per unit length. Table II compares the CPW inductance and capacitance per unit length measured by use of the TRL calibration to the calculated values from the lumped-element model described in Section II-B and the conformal mapping analytical model [23]–[25].

C. Experimental SiO_2 Dielectric Characterization

While the properties of the SiO_2 insulator have little impact on the top CPW structures, they strongly impact the parallel-plate structures. We characterized the SiO_2 insulator by using the TRL-calibrated measurement of a parallel-plate capacitor (see Fig. 6) [33] and used the dielectric constant obtained experimentally in our EM simulations. For that, we expressed the frequency-dependent dielectric constant as in (3) and extrapolated to dc to find an estimate of ε_r

$$\varepsilon_r(\omega) = -\frac{d}{A\omega\varepsilon_0 \operatorname{Im}\{Z_{\mathrm{pp}}(\omega)\}} \tag{3}$$

where A and d are the area of the capacitor plates and their separation, respectively, ω is the angular frequency, ε_0 is the free-space permittivity, and Z_{pp}, the impedance of the capacitor, is obtained from the calibrated scattering-parameter data as $Z_{\mathrm{pp}} = Z_0((1+S_{11})(1+S_{22}) - S_{12}S_{21})/(2S_{21})$ [34].

Assuming the nominal thickness of the SiO_2 dielectric ($d =$ 350 nm), the experimental dielectric constant was found to be $\varepsilon_r = 4.11$.

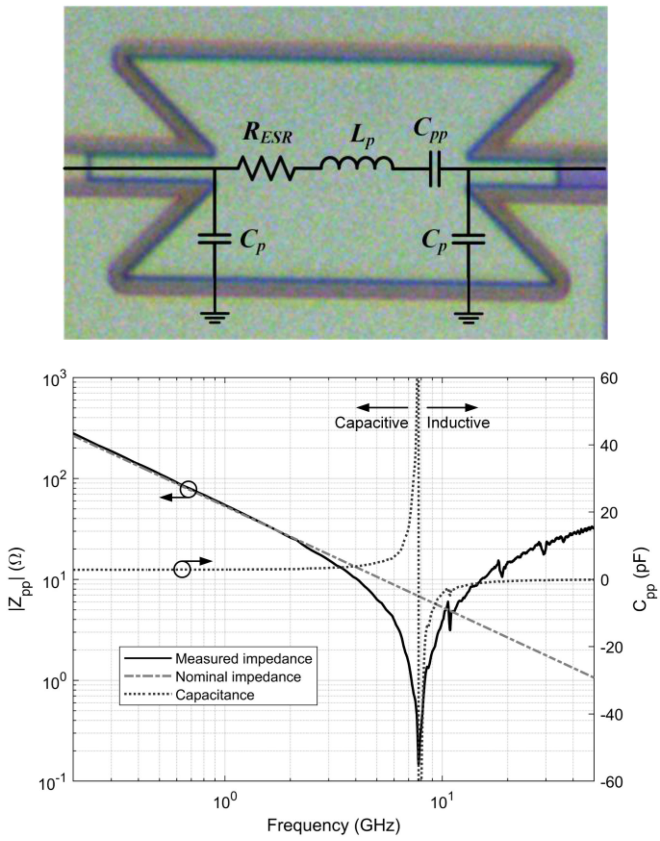

Fig. 6. Top: Photograph of the parallel-plate series capacitor used for characterizing the SiO_2 insulator. The inset shows the capacitor's equivalent circuit. Bottom: Nominal and experimental impedance and experimental capacitance.

We also analyzed the bandwidth and resonance frequency of our test structures. The bottom of Fig. 6 presents the nominal and experimental impedance and the experimental capacitance, $C_{\mathrm{pp}}(\omega) = -1/(\omega \operatorname{Im}\{Z_{\mathrm{pp}}(\omega)\})$, of the parallel-plate series capacitor at the top of the figure.

This capacitor, nominally designed for 3 pF, presented an experimental low-frequency capacitance of 2.84 pF and a resonance frequency of 7.78 GHz. As expected, as the frequency increases, the capacitance deviates from its nominal value, and the parasitic series inductance becomes dominant for frequencies greater than the resonance frequency. A similar behavior was observed for the other parallel-plate structures.

D. Simulations Versus Measurements of the Passive Devices

Fig. 7 presents a comparison between the TRL-calibrated measurements and simulations for the 1.22 pF parallel-plate shunt capacitor illustrated in Fig. 3(a) [see Fig. 7(a) and (b)] and a 4 mm CPW transmission line [see Fig. 7(c) and (d)]. Overall, the measurement and simulation results displayed good agreement across the 50 GHz bandwidth. The parallel-plate structures presented a frequency shift between simulations and measurements.

This frequency shift, believed to be due to process variation, was resolved by adjusting the thickness of the SiO_2 substrate in the EM model within $\pm 10\%$ variation of the fabrication process.

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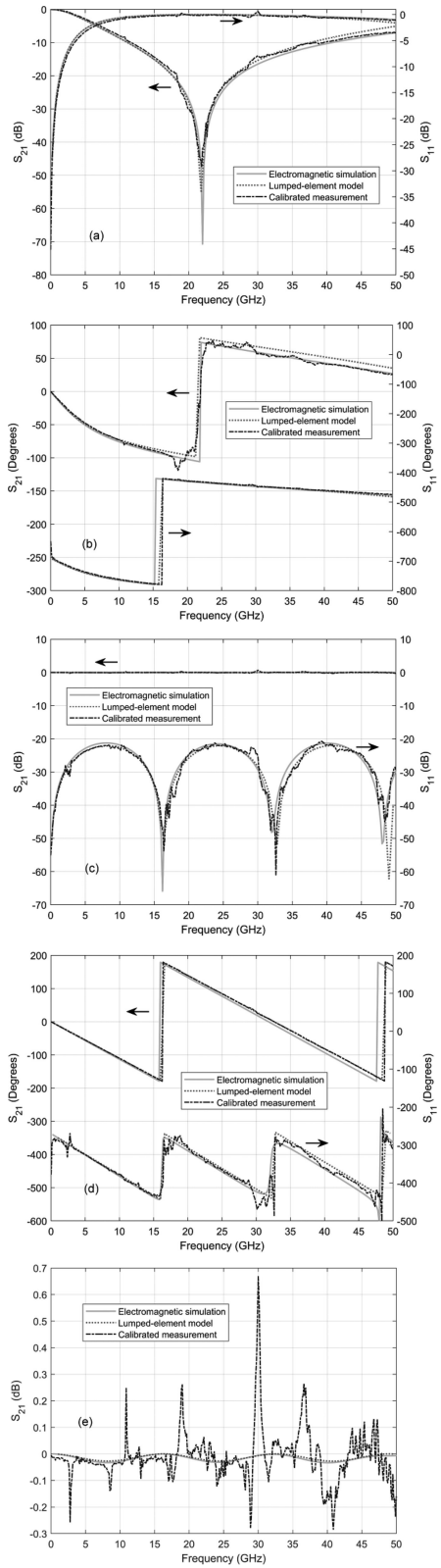

Fig. 7. Comparison between EM models, lumped-element models, and TRL-calibrated measurements. (a) Magnitude of transmission and reflection coefficients of 1.22 pF shunt capacitor. (b) Phase of transmission and reflection coefficients of 1.22 pF shunt capacitor. (c) Magnitude of transmission and reflection coefficients of 4-mm CPW transmission line. (d) Phase of transmission and reflection coefficients of 4-mm CPW transmission line. For clarity of the results, we added a phase offset to the S_{11} phase. (e) Magnification of the CPW transmission coefficient of Fig. 7(c).

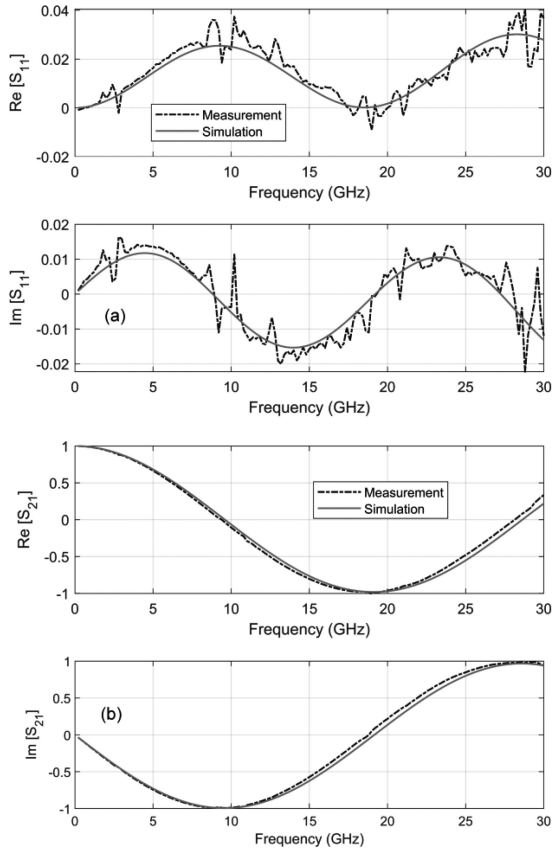

Fig. 8. Josephson array transmission line model validation against TRL-calibrated measurements under small signal. (a) Reflection coefficient. (b) Transmission coefficient.

Our calibrated data presented high-Q artifacts, which are visible, for instance, when magnifying the transmission coefficient of the CPW transmission lines [see Fig. 7(e)]. We attribute these artifacts to a degradation in the quality of the single-mode TRL calibration in the presence of high-Q superconducting parasitic mode coupling. This effect has previously been reported in short-open-load (SOL)-calibrated measurements [11] and is especially problematic in multiline TRL calibrations.

E. Preliminary Validation of the Josephson Transmission Line Model

Here, we present a preliminary validation of the proposed Josephson array transmission line model against TRL-calibrated measurements in a small-signal regime. Fig. 8 shows simulated and measured results for a 1500-junction array under a small RF bias and no dc bias. In these conditions, the array behaves simply as a superconductive transmission line. Further details of the proposed model can be found in [35].

IV. Conclusion

In this article, we developed a cryogenic multiline TRL calibration kit for microwave characterization of superconducting circuits for quantum voltage standard applications. We created

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3-D EM and lumped-element models for these circuits and compared their simulated results to TRL-calibrated measurements.

We developed a Josephson array transmission line model and validated it against TRL-calibrated measurements in a small-signal regime. To the best of our knowledge, this is the first time such an attempt has been made.

Major issues identified in our cryogenic measurement setup included artifacts due to excessive attenuation in the RF wiring and the large quality factor parasitics in and between superconducting structures.

High-frequency noise due to excessive attenuation in the RF wiring was suppressed by using shorter and lower attenuation silver-plated RF cables. The problem of large quality factor superconducting parasitics is being investigated by accurately modeling the RF ground-signal-ground (GSG) probe to CPW discontinuity and exploring strategies to damp the quality factor.

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