Physics-based Electro-thermal Saber Model Validation for 3.3 kV, 45 A 4H-SiC MOSFET in Medium Voltage Power Converters†

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Abstract— The purpose of this paper is to present a physics-based electro-thermal Saber®* model validation for a new 3.3 kV, 45 A 4H-SiC MOSFET developed by Wolfspeed. In this paper, the validated results include output characteristics and inductive load turn-off switching for this device and the current-voltage, capacitance-voltage, reverse leakage, and reverse recovery characteristics for its intrinsic body diode. The validated models are then used to perform a simulation of a two-level three-phase voltage source inverter to evaluate the converter loss and the efficiency.

I. INTRODUCTION

Silicon carbide (SiC) has emerged as a material of choice for the next generation of high-voltage power semiconductor devices. The primary advantage of the SiC material for power devices is that it has an order of magnitude higher breakdown electric field (2×10^6 V/cm to 4×10^6 V/cm) and a higher temperature capability than conventional silicon materials [1]. Today, SiC Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) have established wide-spread commercial acceptance in the low-voltage range (600 V to 1700 V) with a market that is growing exponentially. High-voltage (10 kV) SiC Junction Barrier Schottky (JBS) diodes have also recently been demonstrated as the anti-parallel diode for SiC MOSFETs in 10 kV, 100 A half-bridge modules, and these modules are being applied to demonstrate a 13.8 kV, 2.75 MVA Solid State Power Substation [2]. Although the 10 kV SiC devices represent a transformational technology, it is expected to take some time before such products appear on the market, largely due to the relative lack of maturity of the SiC MOSFETs. However, medium-voltage SiC MOSFETs could be employed sooner. The purpose of this paper is to present the physics-based electro-thermal model validations for the new single die 3.3 kV, 45 A 4H-SiC MOSFET, hereafter referred to as the device under test (DUT) developed by Wolfspeed [3] using a previously developed model [4] where the corresponding automated model parameter extraction tools [5, 6, 7] are used to determine the model parameters from measured data. The high voltage experiments were performed using well characterized experimental test systems [8, 9]. The Saber model of the DUT and its body diode is also used to simulate a two-level three-phase voltage source inverter (VSI) with balanced R-L load.

II. SABER MODEL VALIDATION AND INVERTER SIMULATION RESULTS

A. *Saber Model Validation Results*

Figs. 1, 2, and 3 show the 3.3 kV, 45 A SiC 4H-SiC MOSFET model (solid) compared with measured (dashed) output characteristics at 25 ºC, 125 ºC, and 175 ºC, respectively.

Fig. 4 compares the measured (dashed) and simulated (solid) drain current and drain-source voltage waveforms for clamped inductive load switching at four different switching currents (i.e., 15 A, 25 A, 35 A, and 45 A) for the DUT at the clamped voltage of 2.5 kV, gate resistor of 24.7 Ω and MOSFET temperature of 25 ºC. Fig. 5 compares the measured (dashed) and simulated (solid) drain current and drain-source voltage waveforms for clamped inductive load turn-off switching at different clamp voltages for the DUT at a switching current of 45 A, gate resistor of 24.7 Ω, and MOSFET temperature of 25 ºC. Fig. 6 compares the measured (dashed) and simulated (solid) drain current and drain-source voltage waveforms for clamped inductive load turn-off switching at different gate resistor values for the DUT at a switching current of 45 A, clamp voltage of 2.5 kV, and MOSFET temperature of 25 ºC.

Fig. 7 shows the comparison of measured (dashed) and simulated (solid) output characteristics over a temperature range from 25 ºC to 175 ºC for the body diode of the DUT. Fig. 8 shows the comparison of measured (dashed) and simulated (solid) junction capacitance at 25 ºC for the body diode of a DUT. Figs. 9 and 10 show the comparison of measured (dashed) and simulated (solid) reverse blocking characteristics over a temperature range from 25 ºC to 175 ºC for the body diode of the DUT in logarithmic scale and linear scale, respectively. Figs. 11 and 12 show the comparison of measured (dashed) and simulated (solid) reverse recovery at 25 ºC and 175 ºC for three different di/dt (e.g. 40 A/µs, 80 A/µs, and 160 A/µs) for the body diode of the DUT.

B. *Inverter Simulation Results*

Fig. 13 shows the simulation schematic for the two-level three-phase voltage source inverter enabled by using the validated DUT with balanced R-L load. The intrinsic body diodes of the MOSFETs are used as the anti-parallel diodes in the inverter simulation. Fig. 14 demonstrates that the validated

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model can be used to simulate the performance of a two-level three-phase voltage source inverter with balanced R-L load at dc bus voltage (V_{DC}) of 2.5 kV, peak MOSFET current of 36 A, gate resistor of 25 Ω, and sine-triangle Pulse Width Modulation (PWM) switching frequency of 10 kHz. Fig. 14 shows the simulated three-phase line-to-line output voltage (V_{AB}) and the phase currents (i.e., phase-A, phase-B, and phase-C, respectively) for a two-level three-phase VSI with balanced R-L load. It is assumed that all the six MOSFETs are mounted on the same heat sink, and their junction temperatures are equal. Figs. 13-15 show the simulation results at the junction temperature of 100 °C under the operation condition mentioned in Fig. 13. Fast Fourier Transform (FFT) of the line-to-line voltage V_{AB} and the phase current I_{phA} are plotted in Fig. 15 using the in-built FFT tool of Saber®. The switching harmonics are observed at 10 kHz and its integral multiples. Current and voltage waveform of the MOSFET M2 are plotted in Fig. 16. Overshoot in the MOSFET current is observed due to reverse recovery of the body diode. This overshoot in the current contributes to the additional losses in the MOSFET.

Junction temperatures of the MOSFETs in the practical voltage source inverter are typically maintained in the range of 75 °C to 125 °C based on the thermal dissipation capability of the heat sink. For a given power loss, a higher junction temperature allows for a lower size of the heat sink. The three-phase voltage source inverter is simulated for three junction temperatures 75 °C, 100 °C, and 125 °C at the operating conditions mentioned in Fig. 13. The simulation results are plotted in Fig. 17. Total loss in each of the MOSFETs is calculated by averaging the integration of the product of V_{DS} and I_D of the MOSFET over the 60 Hz cycle. Total power loss in the converter is determined by summing up the individual losses in all of the six MOSFETs. It should be noted here that this loss accounts also for the overshoots due to parasitic in the converter, the capacitive current and the reverse recovery effects of the body diodes at the given junction temperature. Fig. 17 shows that the best efficiency of 97.67 % is obtained at 100 °C. In this condition the heat sink must dissipate 1726 W of the power loss. Assuming the ambient temperature to be 50 °C, the required thermal resistance of the heat sink comes out to be 0.029 °C/W. The plot in Fig. 17 will vary, if different gate resistors are used for turn-on and turn-off of the MOSFETs. This simulation model provides a platform to optimize the converter losses by varying the gate resistor and the desired junction temperature.

CONCLUSIONS

This paper demonstrates the validation of static and dynamic characteristics for a new 3.3 kV, 45 A 4H-SiC MOSFET developed by Wolfspeed in Saber® Circuit Simulator. The validation of static and dynamic characteristics for its anti-parallel diode are also presented. The performance of the validated model can be used in simulation of medium voltage converters such as a two-level three-phase VSI as presented in this paper. This physics-based model provides nearly accurate results considering the parasitic in the power converters and the junction temperature, which is difficult to derive by analytical methods and other simulation models based on piecewise approximation. In practical medium voltage applications, typically multiple dies are paralleled to increase the current capacity of the power module. This physics-based model can be further used to investigate the effect of parasitics due to bond wires and the direct-bonded copper (DBC) layout involved in paralleling the dies to form a power module. The derived model of the power module can be further analyzed to estimate the efficiency of the converter in other widely used medium voltage power converter topology such as neutral point clamped (NPC), cascaded H-bridge (CHB) and modular multilevel converters (MMC).

ACKNOWLEDGMENT

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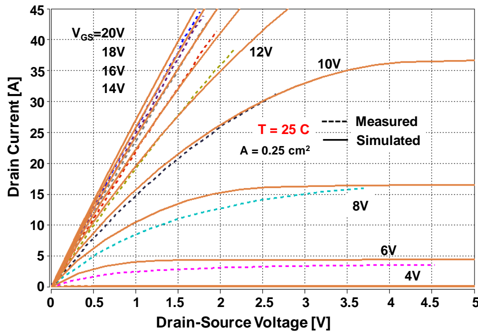
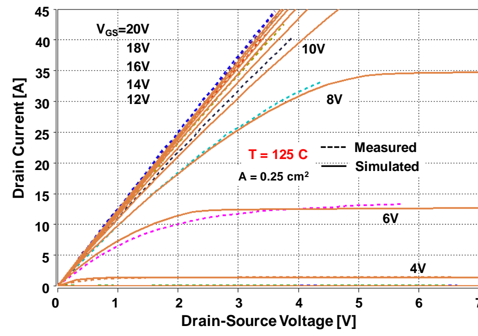




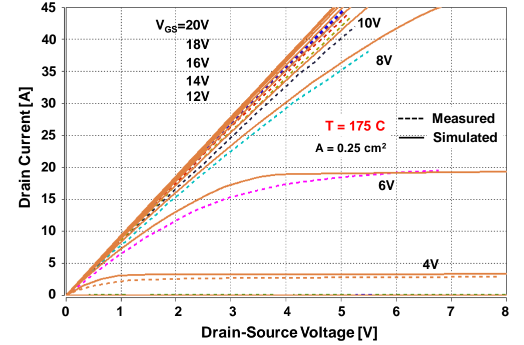
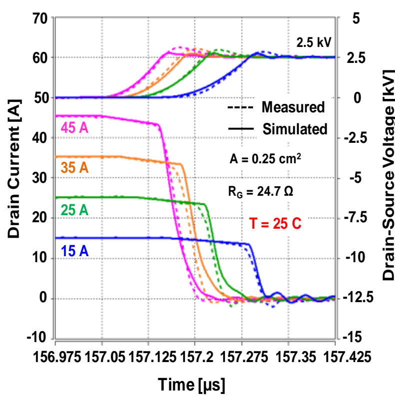
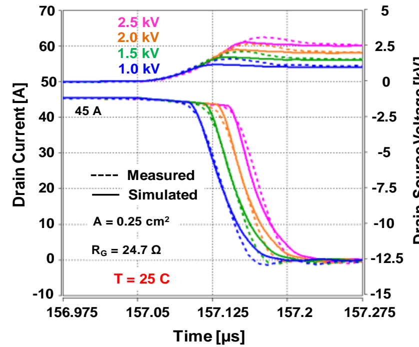


Fig. 1. Comparison of measured (dashed) and simulated output characteristics of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C.

Fig. 2. Comparison of measured (dashed) and simulated output characteristics of a 3.3 kV, 45 A 4H-SiC MOSFET at 125 °C.

Fig. 3. Comparison of measured (dashed) and simulated output characteristics of a 3.3 kV, 45 A 4H-SiC MOSFET at 175 °C.





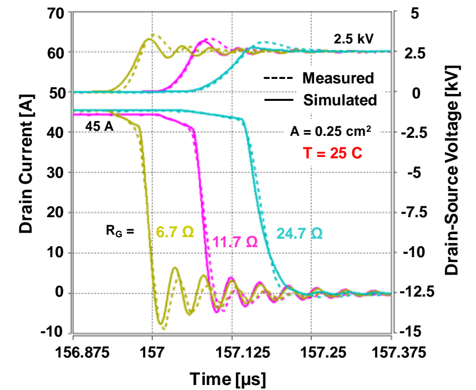
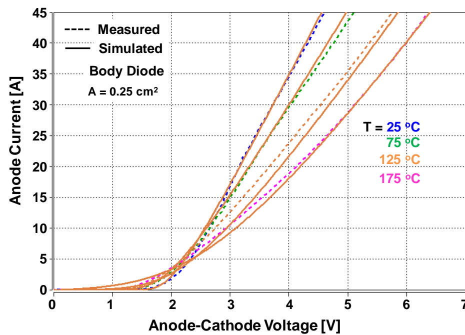
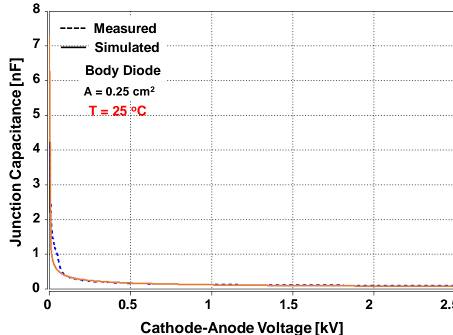


Fig. 4. Measured (dashed) and simulated (solid) drain current and drain-source voltage waveforms for clamped inductive load turn-off switching at different drain currents for a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C.

Fig. 5. Measured (dashed) and simulated (solid) drain current and drain-source voltage waveforms for clamped inductive load turn-off switching at different drain-source voltages for a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C.

Fig. 6. Comparison of measured (dashed) and simulated (solid) clamped inductive load turn-off waveforms at 25 °C and different gate resistors for a 3.3 kV, 45 A 4H-SiC MOSFET.





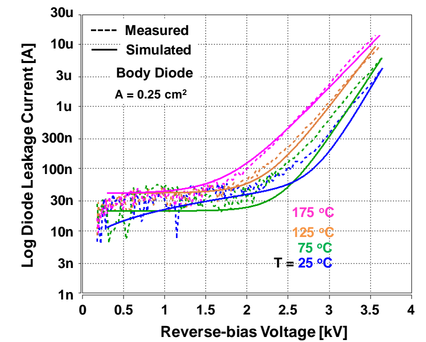


Fig. 7. Comparison of measured (dashed) and simulated output characteristics for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C, 75 °C, 125 °C, and 175 °C.

Fig. 8. Comparison of measured (blue dashed) and simulated (orange solid) junction capacitance for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C.

Fig. 9. Comparison of measured (dashed) and simulated (solid) reverse-biased leakage for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C, 75 °C, 125 °C, and 175 °C.

In this paper, the primary uncertainties of the measurements are based on commercial oscilloscopes probes. Due to the requirements for probe compensation, it is safe to specify that uncertainties in our measurements are within ± 10 %.

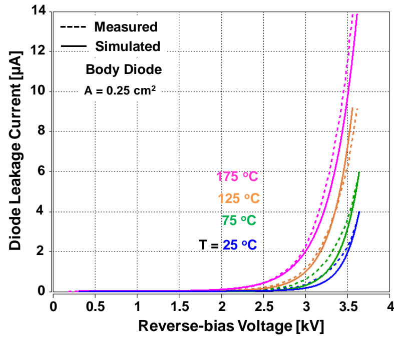


Fig. 10. Comparison of measured (dashed) and simulated (solid) reverse-biased leakage for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C, 75 °C, 125 °C, and 175 °C.

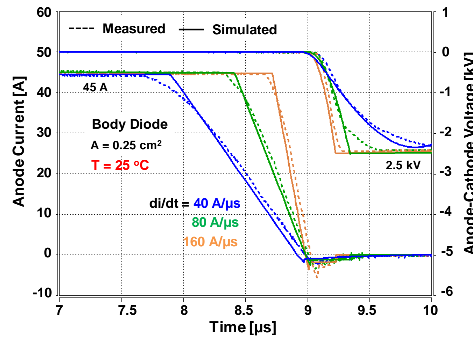


Fig. 11. Comparison of measured (dashed) and simulated (solid) reverse recovery for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 25 °C.

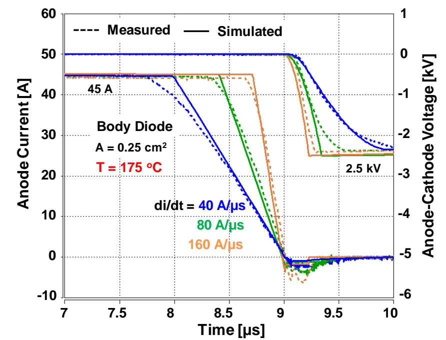


Fig. 12. Comparison of measured (dashed) and simulated (solid) reverse recovery for the body diode of a 3.3 kV, 45 A 4H-SiC MOSFET at 175 °C.

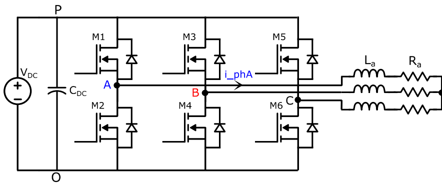


Fig. 13. Simulation schematic for the two-level three-phase voltage source inverter enabled by 3.3 kV, 45 A SiC MOSFETs with balanced R-L load. The intrinsic body diodes of the MOSFETs are used as the anti-parallel diodes in the simulation. V_{DC}: 2500 V, Cdc: 300 µF, dead time: 5 µs, PWM: sine-triangle PWM, fundamental frequency: 60 Hz, switching frequency: 10 kHz, modulation index: 0.95, Ra = 55 Ω, La = 40 mH, winding resistance of La: 2 Ω, parasitic capacitance of La: 100 pF, gate voltage drive: +15V/-5V, gate resistor RG: 25 Ω, M1-M6: 3.3kV, 45A SiC MOSFET.

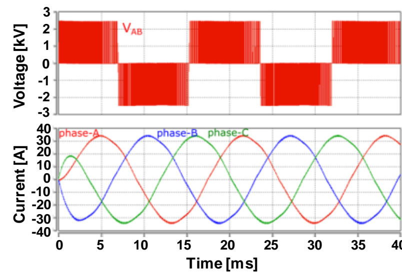


Fig. 14. Simulation results: line-to-line voltage and phase- A load current waveform of the two-level three-phase voltage source inverter with balanced R-L load at Vdc of 2.5 kV, peak MOSFET current of 36 A, gate resistor of 25 Ω, switching frequency of 10 kHz, and the junction temperature of 100 °C using the validated Saber model of a 3.3 kV, 45 A 4H-SiC MOSFET. $V_{L\text{-}L}$ (RMS): 1737 V, I_L (RMS): 24.1A, Output power: 72.5 kVA, Power factor: 0.97.

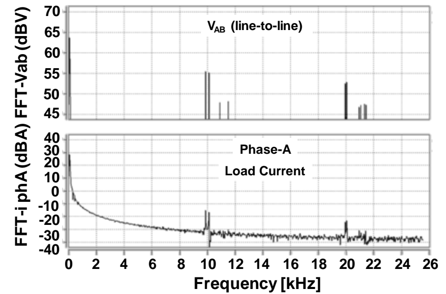


Fig. 15. Simulation results: FFT waveform of the line-to-line voltage and load current of the two-level three-phase voltage converter with the same operating condition mentioned in Fig. 13 and the junction temperature of 100 °C.

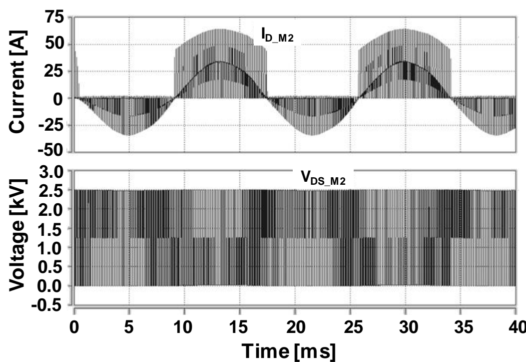


Fig. 16. Simulation results: drain current and drain-to-source voltage waveform of the MOSFET M2 in the two-level three-phase voltage converter with the same operating condition mentioned in Fig. 13 and the junction temperature of 100 °C.

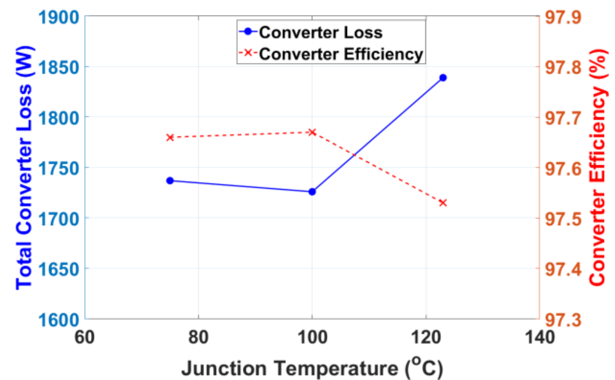


Fig. 17. Simulation results: Plot of the total converter loss and the efficiency at the junction temperatures: 75 °C, 100 °C and 125 °C in the two-level three-phase voltage source inverter at the operating conditions mentioned in Fig. 13. $V_{L\text{-}L}$ (RMS): 1737 V, I_L (RMS): 24.1A, Output power: 72.5 kVA, Power factor: 0.97.