High-Throughput, DC-Parametric Evaluation of Flux-Activated-Switch-Based TDM and CDM SQUID Multiplexers

Carl D. Reintsema, Doug A. Bennett, Edward V. Denison, Malcolm Durkin, Willaim B. Doriese, Joseph W. Fowler, Johnathon D. Gard, Arpi Grigorian, Gene C. Hilton, Johannes Hubmayr, Galen C. O'Neil, John A. B. Mates, Kelsey M. Morgan, Dan R. Schmidt, Robert W. Stevens, Daniel S. Swetz, Leila R. Vale, Joel N. Ullom, Kent D. Irwin, Saptarshi Chaudhuri, Charles J. Titus, and Carl S. Dawson

(Invited Paper)

***Abstract*—The successful realization and broad deployment of transition edge sensor (TES)-based detector systems has led to significant demand for time-division and code-division superconducting quantum interference device (SQUID) multiplexers time division multiplexing (TDM) and code division multiplexing (CDM) as essential components of the cryogenic readout chain. TDM and CDM circuits are produced by the Boulder Microfabrication Facility in large quantities and in multiple varieties to meet the needs of various bolometric and calorimetric applications. In most cases, the basic functionality of these devices must be verified before they are passed along to internal or external collaborators for integration into scientific instruments. We have developed a test bed that utilizes the NIST TDM/CDM read-out electronics to make automated multiplexed measurements on sixteen devices simultaneously in a 4 K liquid-helium dip probe. The optimization of the measurement process has resulted in vastly improved throughput and enhanced data products. We present a thorough analysis of results from the application of the test process to flux-activated-switch-style multiplexers. The utility of this approach in identifying fabrication trends, yield indicators, and common failure modes will be demonstrated.**

***Index Terms*—Cryogenic electronics, superconducting quantum interference devices (SQUIDs), superconducting integrated circuits.**

I. Introduction

SINCE the emergence of the first superconducting quantum interference device (SQUID) multiplexers twenty years ago [1], testing protocols have evolved from rudimentary single-chip evaluations using benchtop instruments and manual parameter extraction [2], to multiplexed high-speed automated measurements of many embedded devices simultaneously [3]. The latest system in use at NIST leverages the capabilities of the NIST Next-Generation digital-feedback electronics [4], [5] to interrogate an array of 16 multiplexers in a single 4 K cooling cycle. The system completes a full suite of dc-parametric measurements on these devices in ∼40 minutes. A set of specifications and a family of plots is automatically generated for each device upon completion of the tests. These data products are distributed with the devices.

To further optimize throughput, we use advanced tools to prescreen and prepare the samples. For certain device classes we employ semi-automated, wafer-scale, room-temperature probing technology to isolate bad devices following fabrication. This saves time and resources that would otherwise be spent cooling and measuring devices with fatal manufacturing defects. As demand remains strong and device technologies evolve, we strive to remain agile in adapting new technologies to help meet our quality assurance (QA) requirements. Some of the future technologies under development will be addressed in Section VI of this article.

II. Test Facility

All tests are conducted in a liquid-helium dip probe at 4 K. The devices are connected to the room-temperature electronics via low-thermal-conductivity flexible transmission lines with 88 signal pairs. This allows us to fully instrument 16 11-channel time division multiplexing (TDM) chips [6] arranged in a 2-row by 8-column array. Chips are mounted on a printed circuit board (PCB) daughter card that plugs into the probe through a pair of high-speed mezzanine connectors. A fully populated daughter card mounted on the dip probe is pictured in Fig. 1. With all row selects (equivalently referred to as *row address* and used interchangeably throughout) and inputs connected these boards require 832 wire bonds. We use a semi-automated wire bonder to fully bond a daughter card in ∼20 minutes with typical yield >99.9%.

Manuscript received October 30, 2018; accepted March 4, 2019. Date of publication March 12, 2019; date of current version April 17, 2019. The authors gratefully acknowledge funding from the NASA SAT Program, "Providing Enabling & Enhancing Technologies for a Demonstration Model of the Athena X-IFU." *(Corresponding author: Carl D. Reintsema.)*

C. D. Reintsema, D. A. Bennett, E. V. Denison, M. Durkin, W. B. Doriese, J. W. Fowler, J. D. Gard, A. Grigorian, G. C. Hilton, J. Hubmayr, G. C. O'Neil, J. A. B. Mates, K. M. Morgan, D. R. Schmidt, R. W. Stevens, D. S. Swetz, L. R. Vale, and J. N. Ullom are with the Quantum Sensors Group, Physical Measurement Laboratory, National Institute of Standards and Technology, Boulder, CO 80305 USA (e-mail: carl.reintsema@nist.gov).

K. D. Irwin, S. Chaudhuri, C. J. Titus, and C. S. Dawson are with the Department of Physics, Stanford University, Stanford, CA 11973 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TASC.2019.2904594

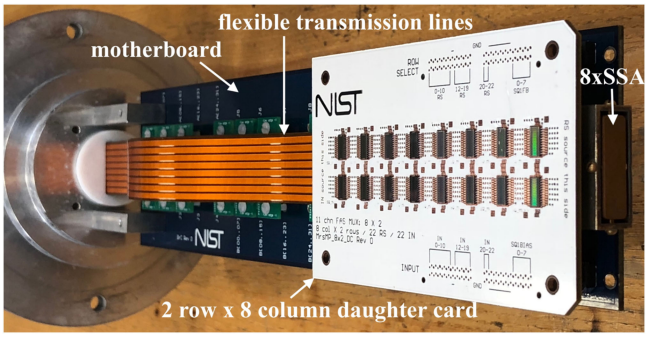

Fig. 1. Image of the cold end of the dip probe with HSMC mounted daughter card. 16 SMUX chips are arranged and bonded in an 8-column by 2-row array.

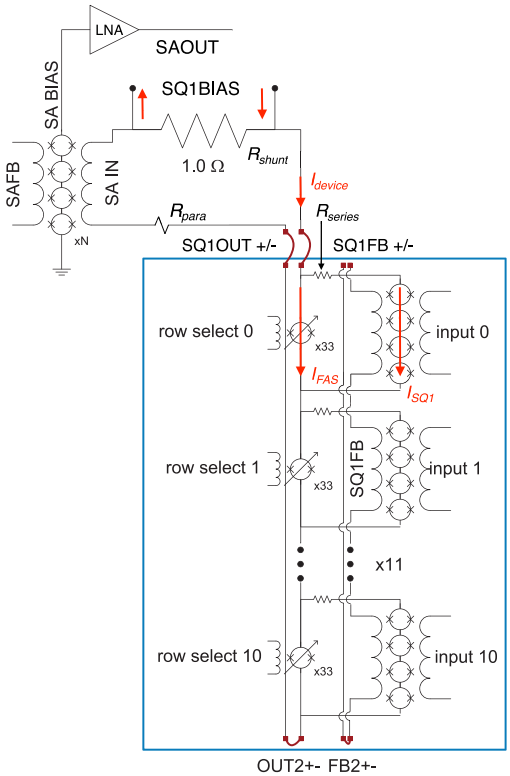

Fig. 2. Device Schematic showing FAS style SQUID multiplexer (inside blue box) and SSA and bias circuitry above.

Each of the 8 columns of chips is read out through a SQUID series array (SSA) mounted on the motherboard at the cold end of the probe. The devices are shielded from magnetic fields and ambient electromagnetic interference (EMI) by a high-permeability magnetic-alloy enclosure and the Faraday cage of the dewar itself.

III. Device Description

The schematic for an 11-channel flux-activated-switch (FAS) style SQUID multiplexer (SMUX) [6] is shown in Fig. 2. The active elements of the SMUX chip are represented within the blue box. The 2nd-stage SSA amplifier and bias circuitry are located off the chip. The $\sim$1 Ω $R_{\rm shunt}$ in parallel with the multiplexer, when driven by the 1st-stage SQUID bias current (SQ1B), presents a voltage bias to the device under test (DUT). The DUT is in series with the input coil to the SSA (SAIN). The SSA is current biased and the output voltage in monitored by a room-temperature, low-noise amplifier (LNA).

The SMUX chip has 11 identical channels composed of a SQUID input stage, a 4-element series array in series with a thin-film resistor $R_{\rm series}$, in parallel with a FAS. Two of these chips are bonded in series to form a column of the device array.

The principle of operation of this device has been described in detail elsewhere [6]–[8]. A FAS remains closed and all current bypasses the input stage when no current is applied to the row-select line, because the switch is superconducting. When current to create flux of 0.5 Φ_0 in the FAS is applied to the row select line, the FAS becomes resistive and current diverts through the input-stage SQUIDs. If this current exceeds the critical current of the input stage SQUIDs (SQ1) then the current in this branch will modulate with magnetic flux applied through either the dedicated input coil (SQ1IN) or the common feedback coil (SQ1FB). This device current is sensed by the SSA which is operated in a flux locked loop (FLL) with a digitally controlled nulling signal applied to the SSA feedback (SAFB).

The tests in our QA protocol manipulate signals on these control lines to parameterize the response of each device. The goal of the process is both to insure basic functionality and to identify devices with similar characteristics so they can be integrated into the destination instrument.

IV. Testing Methodology

A. Flux-Activated-Switch Characterization

For the FAS-style multiplexer the characterization begins with determination of the minimum critical current of the switches in a column, or $I_{\rm ccol}$. Because all switches are in a superconducting state with no flux switch activation applied, and there is normal resistance ($R_{\rm series}$) in the input-element branches, all bias current flows through the switches. This remains the case until the minimum critical current of one of the switches is exceeded thereby shunting current to the input branch of the corresponding row. The onset of resistance in the device occurs when the current exceeds the critical current of any of the 33 SQUID elements in any of the 22 switches. Because the critical currents of the SQUIDs in the FASs are not uniform, a gradual increase in the resistance evolves as the bias current is increased. A flux modulation on the common SQ1FB line will not appear on the SAFB signal until there is sufficient current passing through an input branch to exceed the critical current of the SQUIDs in that branch, i.e., $I_{\rm cmin}$ of SQ1. $I_{\rm ccol}$ is defined as the bias current at which this modulation first appears. The impact on the measurements from this distributed resistance onset below $I_{\rm ccol}$ will be clarified later in this paper.

During operation, the current flowing in the switch branch must never exceed $I_{\rm ccol}$ to ensure that no current flows through any input branch when the corresponding switch is in the closed (bypass) state. The purpose of the first test is to benchmark this current limit for comparison to the $I_{\rm cmin}$ of the SQ1s when they are explicitly measured. The ratio of these values $I_{\rm ccol}/I_{\rm cmin}$ must display sufficient margin to ensure proper functionality and is used to determine device yield.

The determination of I_{ccol} uses a binary search algorithm of the full dynamic range of the SQ1 bias current. At the start of the test a periodic flux bias (multiple Φ_0 in amplitude) is applied to the SQ1FB, the SQ1B current is set to ½ full scale for all columns, and the FLL is closed on SAFB. Because the FLL is sensitive to input slew rate, a *sweep-to-bias* routine is utilized in all tests to constrain the bias-current slew rate and thus avoid flux jumps in the feedback signal. Once the bias current has settled, SAFB data is acquired for all channels of all MUXs simultaneously. These data are averaged, digitally filtered, and evaluated for the onset of modulation via a peak-detection algorithm. Following each bias step and dependent upon whether a particular column shows modulation, the SQ1B is stepped up or down by $1/(2^{\mathrm{step}})$ of the dynamic range of the bias circuit (where step is the step number in the sequence). Iterating this procedure down to the smallest resolvable bias step (limited by noise) results in an accurate determination of the I_{ccol} of each column of the DUT array. This does not determine which of the two MUX chips in the column exceeded I_{ccol}. However, as we are looking for a lower limit to this value it remains a valid yield indicator when determining pass/fail criteria.

The next phase of testing determines the optimal row select bias current to turn on the FAS. The flux-activated switch is a low-β_l array of SQUIDs whose I_{cmin} approaches zero. The application of a flux bias through the row-select line modulates the resistance of the switch. The resistance is periodic with the magnetic-flux quantum, and moves between superconducting at $\Phi_{\mathrm{applied}} = n\Phi_0$ and maximum resistance at $\Phi_{\mathrm{applied}} = n\Phi_0/2$, for integer values of n. For this test the SQ1B current is set below the expected minimum critical current of the 1st stage SQUIDs in the chip and the row-select current driving the switch-activation inductor is swept over multiple Φ_0. With the FLL closed on SAFB, data for all devices is acquired. As the applied flux sweeps through $\Phi_{\mathrm{applied}} = n\Phi_0/2$ where $I_{\mathrm{cmin,FAS}}$ is near zero, the small applied bias current causes substantial modulation in resistance leading to sharp peaks in the SAFB current centered at the optimal flux bias. As with the previous testing step, a combination of averaging, digital filtering, and peak detection allows extraction of the optimal bias current for each switch in all of the MUXs. This data set also yields values for the mutual inductance of the FAS-activation inductors, M_{FAS}, which is deduced from the period of the peaks in the response curve. The FAS-activation current is shared by all FASs in the same row. So, for the next measurement steps the row bias is set to the average value of the optimal bias of the switch elements in that row.

B. First Stage SQUID Characterization

The next phase of testing involves measuring the SQ1 response to applied flux over a range of current bias from zero to above the I_{ccol} of each column. From this large three-dimensional data set several parameters are derived. The most fundamental of these are the I_{cmin} and I_{cmax} of the SQ1s. The measurement applies a multiple-flux-quantum current stimulus to the SQ1FB line of each column, closes the FFL on the SAFB, and captures and analyzes data at each of 256 SQ1 current-bias values. Only the maximum and minimum values of current in the response to the flux sweep are recorded. After completion of the full bias sweep a 2nd analysis step determines the difference between these values and uses it to determine critical currents. I_{cmin} is the onset of modulation and I_{cmax} is the bias current at which the difference, or *modulation depth*, is maximized.

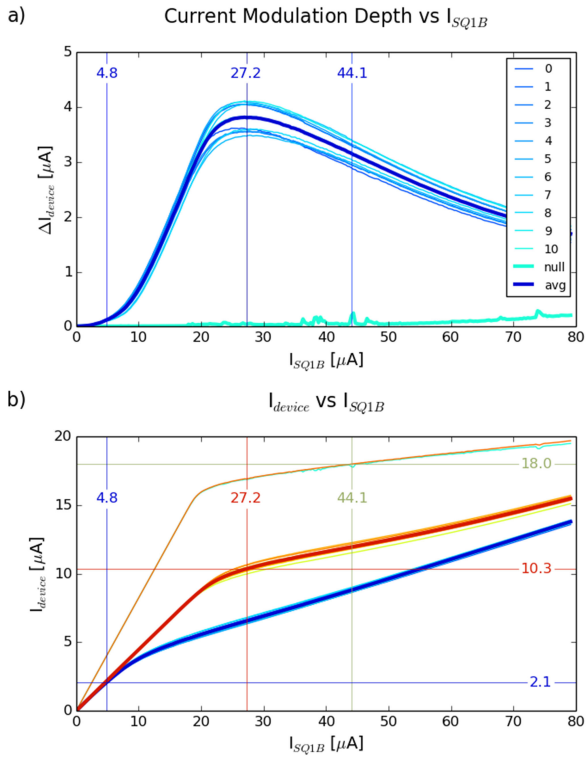

Fig. 3. 1st stage SQUID response to applied flux on SQ1FB line as SQ1 bias is stepped: (a) modulation envelope (difference between maximum and minimum current) vs. bias, (b) modulation minimum and maximum current vs. bias. Bold lines represent the average response from the 11 input stages of the device.

Typical data from the bias sweeps for an 11-channel FAS multiplexer is shown in Fig. 3. There are 12 sets of curves in each plot. Eleven of these are for activated SQ1s, in which a flux bias is applied to open the corresponding FAS. The twelfth curve set, which we call the *null row*, is acquired with none of the row switches addressed. The null row samples the response of the column of switches. In all plots that follow a bold line indicates the average response of the 11 channels on the chip.

Fig. 3a shows the modulation depth (I_{max} - I_{min}) vs. SQ1 bias and Fig. 3b shows the individual values I_{max} and I_{min} vs. SQ1 bias. Fig. 3a shows a uniform onset of modulation, a well-defined maximum modulation, and smooth modulation envelope for all 11 channels as the SQ1 bias is swept. The curve for the null row (11) shows low-level modulation emerging from the noise floor when none of the rows is activated. Fig. 3b offers additional insight as it plots the device current extrema vs. bias. The minima are represented in blue tones and the maxima in orange tones. The green/brown pair is the null row. Horizontal and vertical indices show the average values for the SQ1B and SQ1 device currents of the determined parameters. For the example in Fig. 3b, $I_{\mathrm{cmin}} = 2.1\ \mu$A at SQ1B $= 4.8\ \mu$A, $I_{\mathrm{cmax}} = 10.3\ \mu$A at SQ1B $= 27.2\ \mu$A, and $I_{\mathrm{ccol}} = 18.0\ \mu$A at SQ1B $= 44.1\ \mu$A.

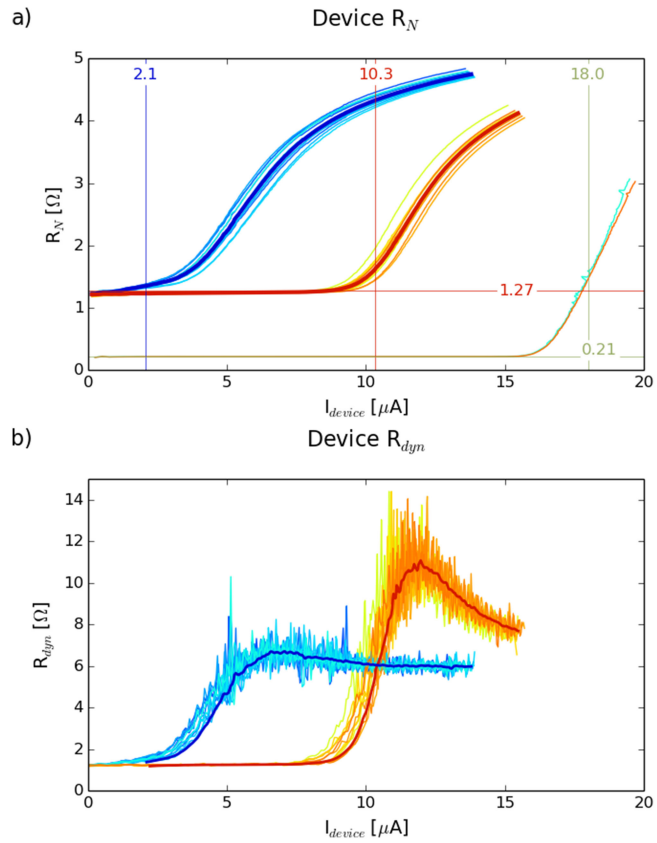

Fig. 4. 1st stage SQUID response to applied flux on SQ1FB line as SQ1 bias is stepped. Modulation minimum and maximum vs. bias: (a) normal resistance, (b) dynamic resistance.

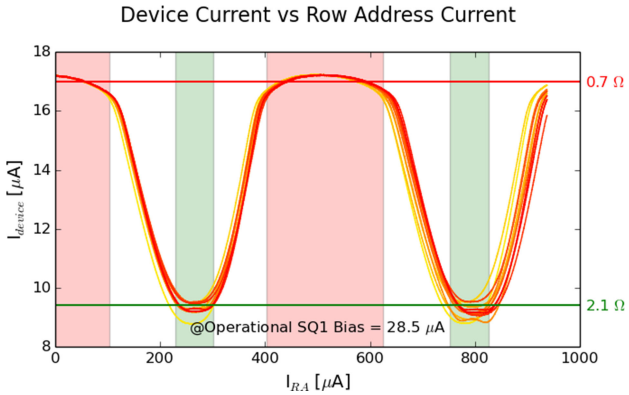

Fig. 5. FAS response to applied flux on row address at operational SQ1 bias. The bold line indicates the average response of the FAS.

A subtle phenomenon worth revisiting is expressed in the data for the null row in Fig. 3b. The superconducting branch is clearly visible as the linear slope rising from the origin. The curve deviates abruptly from this trend with the onset of normal resistance in the switch branch at a bias current of ∼19 μA. However, the detection of modulation on this branch does not occur until a bias current of 44.1 μA. This is a manifestation of the distributed resistance described earlier. As the applied current bias exceeds the I_c of individual SQUIDs in the switches resistance builds gradually across the device with this increasing current bias. Eventually, the current exceeds a threshold, $I_{\rm ccol}$, where sufficient current through one of the SQ1s forces it into the normal state and modulation is observed.

This same data set is manipulated to extract other relevant circuit parameters (see Fig. 2). For example, the current through the device is plotted against voltage: $V_{\rm device} = (I_{\rm SQ1B} - I_{\rm device}) * R_{\rm shunt}$. Likewise, the device resistance is explicitly deduced from this data. Fig. 4a is a plot of the extrema of a suite of $R_{\rm N}(I_{\rm device})$ curves. The critical-current values are overlaid as vertical indices on this plot. The $R_{\rm N}(I)$ plot shows two horizontal indices that are relevant to the analysis. The first, $R_{\rm para} = 0.21\,\Omega$, the slope of the linear region of the null-row data set in Fig. 3b, is the parasitic resistance in the device branch of the embedding circuit. This is non-zero due to normal-metal copper traces in the printed circuit boards, connector contact-resistance, and wire bonds between $R_{\rm shunt}$ and the DUT. It is a useful diagnostic of the status of the interface to the devices; if $R_{\rm para}$ is larger than expected the test results may be jeopardized or invalid. The second index at 1.27 Ω includes the series resistance in the SQ1 branches of the multiplexer circuit, $R_{\rm series} = 1.27\ \Omega - R_{\rm para}$. This is an engineered value determined by a PdAu thin-film resistor that is critical to the performance of the circuit. Fig. 4b plots the dynamic resistance, $R_{\rm dyn} = {\rm d}V/{\rm d}I$, of the DUT at the modulation extrema. $R_{\rm dyn}$ is relevant for projecting the dynamic response and noise performance of the DUT.

The extraction of $I_{\rm cmax}$ from this data set allows an informed choice of optimal bias of the SQ1s. The next phases of testing are performed at a pair of bias values that bracket those that would be used in operation with transition edge sensors (TESs): 110% and 140% of the maximum value of $(I_{\rm cmax})$ of the devices in the column.

The last tests in this group measure the SQ1 input mutual inductances, $M_{\rm in}$, and feedback mutual inductances, $M_{\rm fb}$. SQ1B is set to the 110% value, the FLL is closed on SAFB, and a multiple-flux-quantum sweep of the corresponding inductor is analyzed for periodicity to determine the respective M.

C. Device Characterization Under Operational Bias

A final set of tests is undertaken to evaluate device performance at the operating point. The first of these tests interrogates the FAS to assure its functionality and operating margins under full bias. This contrasts with the earlier measurement of optimal switch bias that occurred at a bias well below the operating point. In this test, the modulation of the device current is measured vs. flux applied to the FAS row-address line for each switch. A response curve for each switch is shown in Fig. 5. Horizontal indices indicate the resistance of the device branch in the OPEN and CLOSED states. In the CLOSED state the average parallel combination of the FAS and the corresponding SQ1 branch is 0.7 Ω. This value is dominated by the low resistance of the switch branch of the circuit and includes $R_{\rm para}$ as well as distributed resistance from low $-I_c$ elements in the switches. When the switch is OPEN, the average parallel combination is 2.1 Ω. This value is dominated by the low resistance of the SQ1 branch and includes $R_{\rm para}$, $R_{\rm series}$, and the normal resistance of SQ1 at its operational bias. Vertical shaded regions in red (CLOSED)

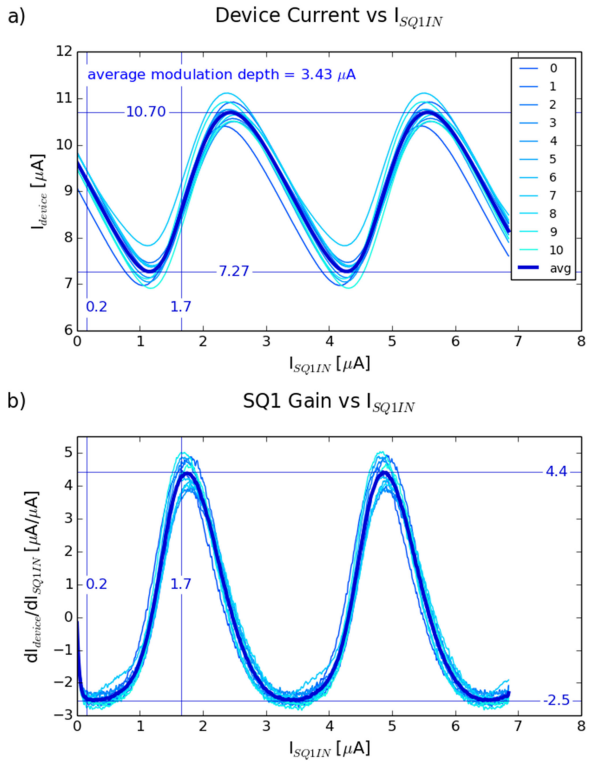

Fig. 6. SQ1 response to input modulation: (a) device current modulation, (b) device gain. Bold lines represent the average response across all 11 input channels.

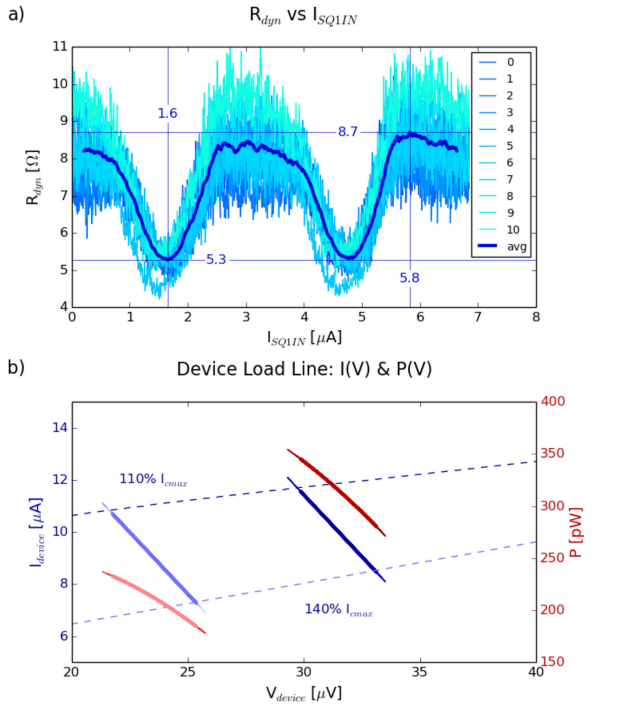

Fig. 7. (a) SQ1 dynamic resistance as a function of input current, (b) device load lines for full input modulation the $I(V)$ plane (blue) and $P(V)$ plane (red). Bold lines represent the average response across all 11 input channels.

and green (OPEN) show the range in row-address current over which these switch states are considered valid.

Next, SQ1 current modulation vs. flux applied to SQ1FB is measured for all devices (Fig. 6a). The plot is annotated to show the range of the average current modulation as well the average modulation depth. The asymmetry in the response curves is due to intentional self-feedback from the bias line to the SQ1 loop. This leads to different values of gain and noise on the steep and shallow slopes. The numerical derivative plot of this data is shown in Fig. 6b. The maximum average gain is 4.4 μA/μA on the steep slope and -2.5 μA/μA on the shallow slope. In the eventual TES application, the SQ1 can be configured to operate on either of these slopes by manipulating the polarity of the loop gain in application of feedback in the FLL.

A final measurement determines the range of $R_{\rm dyn}$ at the operational bias (Fig. 7a). This test is done via differencing of two data sets taken with a small offset in bias about the operating point. The plot indicates the range of average dynamic resistance and the input currents at which the average, minimum, and maximum $R_{\rm dyn}$ occur.

Lastly, Fig. 7b shows the data from Fig. 6a recast as device $I(V)$ and plotted as an operational-bias load line as a function of input current. This plot includes curves acquired at 110% and 140% of the column-maximum value of $I_{\rm cmax}$. Power, $P = I * V$, on the load line is plotted on the second y-axis. This is particularly useful for estimating power dissipation in the cryogenic focal plane of the eventual TES instrumentation [9].

V. Quality Assurance

The completion of these tests on a batch of devices is followed by a comparative analysis of device properties. A separate program is executed to plot and tabulate the results. For each device, this program generates a report that includes the plots above (in addition to others) and outputs a spreadsheet with tabulated results. Test results can also be analyzed in a mode that compares devices by generating surface plots of parameters across the samples. A plot of $I_{\rm cmin}$ and $I_{\rm cmax}$ of a batch of 20 devices is shown in Fig. 8. This is particularly useful when sorting devices into well matched allotments to fill a subarray of a focal plane. This mode can also be employed to investigate fabrication trends by comparing devices between wafers, or within a single wafer.

VI. Future Wafer-Scale Technologies

While the current system and protocols offer substantial improvements over earlier methods, there remains room for improvement in efficiency. Currently our throughput is limited by sample preparation and thermal cycling. Wafer-scale testing could reduce these bottlenecks. We are currently experimenting with the following cryogenic wafer-scale-testing concepts for future devices.

A. Automatic Cryogenic Probe Station

In collaboration with a commercial vendor, we are developing a wafer-scale cryogenic-probe station. This system will allow mounting of up to a 150 mm-diameter wafer on a motion-controlled stage, in vacuum, with cooling to $\sim$4 K. The device interface will be a tungsten-tip ceramic-ring probe card

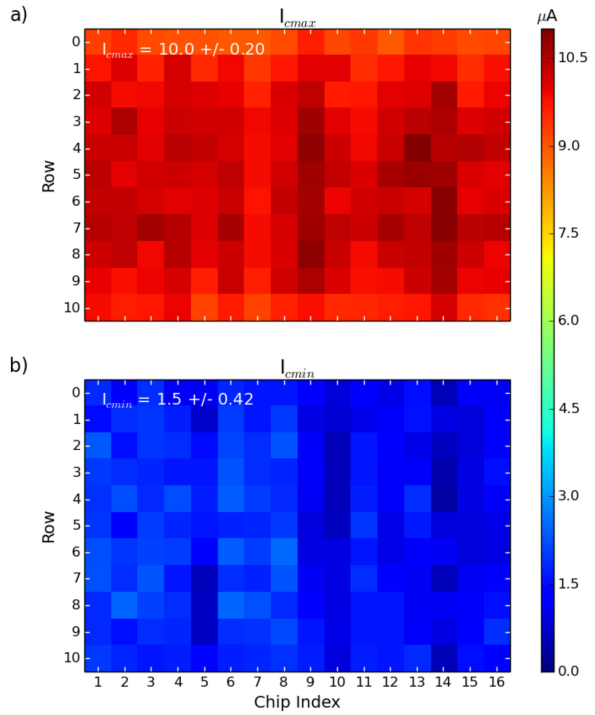

Fig. 8. Critical-current surface plots for a batch of 16 SMUX: (a) I_{cmax}, (b) I_{cmin}.

based on conventional room temperature probe card technology with slight modifications for operation at cryogenic temperatures. Optical access via a cold shutter will allow initial device alignment. At 4 K, an automated step-and-measurement procedure will return a full suite of measurements for every die on the wafer.

The system has been designed and assembled and is currently undergoing acceptance testing. A probe card has been designed and is under assembly. Integration of these components is expected to occur over the coming months. If successful, this system will entirely avert the need for mounting and wire bonding individual dies. Although a single test cycle will be slower than in the current liquid-helium dip system, overall throughput will improve as the number of devices tested per cycle will increase dramatically.

B. Micro-Spring-Pin Concept

A future concept to transcend the limitations of ceramic-ring probe cards is based on micro-spring-pin technology. Probe cards have an array of metallic probe tips mounted around the perimeter of a ceramic probe ring that is affixed to a PCB for interconnection and fan out. This form factor prevents extensive interconnection in the central region of the probe ring and so constrains the fixture to a single-device footprint. Micro-spring-pin fixtures represent a potential solution to this barrier.

We have worked with a vendor to design a cryogenically compatible spring pin. This pin is compact at 3.72 mm in length and 0.231 mm in diameter and can be situated in a capture fixture on 0.200 mm centers. Our intent is to micromachine a capture fixture out of silicon wafers with retention features tailored to the device profile. The holes for the micro-spring pins will align with device pads at one interface surface and with fanout PCB pads on the other. A fixture to align and stack the DUT, micro-spring-pin fixture and PCB is under design. Prototype fixtures are planned for single devices. If successful, structures will be adapted for meta-device scale (pre-diced contiguous groups of devices) and, ultimately, wafer scale testing. This will allow the full efficiency benefits from both wafer-scale and array-format testing and maximize testing throughput.

VII. Conclusion

The main challenge in implementing an automated test system is ensuring repeatable measurement results and reliable data products. We have presented a testbed based on custom hardware and software that satisfies this challenge. At the core of the software are algorithms for parameter extraction that are both robust (e.g., in the presence of EMI) and easily reconfigurable for adaptation to other classes of devices. The system and supporting infrastructure allow fast-turnaround, high-throughput testing of SMUX devices. This has allowed us to keep up with the strong demand from the research community for high-performance cryogenic-readout components. Our most recent collaborations include SPIDER, HIRMES, CLASS [10], TIME-Pilot, and Athena [11].

As cryogenic-readout technologies evolve, and the size of detector arrays continue to grow, new systems and techniques will need to be developed that scale in efficiency and throughput with the demand. We look forward to this challenge with the advancement of prototype systems and new concepts.

References

[1] J. A. Chervenak, K. D. Irwin, E. N. Grossman, J. M. Martinis, C. D. Reintsema, and M. E. Huber, "Superconducting multiplexer for arrays of transition edge sensors," *Appl. Phy. Lett.*, vol. 74, no. 26, pp. 4043–4045, Jun. 1999.

[2] P. A. J. de Korte *et al.*, "Time-division superconducting quantum interference device multiplexer for transition-edge sensors," *Rev. Scientific Instrum.*, vol. 74, no. 8, pp. 3807–3815, Aug. 2003.

[3] S. W. Henderson *et al.*, "Readout of two-kilopixel transition-edge sensor arrays for advanced ACTPol," presented at the Conf. Millimeter, Submillimeter, and Far-Infrared Detect. Instrum. Astron. VIII, Edinburgh, Scotland, Jul. 2016, vol. 9914.

[4] C. D. Reintsema *et al.*, "Prototype system for superconducting quantum interference device multiplexing of large-format transition-edge sensor arrays," *Rev. Scientific Instrum.*, vol. 74, no. 10, pp. 4500–4508, Oct. 2003.

[5] C. D. Reintsema *et al.*, "Electronics for a next-generation SQUID-based time-domain multiplexing system," in *Proc. 13th Int. Workshop Low Temp. Detectors*, Stanford, CA, USA, 2009, vol. 1185, pp. 237–240.

[6] W. B. Doriese *et al.*, "Developments in time-division multiplexing of X-ray transition-edge sensors (vol 184, pg 389, 2016)," (in English), *J. Low Temp. Phys.*, correction vol. 184, no. 1–2, pp. 396–396, Jul. 2016.

[7] J. Beyer and D. Drung, "A SQUID multiplexer with superconducting-to-normalconducting switches," (in English), *Supercond. Sci. Technol.*, vol. 21, no. 10, Oct. 2008, Art. no. 105022.

[8] H. H. Zappe, "Josephson quantum interference computer devices," (in English), *IEEE Trans. Magn.*, vol. MAG-13, no. 1, pp. 41–47, 1977.

[9] W. B. Doriese *et al.*, "Optimization of time- and code-division-multiplexed readout for athena X-IFU," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 5, Aug. 2019, Art. no. 2500305.

[10] T. Essinger-Hileman *et al.*, "CLASS: The cosmology large angular scale surveyor," in *Conf. Millimeter, Submillimeter, Far-Infrared Detect. Instrum. Astronomy VII, BELLINGHAM: SPIE-Int Soc Optical Eng., 2014*, Montreal, Canada, 2014, vol. 9153.

[11] M. Durkin *et al.*, "Demonstration of athena X-IFU compatible 40-row time-division-multiplexed readout," to be published, doi: 10.1109/TASC.2019.2904472.