Metrology Requirements for Next Generation of Semiconductor Devices

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INTRODUCTION

The first International Roadmap for Devices and Systems (IRDS)[1] was published in 2018 and builds on the decades-long effort by the International Technology Roadmap Semiconductors (ITRS). The IRDS Metrology Chapter identifies emerging measurement challenges from devices, systems, and integration in the semiconductor industry and describes research and development pathways for meeting them, covering the next 15 years[1]. This includes, but is not limited to, measurement needs for extending CMOS, accelerating beyond CMOS technologies, novel communication devices, sensors and transducers, materials characterization and structure-function relationships.

Although devices based on traditional CMOS architectures are expected to reach their physical limits in the next few years, the devices and materials involved are more complex and difficult to measure than ever before[2]. The nanoscale sizes mean that the same fundamental limitations that will affect device performance also affect available metrology methods[3]. In addition to nanoscale size and complex structure, next generation devices will incorporate new materials such as graphene and transition metal dichalcogenide films. Because of changes in materials properties, measurements of film thickness and other parameters will require considerably more information about the layer-dependent material properties. This could be challenging for existing metrology techniques. The presentation will outline some of the key materials and lithography metrology challenges and highlight promising new techniques in an era of not only increased complexity, but one where scaling is no longer the main industry driver.

DEVICE AND LITHOGRAPHY OPTIONS

With the proliferation of non-planar device architectures, a key challenge for metrologists has been to develop the techniques required to obtain full three-dimensional device structure information. The introduction of gate all around (GAA) structures (lateral GAA and vertical GAA) and monolithic 3D structures[4] would make this even more challenging. Some of the challenges of GAA include small target volumes, localized information, and low signal to noise ratios. In addition to the above issues, monolithic 3D has the problem of non-uniform sensitivities at different depths. This means that metrology solutions would need to have a large depth of focus or be transmissive. In addition, 3D stacked chips and 3D very large-scale integration (3D VLSI) are fully functional tiers, so destructive characterization would be prohibitively expensive. Table 1 lists some of the device and lithography metrology challenges.

Beyond classical CMOS, most of the proposed device candidates, such as 1D-2D field effect transistors, lateral and vertical heterostructures, include the use of 2D materials (such as graphene and molybdenum disulfide), which are susceptible to beam damage. In addition to complex device structures, specific lithography options have their own challenges; for example, extreme ultra-violet (EUV) lithography has problems with mask defectivity, line-edge roughness and stochastics. Nanoimprint lithography's metrology challenges include defectivity, overlay, and template inspection. In addition to defect inspection, directed self-assembly has unique challenges with overlay and defectivity.

Preprint

TABLE 1. Device structure and lithography metrology challenges

	Lateral Gate All Around	Vertical Gate All Around	3DVLSI/ Monolithic 3D
Patterning	193i, EUV	193i, EUV	193i, High NA, EUV+(DSA)
Channel Material	Ge, IIV(TFET)	Ge, IIV(TFET)	Ge, IIV(TFET) 2D Materials
Metrology Challenges (Select Examples)	• Small target volumes. • Localized information • Low SNR. • Non-uniform sensitivities	• Small target volumes. • Localized information • Low SNR. • Non-uniform sensitivities • Future metrology techniques may be destructive.	• Different materials on multiple levels. • Low contrast materials • Small target volumes. • Localized information • Low SNR. • Non-uniform sensitivities at different depths. • Nonsystematic DSA overlay shift. • Potential beam damage. • Low image contrast • Reduced cross-scattering due to small sizes • Difficulty obtaining optical properties (*n* & *k*)

DSA, directed self-assembly; TFET, tunnel field-effect transistor; SNR, signal-to-noise ratio; NA, numerical aperture

	<- - Imaging Techniques				Spectroscopic Technique - ->				
Application	Critical Dimension-scanning electron microscopy (CD-SEM)	Environmental SEM/ LLBSE-SEM/ HV- SEM	Helium Ion Microscopy	Critical Dimension Atomic force microscopy (CD-AFM)	Optical Critical Dimension (OCD)	Transmission -SAXS	Grazing-Incidence - SAXS	Through focus scanning optical microscopy (TSOM)	Model based Infra-red (MBIR)
2D/3D Lithography	7/5 * shrinkage, needs profile	severe shrinkage	severe shrinkage	14, dense; <5, isolated.	7/5 * thin PR, small CD, n&k	≤ 5	≤ 5	needs study	
2D Planar Etch & Multiple patterning	7/5 * needs profile	5 * needs profile	≤ 5 * needs profile	14, dense; <5, isolated.	7/5 * small CD, n&k, complex periodicities	≤ 5	≤ 5	simulations predict -maybe	needs study
2D + Multiple planar etch	7/5 * needs profile	5 * needs profile	≤ 5 * needs profile	14, dense; <5, isolated.	7/5 * small CD, n&k,	≤ 5	≤ 5	simulations predict -maybe	needs study
3D finFET & nanowire	7/5 * needs profile	5 * needs profile	≤ 5 * needs profile	14, dense; <5, isolated.	7/5 * small CD, n&k,	≤ 5	≤ 5	needs study	needs study
3D High Aspect Ratio (HAR)	7/5 * needs profile	7 *	14 *	No tip access to HAR	7/5 * small CD, n&k, large depth limit?	≤ 5	Beam samples ≤ 400 mm depth	simulations predict -maybe	10 * no depth limit

Color Key:
≤5 nm limit
5 nm limit
7 nm limit
10 nm limit
14 nm limit
≥22nm node limit
not possible
unknown
sims predict maybe

FIGURE 1: Lithography metrology gaps and limits. Continuous improvement and combined use of multiple methods could extend the applicability of some of these techniques[5-8]. All values are in nanometers; color key refers to limits of measurement techniques; LLBSE, low loss back-scattered electrons; SAXS, small angle x-ray scattering, HV, high voltage; Figure courtesy of B. Bunday[9].

POSSIBLE METROLOGY SOLUTIONS

Progress has been made in addressing many of the challenges listed in Table 1, but there continues to be the need for an additional broad range of metrology solutions commensurate with the complexities of the problems[5, 10]. Figure 1 shows metrology capabilities and approximate size limit needs for a wide range of lithography applications. The range of measurements needed to characterize different aspects of 3D features means that a wide variety of tools and instruments are required[11]. No single technique has the needed resolution, range, and low levels of uncertainty required to enable it to fully characterize these features.

A metrology approach that is gaining wider application is hybrid metrology, which relies on the complimentary use of multiple instruments. Figure 2 shows a conceptual diagram of multiple instruments being used to characterize a device. Each technique shown (scanning electron microscopy[2, 6], atomic force microscopy[12, 13], critical dimension x-ray scattering[14], scatterometry[15], and transmission electron microscopy[16, 17]) provides a specific capability[18] that the others do not have. In addition to multiple instruments, hybrid metrology also includes the use of statistical and combinatory techniques[19] that allow complementary analysis of the same features using the best measurement attributes of each technique.

Other promising methods include the use of ptychography-based methods to enhance electron, optical and X-ray based methods. Electron ptychography techniques were recently demonstrated for imaging 2D materials without causing beam damage, achieving a resolution of 0.04 nm[20]. At a larger length scale, X-ray ptychography methods were recently used to image and reconstruct whole chips with a resolution of 14.6 nm over a 10 μm range[21].

Machine learning and other advanced analytics[22] techniques are gaining wide application in metrology[2]. This goes beyond data analysis and classification, and extends to instrument and measurement process optimization, including hybrid and virtual metrology.

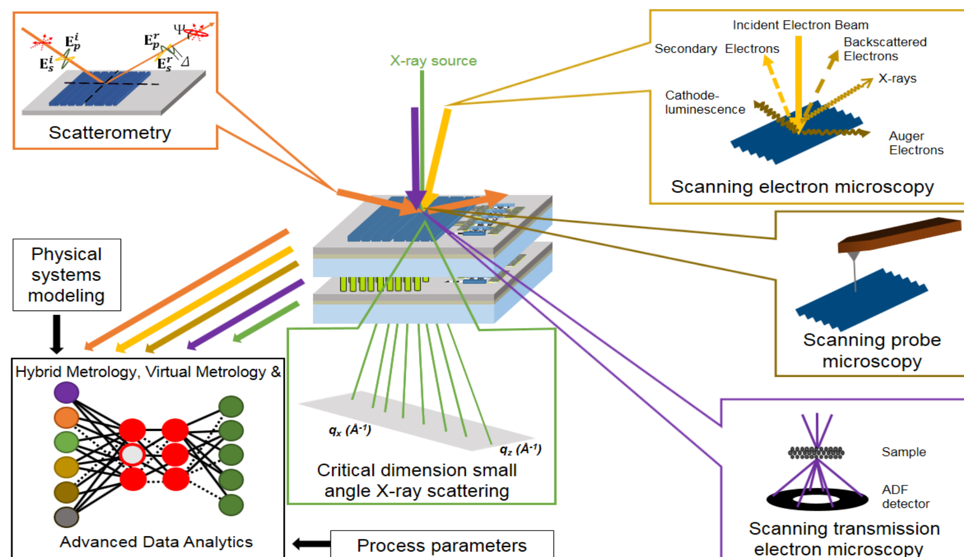

FIGURE 2: Multi-Instrument evaluation of a 3D stacked chip. Increasingly, advanced data analytics plays an increasingly major role in synthesizing information from multiple instruments[23-30] and process parameters. Figure courtesy of G. Orji and B. Barnes[2].

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KEYWORDS

Semiconductor metrology, gate all around. 3D VLSI, nanometrology