Characterization of Uniformity in $Nb/Nb_xSi_{1-x}/Nb$ Josephson Junctions

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***Abstract*—The uniformity of the barriers in Josephson junctions (JJs) is a critical parameter in determining performance and operating margins for a wide variety of superconducting electronic circuits. We present an automated measurement system capable of measuring individual JJs across a 1 × 1 cm die at both ambient temperature and 4 K. This technique allows visualization of the spatial variation over a large area of the critical electrical properties of the junctions and allows for the direct correlation between room-temperature (RT) resistance and low temperature properties. The critical current variation of Nb_xSi_{1-x} ($x = 15\%$) barriers is found to be about 2.6% (one standard deviation) for 1024 junctions across an individual die and only weakly correlates with RT resistance measurements.**

***Index Terms*—Josephson arrays, process control, superconducting device testing, thin-film devices.**

I. Introduction

SUPERCONDUCTING electronics based on different types of Josephson junctions (JJs) are currently in use for applications that include digital single-flux quantum (SFQ) computing [1], [2], quantum computing [3], ac and dc voltage standards [4], [5], and more recently, neuromorphic computing [6], [7]. In these applications (with the possible exception of neuromorphic computing), it is necessary that the electronic properties, most notably the critical current density, J_c, of individual junctions are uniform over the desired circuit area and, ideally, also across wafers and from fabrication run-to-run. Variations in J_c can reduce the operating margins for digital SFQ circuits and, in the case of the Josephson voltage standard, even one junctions out of several hundred thousand with anomalous J_c can cause the chip to be "nonyielding" [8]. It is, therefore, important to have process control monitors (PCMs) that can accurately predict the expected variance in J_c across an area ranging from a single die up to an entire wafer.

The need to have tight control over J_c is well known in the superconducting electronics community, and room-temperature (RT) tests are routinely done to predict low temperature properties. One of the most widely used techniques is to perform RT 4-point resistance measurements on arrays of cross-bridge Kelvin resistor (CBKR) structures [9]–[11]. By measuring the resistance of junctions of various sizes, lithographic runout can be estimated, and the variance in barrier resistivity extracted. If one assumes that the RT conductivity is directly proportional to the critical current density, then the RT measurements of resistance should be a good PCM for monitoring J_c. There are physical arguments, i.e., the physics and temperature dependence of tunneling conductivity, for why RT measurements of the barrier conductivity of junctions should be proportional to the critical current density [12], [9], and studies on $Nb/AlO_x/Nb$ junctions have analyzed the accuracy of this method. One previous study [13] has investigated Nb–Nb via junctions using CBKRs. However, no previous studies have looked at the validity of this method for superconductor-normal-superconductor (SNS), junctions, which have conduction mechanisms that are not dominated by electron tunneling in the normal state.

Another commonly used method to quantify junction J_c uniformity is to acquire a current-voltage *(IV)* curve for a serially-connected array of many junctions, typically hundreds or thousands [14]. Statistics can be obtained by quantifying the voltage steps observed as junctions consecutively exceed their critical-current, I_c, with increasing bias current by assuming a constant step in voltage when each individual junction in the series transitions to the voltage state. By binning the current value at each transition, and then, counting the voltage steps, a histogram can be made and statistics on I_c for the array can be determined.

While both previously mentioned methods have been used with success in analyzing variations in J_c for tunneling barriers, most notably, $Nb/AlO_x/Nb$ barriers that have a well-defined transition to the gap voltage and rely on electron tunneling as the conduction mechanism, they will not work for SNS junctions such as those used in the NIST Josephson voltage standard. It should be noted that these junctions have much lower I_cR_n product, where R_n is the normal resistance of the junction, as well as large J_c compared to more typical superconductor-insulator-superconductor (SIS) junctions used in electronic applications. The transition of an SNS junction to the voltage state does not

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feature a jump to a relatively sharp gap voltage, but smoothly switches to the voltage state. The *IV* characteristics for these junctions can be expressed as $V = R_n\sqrt{I^2 - I_c^2}$ for $I > I_c$ [15]. This fact precludes the use of junction arrays to quantify J_c and develop statistics. Another perhaps subtler issue lies in the fact that junctions that are better described as SNS, have a much lower specific barrier resistivity compared to SIS, tunnel junctions. For example, the specific barrier resistivity (ρ_c) of the junctions in this paper is around 0.085 $\Omega{\cdot}\mu$m^2, which is more than two orders of magnitude lower than that of typical AlO_x barrier junctions. This lower barrier resistivity means that, even in a 4-point geometry, RT measurements of barrier resistance will be dominated by the parasitic spreading resistance in the Nb leads around the junction with the alignment tolerances available to us. If more advanced lithography were used and the top and bottom electrode could be fabricated to be almost the exact size as the junction, then the spreading resistance would again be negligible.

In this paper, an automated variable temperature probing station was used to measure RT resistivity as well as 4 K critical current and normal resistance for individual JJs laid out on a 1 cm $\times$ 1 cm die. This method allows us to directly measure individual junctions at RT and 4 K. We, then, perform statistical analysis of the measured ensembles and directly compare the RT and 4 K properties of each individual junction. As mentioned in the previous paragraph, it is not clear that there should be a direct correlation between RT measurements of resistance and I_c for the junctions used in this paper. Additionally, this method has the advantage that it allows for mapping and visualization of electrical properties of the barrier over a large area. These facts along with the relatively small amount of time required to probe at 4 K and the data presented in this paper, indicate that testing of individual JJs at 4 K can be a valuable PCM for future superconducting circuit fabrication and that it is necessary to obtain valid statistics at 4 K for Nb_xSi_{1-x}-barrier junctions as well as any other junctions with low ρ_c barriers.

II. Experiments and Results

A. Nb/Nb_xSi_{1-x}/Nb CBKR Fabrication

The chip design consisted of 1024 nominally identical CBKR arranged in a 32 $\times$ 32 array on a 1 $\times$ 1 cm die. A schematic of the individual CBKR devices is shown in Fig. 1. The drawn area of the barrier was 2.9 μm^2 and the RT sheet resistance of the Nb leads was 0.25 $\Omega/\square$ for the top electrode, and 0.75 $\Omega/\square$ for the bottom electrode. For all of the junctions fabricated, the NIST voltage standard process [16] was used with the modification that only a single barrier, with composition $Nb_{0.15}Si_{0.85}$ and a thickness of 30 nm, instead of the usual a triple barrier stack was deposited.

B. RT Measurements

Four-wire resistance measurements were performed using a current source and a lock-in amplifier. The ac current excitation was 500 μA rms at a frequency of 97 Hz. The low frequency of the measurement was chosen to avoid any potential parasitic capacitive effects from the junctions or cabling. Probing an individual junction took approximately 1 s, the time required for the lock-in to settle with a 100 ms time constant and 24 dB per octave roll-off. Multiple measurements of the same die were performed, and the repeatability of the measurement was better than 0.5%. The mean barrier resistance for the single die reported in this paper was 223 mΩ and the standard deviation was 4.35 mΩ (2%), assuming a normal distribution, shown in Fig. 2(a).

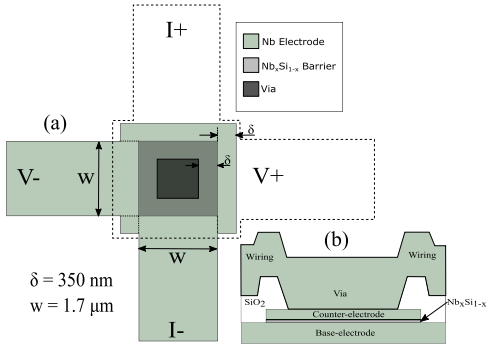

Fig. 1. (a) Layout of a CBKR studied in this paper. The top elecctrode is drawn wider for clarity. In the actual fabricated devices both electrodes had the same nominal dimensions. (b) Cross-section of a device in this paper. The via + counter electrode thickness was 450 nm.

The magnitude of the spreading resistance in CBKR structures can be estimated by

$$R_{\text{measured}} = \frac{\rho_c}{A} + \frac{4R_{sh}\delta^2}{3W^2}\left[1 + \frac{\delta}{2\,(W-\delta)}\right] \qquad (1)$$

where ρ_c is the specific barrier resistivity, R_{sh} is the sheet resistance of the Nb electrodes, δ is the via surround dimension required for high junction yield for the specific lithographic process, *A* is the junction area, and *W* is the width of the junction [17]. A schematic of the CBKR along with the geometrical parameters are shown in Fig. 1. It should be noted that this equation was originally derived for semiconductor contacts where the resistance of the top electrode was much less than the bottom electrode. For the structures in this study, the sheet resistances of both electrodes are similar, and both contribute significantly to the measured resistance. It is, therefore, reasonable to assume that there will be two spreading resistance terms, one for the top electrode, and one for the bottom electrode, with the sheet resistances different for each electrode. There is also a difference in geometry for the top electrode compared to the bottom electrode. In the top electrode, the current must travel through 2δ compared to δ for the bottom electrode.

For these low barrier resistance junctions, the via and the counter electrode will add yet another parasitic resistance term to the overall resistance measured. For the specific devices studied, the via resistance is estimated to be approximately 45 mΩ, which is similar to the junction resistance.

The contribution to the overall junction resistance of both the nominal barrier resistance as well as the parasitic spreading resistance from both electrodes as a function of ρ_c and including the via + counter electrode resistance is shown in Fig. 3. For the junctions in this study, the spreading resistance of the top

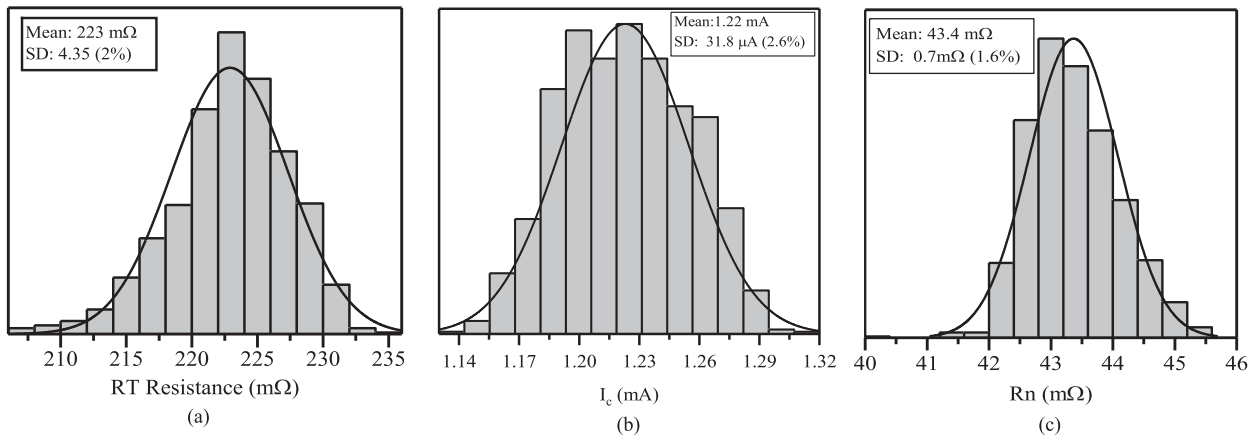

Fig. 2. Statistical distribution of the 1024 JJs measured. (a) RT resitance measurements with a mean resitance of 223 mΩ and a standard deviation of 2%. (b) Distribution of *Ic* with a mean of 1.22 mA and standard deviation of 31.8 μA. (c) Normal resistance measured at 4 K with a mean value of 43.4 mΩ and standard deviation of 1.6%. The solid curve is a fit of a normal distribution.

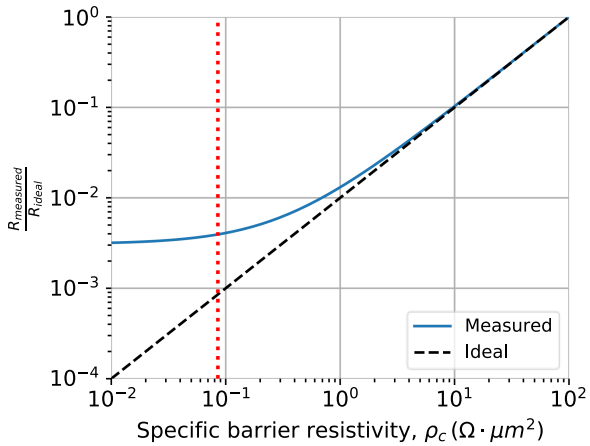

Fig. 3. Plot of measured resistance versus ideal barrier resistance for a KBCR structure with $R_{\rm sh} = 0.75\ \Omega/\square$ (top-electrode), $R_{\rm sh} = 0.25\ \Omega/\square$ (bottom-electrode), and $R_{\rm via} = 45\ \mathrm{m}\Omega$, compared to the specific barrier resistivity. The red line corresponds to the specific resistivity for the junctions in this paper ($0.09\ \Omega\cdot\mu\mathrm{m}^2$). *W* and δ are given in Fig. 1 and a via + counter-electrode depth of 450 nm were used for the calculation.

electrode is 76 mΩ, the bottom electrode 47 mΩ. Therefore, the total parasitic resistance is approximately four times the barrier resistance. It should also be noted that the calculated resistance value for these devices is 217 mΩ, in an excellent agreement with the measured decives.

Additionally, the magnitude of the spreading resistance varies with junction size and is very sensitive to small changes in δ. A more complete analysis was performed using a physics-based finite-element analysis program and showed similar results.

C. Cryogenic Measurements

Cryogenic measurements were performed in a liquid He flow cryostat where the sample as well as the probe positioners are at the same base temperature of 4 K, ensuring that the probes do not locally heat the junction under test. This is a distinct advantage of this system compared to probe stations where the positioners are connected to RT via a mechanical linkage. Additionally, the sample temperature and/or probe temperature could be set between 3.5–300 K. An optical port above the sample allows for direct viewing of the chip as well as the probes, using a microscope and a computer. The piezoelectric positioners used here do not have position encoders, so the position of the probes was monitored and controlled using a machine vision software developed at the NIST. The machine vision allows us for up to four arbitrary probes to be automatically positioned over any chip under test. The accuracy of the positioning is determined by the optical setup and specific image sensor used and was approximately 3 μm for the 5-mm field of view used during probing.

The procedure for measuring the individual junction parameters is important because the effects of photonic excitations, flux-trapping, and temperature variation must be mitigated. The junction measurement procedure was as follows. The 4-point probes are moved to an individual junction, and then, brought into contact. After landing the probes on each junction an optical shutter was closed to ensure that no heating from the microscope illumination or quasiparticles formation affected the measurement. After closing the shutter, the sample was heated to 10 K for 2 s to remove trapped magnetic flux from the chip. This step was necessary to obtain consistent measurements and was the most time-consuming step in the probing, requiring 1 min to heat, and then, settle to 4 K. The temperature was controlled using a heater to stability better than 2 mK. This level of temperature stability was required to obtain consistent results because the I_c of Nb_xSi_{1-x} junctions is strongly dependent on temperature around 4 K, approximately 1% change in I_c per 10 mK. An *I–V* curve was acquired for each device and the relationship from [15] was used to fit the data and extract I_c and R_n for each device.

Probing of all 1024 junction took around 18 h. To verify that the measurement and analysis procedure were providing accurate results, a single junction was measured 100 times using the full procedure of landing the probes, heating, and obtaining an *I-V* curve. The standard error of I_c for the 100 trials was 0.07%. Additionally, multiple individual junctions were measured several times and in different cooldowns and the repeatability was better than 0.5% after mounting and unmounting the sample.

The statistical distributions of the RT and 4 K measurements are summarized in Fig. 2(a) and (b). The mean value of I_c, shown

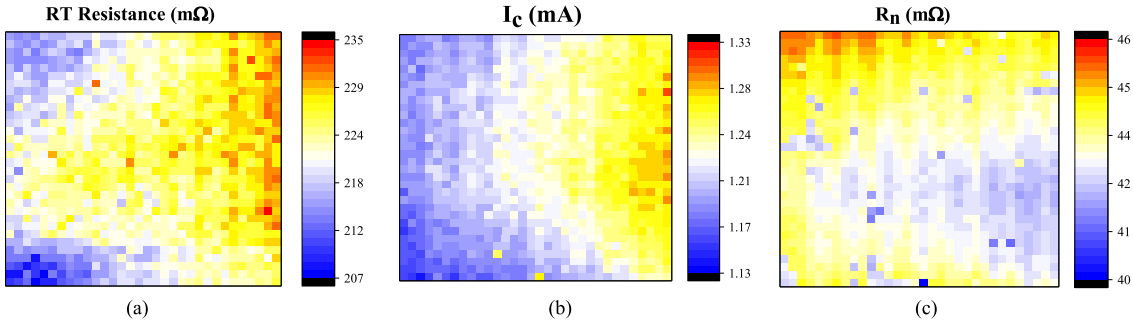

Fig. 4. Spatial distributions over a 1 × 1 cm die of (a) RT resitance, (b) critical current *Ic*, and (c) normal resitance, R_n, at 4 K. Each square is an individual JJ in the 32 × 32 array.

in Fig. 2(b), is 1.22 mA with a standard deviation of 31.8 μA (2.6%). This corresponds to a mean $J_c = 41.4\,\mathrm{kA/cm^2}$, which is large compared to a typical SIS junction. The mean of the normal resistance measured at 4 K is 43 mΩ with a standard deviation of 700 $\mu\Omega$ (1.6%). This corresponds to a mean $I_cR_n = 52.5\,\mu$V, which is small compared to SIS junctions. All three distributions can reasonably be fit to a normal distribution.

The barrier resistivity of these junctions has very little temperature dependence from 300 to 4 K and slightly increases as the temperature decreases [18]. When the JJ is in the voltage state, the Nb leads are still superconducting. This means that the measurement of R_n is not affected by the parasitic spreading resistance and gives an accurate measure of the barrier properties. The ratio of the mean of R_n to the mean of the RT resistance is 0.19, in a good agreement with (1), modified to include the contribution from both electrodes and via + counter-electrode, that predicted that at RT the barrier resistance would account for 0.21 of the measured resistance.

Probing each junction across the 1 × 1 cm die also allows us to plot and visualize how the parameters are changing spatially. Fig. 4 shows the spatial distributions of the same three parameters (*RT R*, I_c, 4 K R_n) plotted as histograms in Fig. 2. Fig. 4(a) shows that the minimum RT resistance measurements are in the lower left corner of the die with a trend to higher resistance value further right on the chip. A similar trend is also observed in the critical current values, shown in Fig. 4(b), with consistently lower I_c on the left side of the chip and higher values on the right. An opposite trend is observed in the R_n measurements, shown in Fig. 4(c), with the highest value in the upper left of the chip and trending to lower values in the right. Being able to visualize the spatial variation of key junction parameters is immensely useful and it is immediately obvious that there appears to be a direct correlation between the RT resistance and I_c of individual junctions. It also appears that there may be an inverse correlation between the RT resistance and R_n.

To more directly investigate how the RT measurements, correlate with I_c and R_n, I_c is plotted versus RT resistance in Fig. 5. Here we can see that there is indeed a statistically significant correlation (with a bivariate correlation = 0.78) between the RT resistance and the critical current for individual junctions. The critical current of Nb_xSi_{1-x} junctions, as well as the barrier resistivity, is determined by three main factors: junction area, Nb doping concentration, and barrier thickness. We would expect higher I_c (lower resistance) for larger junctions, thinner

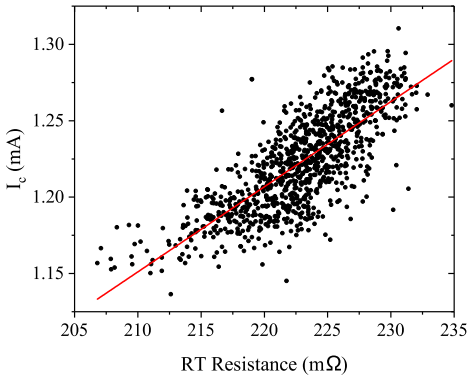

Fig. 5. Plot of I_c versus RT resistance. I_c exhibits a weak correlation with the RT resistance, which is the opposite behavior expected. Red line is a linear fit for the data.

junctions, or higher Nb doping. One possible explanation for the opposite correlation observed in the data is that there are two opposing factors affecting the measured RT resistance and the critical current. Looking at the RT resistance spatial distribution in Fig. 4(a), there is a trend of lower resistance in the bottom and top left trending to higher resistance in the right of the chip. This trend in resistance can possibly be explained by a process variation, such as a small difference in the drawn sizes on the reticle, or minor differences in focus resulting in the junctions on the right of the die having slightly larger junction size or δ, compared to the left side. If simultaneously there is a nonuniformity in the deposited Nb_xSi_{1-x} barrier resulting in either higher doping or thinner junctions towards the right of the chip, where the measured resistance is higher, then the observed correlation between I_c and the RT resistance would result. An alternate explanation is that both the junction and the electrode are thinner in the upper right-hand side of the chip. The thinner electrode would result in a higher measured resistance while the thinner barrier would result in larger I_c.

We also plot the correlation between the RT resistance and R_n at 4 K, shown in Fig. 6. Here there is an inverse correlation between the two variables (bivariate correlation = −0.35) as expected, because I_c is inversely correlated to R_n. The lower value of the bivariate correlation is a result of the bivariate correlation between I_c and R_n of −0.41. As mentioned earlier, the RT resistance measurement is dominated by the spreading resistance term. The spreading resistance is most sensitive to the difference

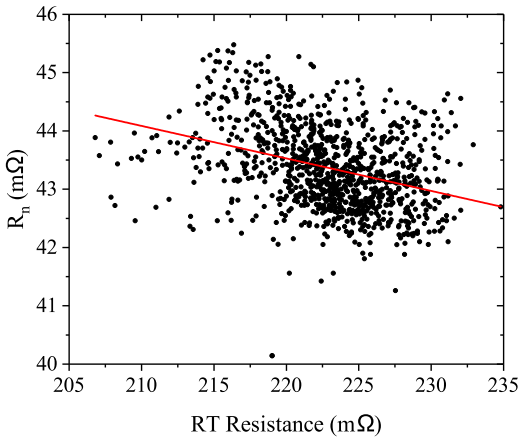

Fig. 6. Plot of the 4 K normal resistance versus RT resistance. There is a little correlation between R_n and the RT resistance. This lack of correlation is caused by random variations in process sizes resulting in different spreading resistance contributions for individual devices.

in size, δ, between the junction (or via) and the electrodes with a change in this parameter of ≈50 nm causing a 5% change in RT resistance. The fact that R_n is not as strongly correlated with the RT measurements as I_c could be due to the fact that I_c has an exponential dependence on the thickness of the barrier [19]. This means that small differences in thickness that would result in a linear change in R_n will result in an exponential change in I_c. Also, the fact that R_n is influenced by both changes in Nb concentration as well as barrier thickness further obscure the relationship with the RT measurements. This contrasts with tunnel junctions where $I_c \cdot R_n$ is expected to be constant, even with small differences in barrier thickness.

III. Conclusion

We have demonstrated an automated probing system allowing us to measure 1024 individual JJs on a 1 × 1 cm die at both RT and 4 K. This system has allowed us to directly measure I_c and R_n for a large number of junctions for the first time and analyze the statistical distributions of their low temperature properties. Additionally, we have been able to directly compare the RT and cryogenic properties of individual junctions. We find that for low barrier resistivity junctions like the ones in this study, RT measurements of resistance are dominated by the spreading resistance in the electrodes and do not give an accurate measure of low temperature electrical properties of the junctions. This study provides strong evidence that automated probing at 4 K is an invaluable PCM for Nb_xSi_{1-x}-barrier JJs, and more broadly any junction whose barriers are highly conductive.

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