Nanometre scale dimensional measurements

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We can make really small features, but how well can we measure them? In our Nature Electronics article, we review dimensional metrology methods needed for future semiconductor devices.

Our paper is available here: Metrology for the next generation of semiconductor devices[1]

As contributors to the metrology section of the International Roadmap for Devices and Systems (IRDS)[2] (formerly the International Technology Roadmap for Semiconductors – ITRS), we regularly get questions about how small or fast we think semiconductor chips will get. Over the years we've observed that most non-specialists understand the role decreasing device sizes (scaling) has played in microelectronics. Many know that these devices will soon reach some fundamental size limits, but the topic of what techniques are required to actually determine these sizes rarely comes up. This is the same for people with or without science and engineering backgrounds.

In a relatively short period, the mainstream device architecture (CMOS) has moved from a planar orientation to one that is not only three dimensional in function (with a host of new important parameters), but also contains more types of materials than ever before. The 2017 IRDS specifies a gate length of 6 nm for the years 2027 to 2033. In contrast, the smallest feature size specified by the 1994 roadmap was 0.35 μm, more than 50 times larger than that of 2018. The features are small enough that the level of manufacturing control needed is now at a point where random variation in the position and location of molecules can affect device performance, and in some cases are below the measurement capability of most instruments. To make matters more interesting (or complicated depending on one's view), a wide range of possible replacement candidates for CMOS have been proposed. Some of the proposed devices have materials with similar properties to each other (making them difficult to distinguish) and complex shapes that would be difficult to measure. In addition, the various lithography options such as directed self-assembly, nanoimprint, and extreme ultraviolet, among others, all have metrology pros and cons. With various possibilities developing so quickly, even people already familiar with semiconductor metrology could get confused about the measurement options available. During an IRDS meeting earlier this year, we decided it was time to write this review.

In the paper, we focus mostly on dimensional metrology because it directly addresses size. What techniques are available to measure a 5 nm line, what are their advantages and limits, what is the underlying physics, what is the resolution, what improvements are needed, and what are the latest developments? But, of course, material properties play a key role in an instrument's ability to determine size, and more so at nanoscale dimensions. We focus the discussion on the main techniques used for integrated circuit dimensional metrology: scanning electron microscopy, atomic force microscopy, scatterometry, and transmission electron microscopy. We also cover critical dimension small angle X-ray scattering, which is rarely used in the fab but is an area of intense research because of its small X-ray wavelength. One question we try to answer is how new device designs affect metrology requirements.

Figure 1 shows a diagram of a stacked chip being measured by different techniques[1, 3-7]. The measurement needs of such a chip (individual layers or as a whole) are quite complex: dozens of materials with differing interaction physics with the metrology method, features with complex geometries and at different levels, small target volumes (leading to quantum confinement), interfacial roughness, optically opaque layers, and so on. The requirements are stringent and varied enough that no single technique has the needed resolution, speed, and low

levels of uncertainty required to make the measurements--and in some cases no known measurement method exists. Multiple techniques, individually or combined statistically through hybrid metrology[8], are needed to make these critical measurements.

We hope our review will help stimulate discussions that could lead to new measurement approaches. So please, next time ask about the underlying measurement methods; they may not be optimum or even exist, but the question would make for a livelier discussion.

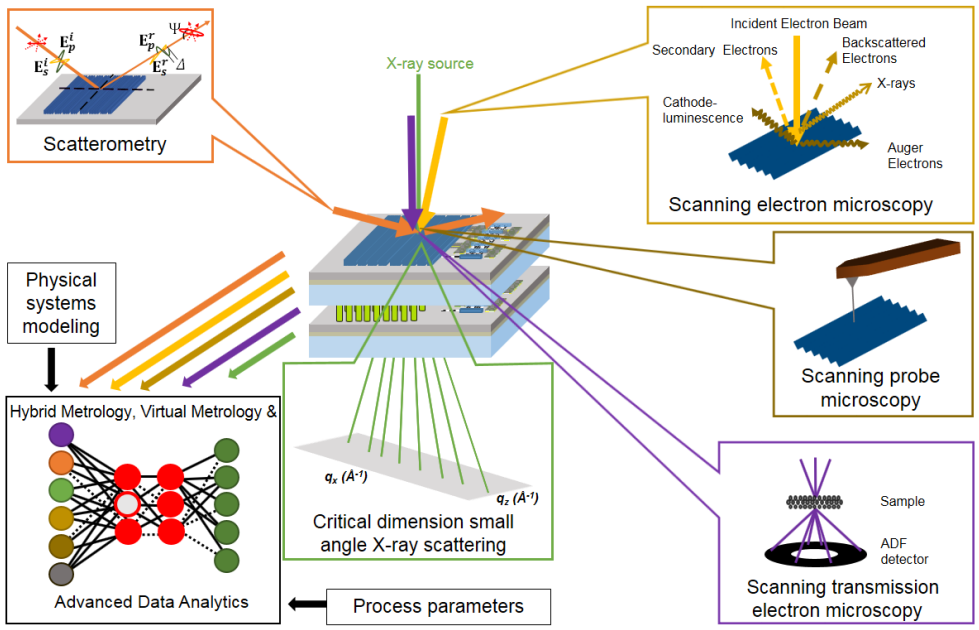

Figure 1: Multi-Instrument evaluation of next generation chips

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