# Current quantization due to single-electron transfer in Si-wire charge-coupled devices

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We observe a quantized current due to single-electron transfer in a small charge-coupled device, which consists of a narrow Si-wire channel with fine gates; the gate is used to form a tunable barrier potential. By modulating two barrier potentials under the fine gates with phase-shifted pulse voltages, quantized numbers of electrons are injected into and extracted from the charge island sandwiched by the two barriers. Current plateaus due to single-electron transfer are clearly observed at 20 K with frequencies up to 100 MHz and a current level of 16 pA. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1650036]

One by one transfer of charge carriers has been of much interest for a variety of possible applications including integrated single-electron (SE) circuits, current standards in metrology, and single-photon sources. SE pumps[1] and turnstiles[2] were proposed and experimentally demonstrated by using multiple metal islands separated by metal–oxide tunnel junctions. They can give a quantized current equal to $ef$, where $f$ is the frequency with which electrons are clocked through the devices. Although accurate transfer with error of $10^{-8}$ was performed by using a seven-tunnel junction pump,[3] the operation frequency was limited to the order of MHz due to the resistance of the tunnel junctions.

From a practical viewpoint, semiconductor-based devices are important because of their higher operating temperature and larger potential for circuit application. It is also a merit that one can modulate tunnel barriers electrically. Although the operation frequencies were still limited to the order of MHz, there have been reports on the use of modulated tunnel barriers; in a AlGaAs/GaAs-based SE transistor, temporal modulation of two tunnel barriers was used to enable SE transfer.[4,5] SE pumps[6] and turnstiles[7] operating at 25 K were realized using a Si SE transistor combined with two metal–oxide–semiconductor field-effect transistors (MOSFETs).

One of the most suitable structures for high-frequency SE transfer is a nanometer-scale charge-coupled device (CCD),[8] in which the electrically formed potential barrier is tunable. Back-and-forth manipulation of single holes was demonstrated using a Si-wire CCD at 25 K.[9] In this letter we report the observation of current quantization in a Si-wire CCD, which was obtained by using a simple pulse sequence to modulate two barrier potentials.

The devices are basically Si-wire MOSFETs fabricated on a silicon-on-insulator wafer. Figure 1(a) shows a schematic top view of the device. The 30 nm wide Si-wire channel and the array of fine poly-Si gates are fabricated by electron beam lithography. A double-layer gate structure is employed; the wide upper poly-Si gate (UG) is used as an implantation mask during the formation of $n$-type source and drain regions. Figure 1(b) shows a top-view scanning electron microscope image of the device before UG formation. For SE transfer, two repetitive pulse voltages ($V_{G1}$ and $V_{G2}$) are applied to the two of the fine MOS gates (G1 and G2). In this case the third fine gate (G3) is not essential for operation and its voltage ($V_{G3}$) is kept at 0.5 V. The substrate voltage ($V_{\mathrm{sub}}$) is fixed and the source is grounded. For dc drain volt-

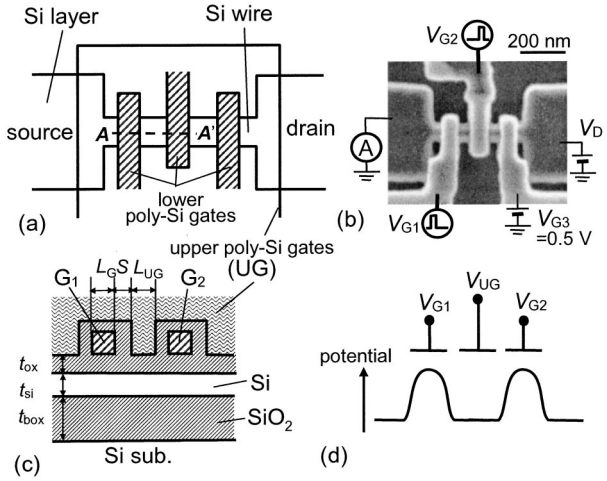


FIG. 1. (a) Schematic top view of the device. (b) Scanning electron microscope image of the device before upper gate formation. Repeated pulse voltages denoted by $V_{G1}$ and $V_{G2}$ are applied to two of the gates. (c) Schematic cross section along line $A-A'$. (d) Schematic diagram of the potential profile and gate control. The island region is mainly controlled by upper gate voltage $V_{\mathrm{UG}}$.

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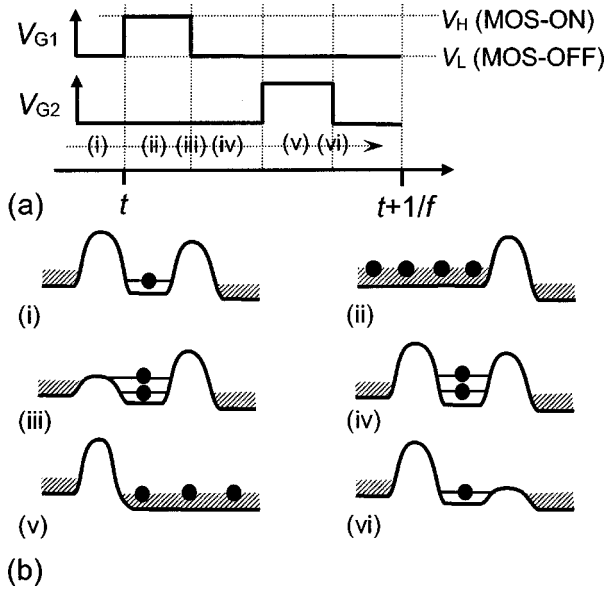


FIG. 2. (a) Pulse sequence for $V_{G1}$ and $V_{G2}$. (b) Schematic diagram of the charge transfer procedure for steps (i)–(vi).

age ($V_D$), the current between the source and the drain is measured as a dc current. Figure 1 (c) shows a cross-sectional view along the $A-A'$ line in Fig. 1(a). The thicknesses of the Si wire ($t_{\mathrm{Si}}$), the gate oxide ($t_{\mathrm{ox}}$) and the buried oxide ($t_{\mathrm{box}}$) are about 20, 30 and 400 nm, respectively. The gate length ($L_G$) and the spacer thickness ($S$) are, respectively, 40 and 30 nm. Because the UG intrudes into the gap between G1 and G2, the channel region with length $L_{\mathrm{UG}}=40$ nm, which acts as a charge island, is controlled by the upper gate voltage ($V_{\mathrm{UG}}$). If we assume that the island length is $L_{\mathrm{UG}}+S$, the total capacitance ($C_T$) is estimated to be on the order of 10 aF. A sketch of the electron potential and the gate control is shown in Fig. 1(d).

The pulse sequence for $V_{G1}$ and $V_{G2}$ is shown in Fig. 2(a). The high and low levels ($V_H$ and $V_L$) are 0 and $-1$ V, which correspond to ON and OFF states of the MOS, respectively. The threshold voltage of the MOS is between $V_H$ and $V_L$ (for example, $-0.3$ V at $V_{\mathrm{UG}}=0$ V). A quarter period pulse is applied to the two gates with a half period shift. Figure 2(b) describes how SE transfer occurs according to the procedure steps (i)–(vi). At step (i) the island is isolated from the source and the drain. At (ii) the island is connected to the source since the G1 MOS is in the ON state. When $V_{G1}$ is changed from $V_H$ to $V_L$ at (iii), a potential barrier forms to capture electrons in the island. We suggest that the single-electron tunneling box forms at a certain voltage between $V_H$ and $V_L$ where the island is coupled to the source via a tunnel barrier. It should be noted that $V_D$ barely affects the island potential in such a case because the island and the drain become disconnected by the MOS; the coupling between the island and the drain is negligibly small. Consequently, the number of captured electrons ($N_1$) is dictated by the difference in voltage between the source and the upper gate; $N_1=n$ if $n-1/2<C_{\mathrm{UG}}V_{\mathrm{UG}}/e<n+1/2$. Here, $n$ is an integer and $C_{\mathrm{UG}}$ is the capacitance between the upper gate and the island. This is strikingly different from the case of metal-based SE turnstiles, in which $V_D$ affects the island potential. In steps (v) and (vi), the island is connected to the drain. In this case, the number of electrons after these steps ($N_2$) is determined by $V_{\mathrm{UG}}$ and $V_D$ to be $N_2=m$ if $m-1/2<C_{\mathrm{UG}}(V_{\mathrm{UG}}-V_D)/e<m+1/2$, where $m$ is an integer. With one cycle of the sequence, the net number ($N$) of electrons transferred from the source to the drain amounts to $N=N_1-N_2$. Then, the current ($I$) from the drain to the source is quantized as $I=Nef$.

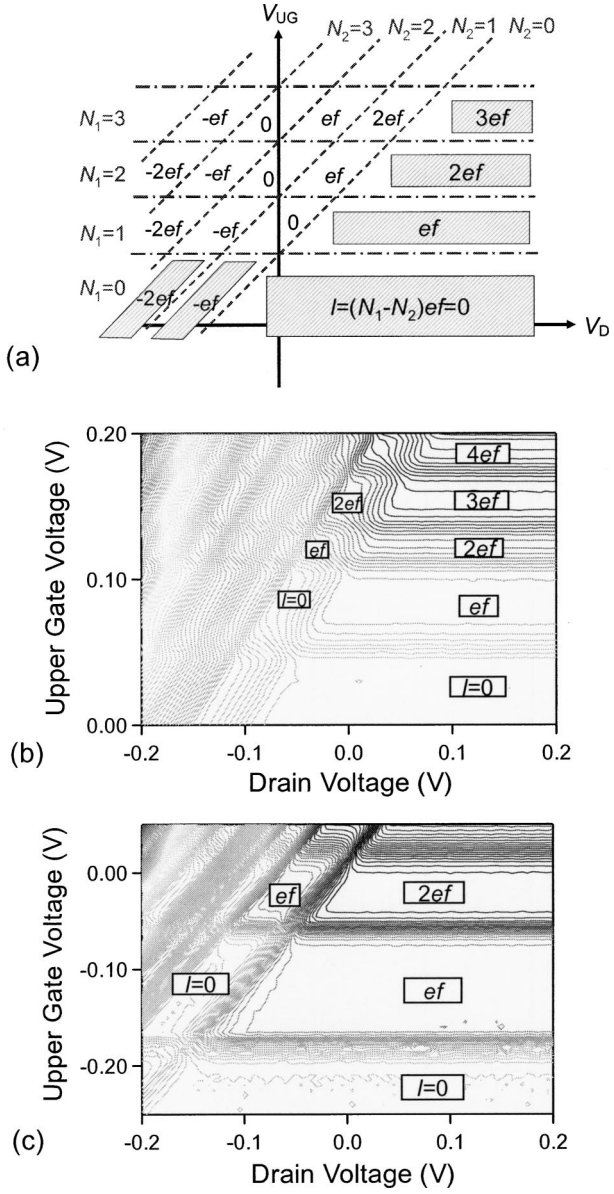


FIG. 3. (a) Stability diagram for $N_1$, $N_2$, and $I=Nef$ in the ($V_D$, $V_{\mathrm{UG}}$) plane. The dot-dashed lines depict the boundaries for $N_1$ while the dashed lines are those for $N_2$. In the hatched regions, the island is depleted during the charge transfer cycle. (b) Contour plot of $I$ vs $V_D$ and $V_{\mathrm{UG}}$ measured at 20 K ($V_{\mathrm{sub}}=2$ V, 5 MHz). Contour lines are 100 fA steps. (c) Result obtained when the pulse voltages are applied to G2 and G3 of the same device ($V_{G1}=0.5$ V, $V_{\mathrm{sub}}=4$ V, 5 MHz). Contour lines are 50 fA steps.

Figure 3(a) shows a stability diagram for $N_1$, $N_2$, and $Nef$ plotted in the ($V_D$, $V_{\mathrm{UG}}$) plane. Since $N_1$ is independent of $V_D$, the boundaries of the $N_1$ diagram are parallel to the $V_D$ axis. The boundaries for $N_2$ are parallel to the (1, 1) direction in the plane, which shows that $N_2$ is a function of $V_{\mathrm{UG}}-V_D$. Like conventional SE turnstiles[2] $I=0$ when $V_D=0$ V.

Note that there are lower bounds, that is, $N_1=0$ and $N_2=0$ because the island is made of semiconductors. $N_2$

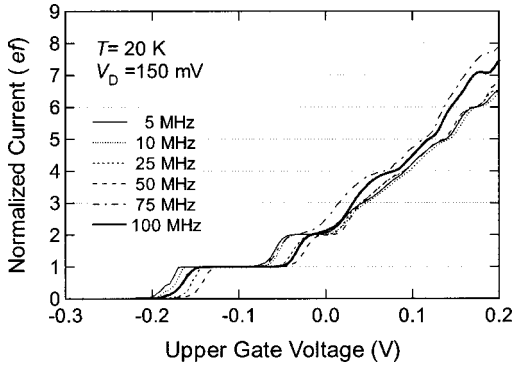


FIG. 4. Frequency dependence of the current staircases as a function of $V_{UG}$ at $V_D = 150$ mV. The data shown correspond to the result shown in Fig. 3(c).

$=0$ gives rise to a unique region at positive high $V_D$, where the current does not depend on $V_D$, but exclusively on $V_{UG}$. This is because all of the electrons captured from the source move to the drain so that the island is completely depleted. Therefore, $N$ is equal to $N_1$.

Figure 3(b) shows an experimental result of the contour plot of the current versus $V_D$ and $V_{UG}$. The measurement temperature is 20 K. The pulse frequency is 5 MHz, that is, $ef = 801$ fA. The plateaus for quantized current $Nef$ are clearly observed. Note that the observed current quantization is not related to quantized conductance due to ballistic transport. The shape of the diagram agrees well with that of the diagram in Fig. 3(a). From fitting of orthodox Coulomb-blockade theory to the results, $C_T$ and $C_{UG}$ are estimated to be 12 and 7 aF, respectively, which agrees reasonably well with the dimensions of the structure. It should be noted that the current is nonzero even at $V_D = 0$ V. This can be attributed to the effect of cross capacitance between G1 (G2) and the island because the gate oxide is not very thin. For example, when G2 MOS is off, the island is coupled to G2 by a few tens of a percent of the total coupling. This can shift the stability boundaries for $N_1$ in Fig. 3(a). Since the cross-capacitance effect differs for $N_1$ and $N_2$ due to the structural difference between G1 and G2, nonzero current could be obtained at $V_D = 0$ V. Figure 3(c) shows other data obtained for the same device when we used G2 and G3. Enlarged clearer plateaus are observed especially in the few-electron regime where $C_T$ is estimated to be as small as 4 aF for $N = 1$. The reason for this is not clear, but the island between G2 and G3 might be smaller due to pattern-size fluctuation.

Figure 4 shows the frequency dependence of the current staircases as a function of $V_{UG}$ at $V_D = 150$ mV where the island is likely depleted. The current quantization as a function of $V_{UG}$ is clearly observed up to 100 MHz ($ef = 16$ pA). The curves depend slightly on the frequency, which might result from deformation of the pulse shape, which can affect the characteristics through the cross-capacitance effect. It is seen that the width of the plateau is largest for $N = 1$ and gets smaller as $N$ increases, which suggests that the capacitance of the island is smaller for smaller $N$. This might suggest that the wave function of a few electrons is localized in a smaller center region within the electrically formed island, thereby leading to smaller capacitance.

The proposed device has several advantages. First, the device structure and the pulse sequence are quite simple. Second, high frequency operation is expected because charge quantization will occur when the barrier resistance is significantly low as shown in step (iii) of Fig. 2(b). Future work must be done to clarify the charge-transfer error mechanism when the barrier conductance changes dynamically,[10] which would limit the maximum frequency. The error rate could not be evaluated in this experiment, but it should be less than $10^{-2}$ even at 100 MHz; it was limited by the accuracy of our current measurement system. Third, the number of electrons transferred is easily controlled by the gate voltage bias if we use the region where the island is depleted. This is unique because, for conventional metal devices, we need to adjust the trajectory for control of the two ac gate voltages[1] or change the drain voltage.[2]

In conclusion, we have demonstrated single-charge transfer in a small CCD with a narrow Si-wire channel at 20 K and frequency up to 100 MHz. The current staircases were obtained as a function of the gate voltage due to depletion of the Si island during the transfer cycle.

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