


## Low-Resistance, High-Yield Electrical Contacts to Atom Scale Si:P Devices Using Palladium Silicide

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Scanning tunneling microscopy (STM) enables the fabrication of two-dimensional  $\delta$ -doped structures in Si with atomistic precision, with applications from tunnel field-effect transistors to qubits. The combination of a very small contact area and the restrictive thermal budget necessary to maintain the integrity of the  $\delta$  layer make developing a robust electrical contact method a significant challenge to realizing the potential of atomically precise devices. We demonstrate a method for electrical contact using Pd<sub>2</sub>Si formed at the temperature of silicon overgrowth (250 °C), minimizing the diffusive impact on the  $\delta$  layer. We use the transfer length method to show our Pd<sub>2</sub>Si contacts have very high yield (99.7% +0.2% –1.5%) and low resistivity ( $272 \pm 41 \Omega \mu\text{m}$ ) in contacting mesa-etched Si:P  $\delta$  layers. We also present three terminal measurements of low contact resistance (<1 k $\Omega$ ) to devices written by STM hydrogen depassivation lithography with similarly high yield (100% +0% –3.2%).

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### I. INTRODUCTION

Fabrication of  $\delta$ -doped Si:P nanostructures with atomistic precision is the subject of intense ongoing study due to the potential to utilize this system in high-performance electronics and quantum computation [1–4]. While Si:P devices have been demonstrated in the laboratory, fabrication challenges intrinsic to this material make it difficult to produce the yield necessary to truly exploit the system. For instance, atomically precise devices present both an extremely small contact area (approximately equal to 1 nm thick) and an extremely restrictive thermal budget (ideally  $\leq 250$  °C) to minimize dopant diffusion and retain the precision nature of the device. In Si:P quantum devices, even dopant diffusion at the atomic scale can substantially alter device operation and performance [5]. The atomically thin structure of Si:P differentiates this material from traditional doped Si, introducing contact challenges similar to those in other two-dimensional (2D) systems [6]. Additionally, the Si:P device layer is buried beneath 30 nm of undoped Si, further complicating contact strategies. These issues underlie the prominent challenge in forming low-resistance, Ohmic contacts with high yield, and require a reexamination of contact technology.

Several electrical contact techniques are currently in use. An Al “spiking” approach, in which metal pads

are deposited and annealed at approximately 350 °C [4], produces a random distribution of Al spikes between the Si/Al interface and the  $\delta$ -doped structure. This process can be unreliable for micrometer-scale contact pads: no spikes may form or the penetration depth may be too shallow. To overcome the randomness of Al spiking, lithographically defined vias can be filled with Al metal [7], forming edge contacts to the  $\delta$  layer. Using vias to form reliable contacts requires a clean interface at the approximately 1-nm-thick  $\delta$ -layer edge, while also finely tuning the etch process to ensure a bowl-shaped geometry to maximize contact area. These considerations lead to a precariously narrow process window for via-etched contacts. In one case, vias are reported to provide contact resistances <100 k $\Omega$ . [8] Another approach is the formation of preimplanted contacts, which are then relocated *in situ* so that device contacts are written to overlap with the preimplanted surface [9,10]. While this approach has met with success, it restricts the thermal budget for UHV processing and gives a high parasitic resistance compared to metal contacts of the same dimensions. Preimplanted contact resistances have been reported ranging as high as 48 k $\Omega$  [9] with the lowest published contact resistivity being approximately 1 k $\Omega \mu\text{m}$ , a value approximated from a two-point resistance measurement. [10] The Pd<sub>2</sub>Si contacts reported here offer an order of magnitude improvement over typical contact resistances and a substantial improvement in contact variability.

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We address these challenges by utilizing palladium silicide ( $\text{Pd}_2\text{Si}$ ) to contact  $\delta$ -doped Si:P devices.  $\text{Pd}_2\text{Si}$  is a low-temperature metallic silicide with a hexagonal structure. As shown in Fig. 1(a), the Si:P device is buried beneath a Si encapsulation layer. In our process, palladium is deposited in the contact region and annealed at 250 °C for 20 min. During annealing, the Si and metal interdiffuse, consuming Si, displacing P into the substrate [11], and adjoining the Si:P device and  $\text{Pd}_2\text{Si}$  contact.  $\text{Pd}_2\text{Si}$  contacts form without etching, enabling a clean interface to the Si:P layer. Furthermore, the process is deterministic, with subsurface metal diffusion occurring uniformly across each lithographically defined contact. Thus,  $\text{Pd}_2\text{Si}$  contacts combine the advantages of the common Al contacting methods discussed above while avoiding their disadvantages.

Low-temperature silicide [see Fig. 1(b)] contacts to conventional semiconductor devices are common practice [12], but their use for contacting 2D Si:P  $\delta$ -doped devices has been limited. Polley *et al.* demonstrated NiSi contacts [13,14] to eliminate complications from the superconducting transition that occurs in Al near 1.2 K. In that work, to avoid the resistive  $\text{Ni}_2\text{Si}$  phase, samples were annealed at 400 °C, and additional etch steps were performed to remove unreacted, magnetic Ni atoms, which can induce hysteretic effects in the magnetotransport. As mentioned above, our use of  $\text{Pd}_2\text{Si}$  allows contacts to form at much

lower temperatures and avoids magnetic materials while maintaining a straightforward process.

Finally, our choice of  $\text{Pd}_2\text{Si}$  is advantageous due to reaction kinetics. First, the choice of dimetal silicides ( $M_2\text{Si}$ ) is often preferable, since the metal atom tends to be the dominant diffusive species (DDS), whereas Si tends to be the DDS in monosilicides ( $M\text{Si}$ ) [15]. When the metal is the DDS, formation of voids at the silicon–silicide interface is minimized and contaminants are left at the metal–silicide interface, forming a pristine interface layer abutting the Si:P layer. In contrast, when the DDS is Si, Kirkendall voids can form at the silicon–silicide interface [16]. Platinum silicide, a metallurgically similar candidate silicide of broad interest [17,18], forms both dimetal and monosilicide phases at low temperature [19]. In contrast, the large difference between the formation temperatures of  $\text{Pd}_2\text{Si}$  (250 °C) and PdSi (820 °C) [20,21] ensures a well-controlled reaction where Pd will remain the DDS. Second, Pd can diffuse through a  $\text{SiO}_2$  film more easily than Pt or Ni, meaning a thin native oxide poses less of a barrier to silicide formation [22].

$\text{Pd}_2\text{Si}$  offers the lowest formation temperature of all candidate silicides [Fig. 1(c)] [14,23], reported to be from 100 °C [24,25] to 190 °C [23]. Additionally,  $\text{Pd}_2\text{Si}$  exhibits a very weak electron-phonon interaction, suggesting that any superconductivity could be easily suppressed [26]. Finally, both  $\text{Pd}_2\text{Si}$  and residual Pd metal are nonmagnetic, minimizing the influence of stray magnetic moments and eliminating the need to remove residual metal.

## II. EXPERIMENTAL PROCEDURES

$\delta$ -doped Si:P devices are fabricated by gas-phase  $\text{PH}_3$  dosing of the Si(100) surface, which has been prepatterned with etched alignment marks [27]. The  $2 \times 1$  surface reconstruction is prepared by flashing to 1200 °C, cooling rapidly to 800 °C, and then cooling slowly (2.5 °C/s) to 350 °C. The surface is optionally passivated by atomic H cracked on a 1300 °C W filament (10 min) before cooling slowly to room temperature. For passivated surfaces, the device geometry is defined by hydrogen depassivation lithography [28,29] in the scanning tunneling microscope (STM) [30]. STM is performed in an Omicron variable temperature STM with polycrystalline W tips prepared by electrochemical etching and optionally sputter sharpened [31]. The tip is biased relative to a grounded sample. For unpassivated surfaces, approximately 30 mm<sup>2</sup>, uniform  $\delta$ -doped Si:P films (“blanket  $\delta$  layers”) are produced and later patterned by optical or *e*-beam lithography and etching after Si encapsulation. For H passivated surfaces, the H serves as a chemical resist, which is locally desorbed to expose Si dangling bonds; only the patterned area is converted to  $\delta$ -doped Si:P. The surface is exposed to  $\text{PH}_3$  gas at  $4 \times 10^{-6}$  Pa for 6 min, saturating unpassivated portions of the surface.

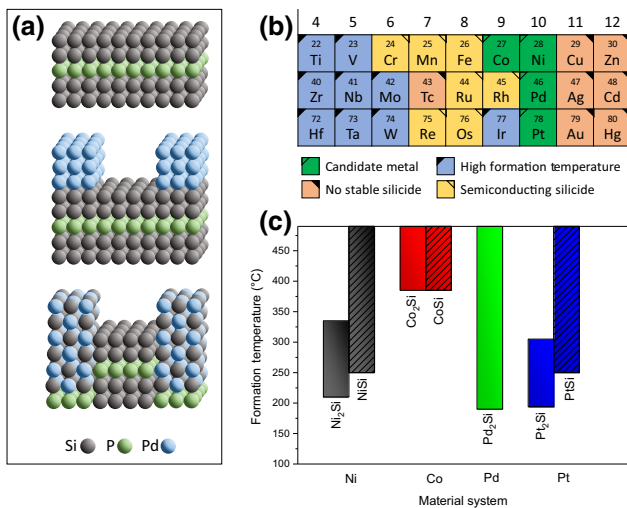


FIG. 1. Silicide contact process and selection of transition metal. (a) Si:P device is buried beneath 30 nm of epitaxial Si. Pd metal pads are deposited in contact region and Si and Pd interdiffuse to form  $\text{Pd}_2\text{Si}$ , consuming Si and interfacing with the Si:P device. (b) Candidate metals for silicide formation (green) are identified, excluding elements that do not form stable silicides (orange), that form semiconducting silicides (yellow), and that form silicides at temperatures  $> 500$  °C (blue). (c) Four candidate silicides are compared by the phases in which they exist and the temperature ranges in which these phases form. Dimetal silicide phases are shown in solid color. Monosilicides are shown with cross hatching.

P adatoms are incorporated by annealing [32]. A 30-nm Si encapsulation layer is deposited using a Si sublimation (SUSI) source at a rate of 0.6 monolayers/min [33–36]. During encapsulation, the P device is enclosed beneath this Si layer, which allows the sample to be removed from vacuum without contaminating the active area or degrading the quality of the device. Because of this, the STM-patterned devices are compatible with conventional cleanroom processing, as well as *ex situ* analysis and measurement techniques. For STM-patterned devices, patterns are relocated to within 200 nm with Kelvin probe force microscopy (KPFM) [37,38].

Contact pads are defined by a lift-off process and *e*-beam evaporation of 100-nm Pd metal at a base pressure of  $\leq 4 \times 10^{-4}$  Pa and deposition rate of 0.2 nm/s. Native SiO<sub>2</sub> is removed by immersion in 100:1 buffered HF for 1 min immediately before evaporation. Pd<sub>2</sub>Si is formed by thermal annealing to 250 °C for 20 min with a base pressure below 0.67 Pa and back filled with Ar to atmospheric pressure with the sample held on a SiC susceptor and temperature monitored by both a pyrometer and thermocouple. The temperature setpoint is achieved in a single step with a ramp rate of 250 °C/min. Ramp time is in addition to the specified annealing time. No process for residual Pd removal is performed.

During the process development, Pd and Pd<sub>2</sub>Si are characterized by x-ray diffraction (XRD), transmission electron microscopy (TEM), and energy dispersive x-ray spectroscopy (EDS). Electrical measurements are performed in a closed-cycle cryostat with a base temperature of 3.1 K. All measurements are performed in independent systems, with removal from UHV occurring only after deposition of the Si encapsulation layer.

### III. RESULTS AND DISCUSSION

To accommodate approximately  $1\sigma$  variations in Si encapsulation layer thickness ( $\pm 2$  nm), Pd thickness ( $\pm 10$  nm), and Pd<sub>2</sub>Si/Si interface roughness (approximately equal to 10 nm), we target a Pd metal thickness of 100 nm for a nominal junction depth of 70 nm [39].

We explore the progression of silicide formation by XRD of annealed metal films deposited on chemically passivated Si(100). Spectral peaks are identified in an annealed Pd<sub>2</sub>Si film, which exhibits both Pd and Pd<sub>2</sub>Si peaks [Fig. 2(a)]; 120 nm of Pd is annealed for 20 min, the conditions for which Pd is partially but not fully converted to Pd<sub>2</sub>Si. The peak positions for Pd, Pd<sub>2</sub>Si, and Si are indicated above the spectrum together with peaks arising from the sample stage of our XRD system. Unlabeled peaks between 60° and 67° are derived from the Si(400) peak and result from nonmonochromaticity of the x-ray beam. Spectral features are identified as the Pd(111) and Pd(200) planes and the Pd<sub>2</sub>Si(002) plane. There is no overlap in the spectral fingerprint of these materials as the

commercial Si(100) wafer is single crystal. The Pd film is predominantly (111) textured and Pd<sub>2</sub>Si is (001) textured. The large spectral width of the Pd<sub>2</sub>Si peak suggests that the film is polycrystalline and has a crystallite size of approximately 5 nm for annealing times  $\leq 20$  min, a result consistent with earlier studies [40]. To follow the progression of silicide formation, separate and independent samples are annealed at 250 °C for intervals from 0 to 60 min [Fig. 2(b)]. We focus on the spectral region from 35° to 60° and observe the progression from Pd to Pd<sub>2</sub>Si. To elucidate this progression, spectra are normalized so that the sum of the Pd(111) and Pd<sub>2</sub>Si(002) peak intensities is a constant. The absence of the Pd(111) peak after annealing indicates that all Pd metal is converted after 60 min. After annealing 60 min, the measured crystallite size increases to approximately 8 nm.

We expect that texturing of the Pd<sub>2</sub>Si film is less critical when contacting the 2D  $\delta$ -doped Si:P layer because contact is made along the edge of the silicide, unlike conventional semiconductor devices where the contact area can extend deeply beneath the pad. Regardless of film texture, rotational misalignment between grains will result in a varying interface between Si:P and Pd<sub>2</sub>Si. Although this electronic interface is of potential future interest, only an epitaxial silicide would allow for it to be explored in detail.

To further study contact structure and composition, Pd<sub>2</sub>Si contacts to Si:P  $\delta$  layers are extracted by focused ion-beam (FIB) milling and characterized by TEM and EDS. In the TEM micrograph [Fig. 2(c)], we observe penetration of Pd<sub>2</sub>Si into the substrate to a depth approximately equal to 48 nm, crossing the Si:P  $\delta$  layer (the position of the  $\delta$  layer is indicated by a dashed red line). This Pd<sub>2</sub>Si penetration depth is reduced from its  $>60$ -nm bulk value at the edge of the contact pad due to a local reduction in Pd metal thickness. This is primarily a result of shadowing by resist during Pd deposition and possibly some lateral encroachment of Pd during annealing. The silicide is polycrystalline with a grain size of approximately 20 nm near the contact. The high resolution of TEM micrographs also results in limited sample size; the crystallite size determined by XRD measurements provides better statistical reliability regarding average grain size when compared to TEM. Furthermore, grain sizes near the contact area may be larger than in the bulk due to the reduced film thickness in that region, which causes silicide formation to occur more rapidly.

From a one-dimensional EDS line scan across the silicide [position indicated by a solid green line and data plotted in Fig. 2(d)], we confirm that the contact is composed of Pd<sub>2</sub>Si, with uniform composition throughout the bulk of the film. A Pd-rich (Pd<sub>*x*</sub>Si,  $x \approx 4$ ) surface layer approximately 20 nm in thickness is observed, which indicates incomplete silicide formation at the surface. Conductivity in the Pd<sub>2</sub>Si film is assessed with a silicide Hall bar, from

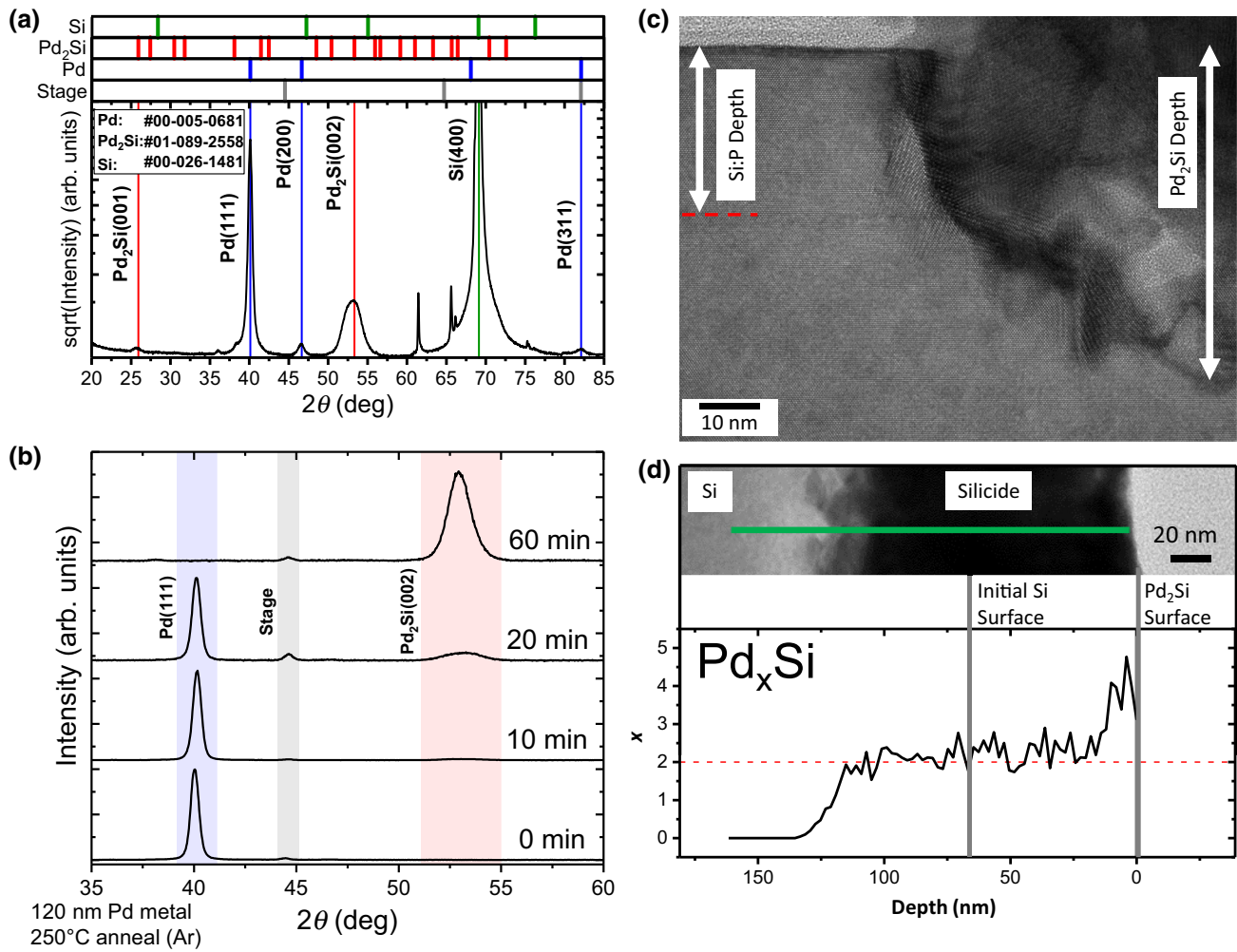


FIG. 2. Analysis of the structure and formation of  $\text{Pd}_2\text{Si}$ . (a) XRD spectrum of Pd film on Si(100) after partial annealing at  $250^\circ\text{C}$ . Anticipated derived characteristic peaks corresponding to the Pd(111) and Si(400) peaks are indicated with arrows. (b) Progression of normalized spectra for different annealing times. The Pd(111) peak vanishes and is replaced by the  $\text{Pd}_2\text{Si}$ (002) peak when annealed. (c) TEM micrograph of annealed  $\text{Pd}_2\text{Si}$  contact to a Si:P  $\delta$  layer (location of  $\delta$  layer is indicated with a red dashed line). (d) EDS mapping across a  $\text{Pd}_2\text{Si}$  contact pad at position indicated by a solid green line. The composition ( $\text{Pd}_2\text{Si}$ ) is uniform with the exception of a 20-nm Pd-rich (approximately equivalent to  $\text{Pd}_4\text{Si}$ ) surface layer. The position of the original Si surface is estimated [32].

which a resistivity of  $80\ \mu\Omega\text{ cm}$  at approximately 3 K is measured, assuming the nominal depth discussed above.

To assess yield and variations in contact resistance, electrical tests are performed on blanket  $\delta$ -layer devices, avoiding the inherently serial process of STM lithography for which write times can be several hours depending on the device size and required precision [41].

The Si:P  $\delta$  layer is patterned into a Hall bar from which sheet resistance ( $1.3\ \text{k}\Omega$ ), carrier density ( $1.1 \times 10^{14}\ \text{cm}^{-2}$ ), and mobility ( $42\ \text{cm}^2/\text{V s}$ ) are extracted. These properties are a function of the specific process utilized here and can be controlled by varying process conditions. We also pattern a series of five transfer length measurement (TLM) devices of different widths ( $50\ \text{nm} \leq W \leq 5\ \mu\text{m}$ ) from which contact resistance and

sheet resistance are extracted. Within each TLM, channel length ( $L$ ) is varied from 350 nm to  $5\ \mu\text{m}$ . For each device, we measure the relationship between  $L$  and the two-point resistance between consecutive contacts ( $R_T$ ). In this structure,  $R_T$  is related to contact resistance ( $R_C$ ) and sheet resistance ( $R_S$ ) by

$$R_T = \frac{R_S}{W}L + 2R_C. \quad (1)$$

For each device, a linear fit is performed and the contact resistance is extracted from the extrapolated  $y$  intercept. Sheet resistance is extracted from the slope of the linear fit. Two outlying points are excluded from fitting: ( $W = 200\ \text{nm}$ ,  $L = 350\ \text{nm}$ ) and ( $W = 50\ \text{nm}$ ,  $L = 5\ \mu\text{m}$ ) [42]. Contact resistances and sheet resistances are shown

TABLE I. Contact resistances extracted from TLM devices and used in the generation of Figs. 3(a) and 3(b). Uncertainties correspond to a  $1\sigma$  fit uncertainty.

$W$ (nm)	$R_C$ ( $\Omega$ )	$R_S$ ( $\Omega$ )
50	$3207 \pm 550$	$1318 \pm 44$
200	$531 \pm 136$	$1307 \pm 22$
500	$445 \pm 12$	$1305 \pm 5$
2000	$157 \pm 13$	$1357 \pm 20$
5000	$107 \pm 22$	$1376 \pm 5$

in Table I. In Fig. 3(a), we plot  $W \times (R_T - 2R_C)$  for each device, where  $R_C$  is extracted from the linear fit. The collapse of all datasets to a single line indicates quality of fit, uniformity of sheet resistance, and appropriate extraction of contact resistance. A representative device geometry is shown in the inset.

In Fig. 3(b), we plot contact conductance (solid black squares) and sheet resistance (open red circles) as a function of  $W$ . Sheet resistance extracted from the 10- $\mu\text{m}$ -wide Hall bar is indicated by a red line for comparison. There exists strong agreement between sheet resistances extracted from these two techniques, with deviations occurring only for small values of  $W$  ( $<500$  nm). This deviation likely results from edge effects arising as the width of the mesa-etched wire becomes small, but we cannot rule out local variations in carrier density or mobility within the  $\delta$  layer at these scales. Measured contact conductance is represented by a weighted linear fit (solid black line) with  $1/\sigma^2$  weighting and 95% pointwise confidence bands (gray) corresponding to a contact resistivity of  $\rho_C = 272 \pm 41 \Omega \mu\text{m}$  ( $R^2 = 0.94$ ). Here, the uncertainty reflects a  $1\sigma$  statistical fit uncertainty. We note that contact conductance appears to depart from linearity for large values of  $W$ , but this deviation corresponds to a single data point ( $W = 5 \mu\text{m}$ ) with relatively large uncertainty. As typical devices include contact lengths of  $<2 \mu\text{m}$ , the technologically relevant regime is low  $W$ , where linearity is observed and the confidence band is tight.

Through the fabrication of numerous devices for a range of experimental purposes, 313  $\text{Pd}_2\text{Si}$  contacts are formed to blanket  $\delta$ -layer devices and 312 of these contacts are Ohmic and exhibited contact resistances  $\leq 1$  k $\Omega$ . Unlike TLM devices, many of these contact resistances are deduced from simple two-terminal measurements, and therefore, represent upper bounds on contact resistance. This corresponds to a yield of  $99.7\% +0.2\% -1.5\%$  with a 95% Wilson confidence interval [43] for blanket  $\delta$ -layer device contacts. The minimum carrier density for tested devices is  $8 \times 10^{12} \text{ cm}^{-2}$ , which is achieved by reducing the dose of  $\text{PH}_3$  gas during fabrication. All contacts are functional at this carrier density.

These results clearly demonstrate that  $\text{Pd}_2\text{Si}$  contacts to Si:P films are of low resistance and high yield. While this

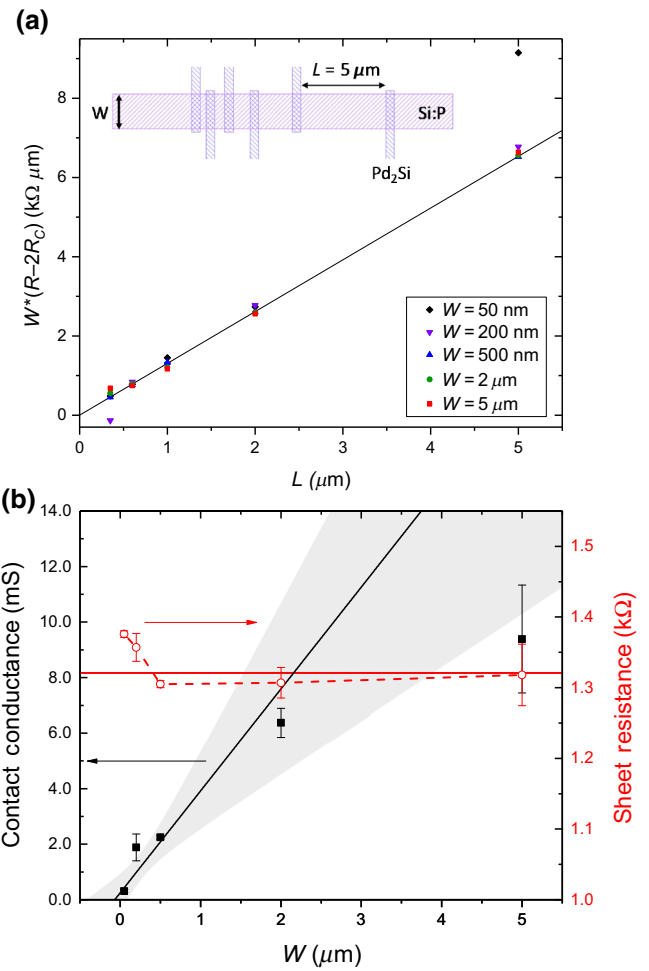


FIG. 3. TLM devices in Si:P blanket  $\delta$  layers. (a) Device measurements in five devices with varying contact dimensions ( $W$ ). Contact resistance and sheet resistance are extracted from linear fits (shown in Table I) and  $W \times (R - 2R_C)$  is plotted vs  $L$ . All data collapse to a single line, shown as a guide to the eye. The geometry of the device is shown in inset. (b) Contact conductance and sheet resistance as a function of  $W$ . Sheet resistance is shown relative to value extracted from nearby Hall bar (solid red line). Contact resistivity is estimated from a weighted linear fit to contact conductance, indicated by a solid black line. 95% confidence bands for the linear fit are shown in gray. Uncertainty in the data points corresponds to a  $1\sigma$  fit uncertainty only.

blanket  $\delta$ -layer system provides a close approximation of the STM-patterned materials, which will ultimately form the basis of Si:P devices, we must demonstrate that the process is easily transferable to STM-patterned devices. One important difference between the two systems is the presence of a mesa edge in blanket  $\delta$ -layer devices over which contact metal extends. STM-patterned devices eliminate this edge, thus eliminating any possibility that edge contacts might be formed.

We demonstrate Ohmic and low-resistance contacts to a STM-patterned  $5 \times 5 \mu\text{m}^2$  van der Pauw (VdP) structure, an easily fabricated test structure used for process

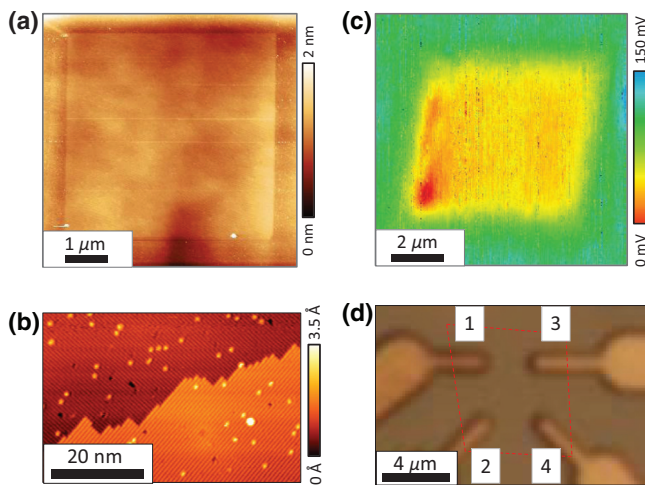


FIG. 4. Contacts to STM-patterned device. (a) STM topograph of device prior to  $\text{PH}_3$  dosing. (b) STM topograph of  $\text{Si}(100) 2 \times 1:\text{H}$  surface prior to lithographic patterning. Bright spots correspond to isolated Si dangling bonds. Isolated bonds will not facilitate spurious P atom incorporation. (c) KPFM image of surface potential after overgrowth, indicating location of device and allowing alignment of contact pads relative to etched alignment marks. (d) Optical image of device after fabrication of contacts. Device location is indicated by dashed red box. Contacts are identified by number.

development and characterization. Figure 4(a) shows a STM topographic image ( $-3$  V,  $200$  pA) of the device prior to  $\text{PH}_3$  dosing. The darker regions surrounding the box correspond to the  $\text{Si}(100) 2 \times 1:\text{H}$  surface. The bright box in the center of the image corresponds to chemically reactive Si dangling bonds, which are exposed by electron-stimulated desorption of a H passivation layer in the STM. Figure 4(b) shows an atomic-scale STM topographic image ( $-3$  V,  $200$  pA) of the same area prior to H depassivation lithography. A typical  $\text{Si}(100) 2 \times 1:\text{H}$  surface is seen with dimer row resolution and terracing. Bright spots represent single Si dangling bonds; note that a single dangling bond is not sufficient to induce the incorporation of a spurious P atom; a cluster of approximately six dangling bonds is necessary for this to occur [2]. Lithography is performed with a tip bias of  $-10$  V, tunneling current of  $200$  nA, and dose of  $10 \mu\text{C}/\mu\text{m}^2$ . After Si overgrowth to a nominal depth of  $30$  nm, the device is relocated by KPFM [Fig. 4(b)] relative to etched alignment marks. Contact pads are defined by  $e$ -beam lithography, shown in Fig. 4(c) with a red dashed line approximating the outline of the device, which is not visible by optical microscopy. From the VdP device, a carrier density of  $8.0 \times 10^{13} \text{ cm}^{-2}$  and mobility of  $44 \text{ cm}^2/\text{V s}$  are measured.

The VdP device is utilized as a Kelvin contact-resistance test structure to estimate contact resistance [44]. Although the VdP geometry is not ideally suited for this

measurement, upper bounds for contact resistance can be extracted. The resulting contact resistances are  $\leq 775 \Omega$  (contact 1),  $\leq 952 \Omega$  (contact 2),  $\leq 709 \Omega$  (contact 3), and  $\leq 729 \Omega$  (contact 4). The actual contact resistances are likely lower than these conservative estimates. Contact resistances in this device may be higher than in the blanket  $\delta$  layer due to lower carrier density in this STM-patterned VdP device (27% lower compared to blanket  $\delta$ -layer devices). In total, 117  $\text{Pd}_2\text{Si}$  contacts to functional STM-patterned devices are tested, all of which are found to provide Ohmic electrical contact with estimated contact resistances  $< 1 \text{ k}\Omega$ . Nonfunctional devices are excluded from consideration, but only if they could be independently verified to be defective for reasons unrelated to contacts using TEM, atomic force microscopy, or optical microscopy. From these measurements, the contact yield for STM-patterned devices is  $100\% +0\% -3.2\%$  with a 95% Wilson confidence interval [43].

#### IV. CONCLUSIONS

In this work, we demonstrate an alternative contact scheme for  $\delta$ -doped Si:P quantum devices using  $\text{Pd}_2\text{Si}$  with noteworthy resistivity and yield. The simplicity of this approach makes it readily applicable to Si:P device technologies. The low contact resistivity exhibited by  $\text{Pd}_2\text{Si}$  will allow for reduced write times and overhead associated with STM-defined contact pads. The high yield will enable reliable contacts to complex device architectures such as multiple-qubit systems.

$\text{Pd}_2\text{Si}$  contacts are stoichiometrically uniform, conductive at low temperature ( $80 \mu\Omega \text{ cm}$  at approximately  $3 \text{ K}$ ), and compatible with devices formed either by etching blanket  $\delta$  layers or by STM-based patterning of  $\text{Si}(100) 2 \times 1:\text{H}$ . Moreover,  $\text{Pd}_2\text{Si}$  contacts are compatible with a range of device layer carrier densities ranging from  $8.0 \times 10^{12} \text{ cm}^{-2}$  to  $1.1 \times 10^{14} \text{ cm}^{-2}$ . As Si:P carrier densities fall, the width of the Schottky barrier increases, moving contacts out of the tunneling regime. The larger the range of carrier densities for which Ohmic contact can be made, the greater the scope of devices and physics that can be investigated. Further study is required to explore the limits of  $\text{Pd}_2\text{Si}$  contacts to lightly doped Si:P films, but it is noteworthy that the reduction in carrier density seen here does not substantially increase contact resistance.

The resulting contact resistivity is low:  $272 \pm 41 \Omega \mu\text{m}$  for blanket  $\delta$  layers with carrier densities of  $1.1 \times 10^{14} \text{ cm}^{-2}$ . These results indicate that a  $1\text{-k}\Omega$  contact resistance is achievable for  $300\text{-nm}$  contacts, a size consistent with typical Si:P contact geometries. For STM-patterned devices with lower carrier densities of  $8.0 \times 10^{13} \text{ cm}^{-2}$ , contact resistances below  $1 \text{ k}\Omega$  are measured with contact lengths of the order of  $1 \mu\text{m}$ . This low contact resistance will allow for STM-patterned contact pads to be made smaller, reducing STM write times and contact pad footprints,

allowing additional surface area to be dedicated to the active portions of devices.

In the case of Si:P blanket  $\delta$  layers, we demonstrate a yield of 99.7% +0.2% -1.5% with 95% confidence. For STM-patterned devices, we demonstrate a yield of 100% +0% -3.2% with 95% confidence. With a yield >96.8%, the expected number of functional contacts fabricated before failure is >31 for STM-patterned devices. This suggests that a five-qubit device (three contacts per qubit) could be made with yield >60% due to contacts alone. As all STM-fabricated device contacts in this work are functional, this yield estimate may rise with additional testing.

In addition to implications in the field of Si:P quantum device fabrication, it is expected that Pd<sub>2</sub>Si contacts will offer enduring advantages as the development of  $\delta$ -doped materials continues beyond Si:P. While Si:P provides a well-understood material testbed for contact development, this work additionally suggests the potential for silicide contacts to other material systems, including  $\delta$ -doped Si:B or Si:Al [45], for which fabrication technologies remain in developmental stages. Achieving reliable electrical contacts for these systems could accelerate development of this burgeoning class of bipolar quantum materials.

The fabrication technology presented here enables the formation of reliable, low-resistance electrical contacts to buried Si:P quantum devices for a wide range of carrier densities. Pd<sub>2</sub>Si contact technology consistently provides Ohmic contacts with high yield, reducing one persistent barrier to the advancement of Si quantum device fabrication to a technologically relevant scale.

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