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Results and model for single-gate ratchet charge pumping

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ABSTRACT

We show experimentally that, in the same Si devices, we can demonstrate multiple two-gate pumping modes but not single-gate mode. We contrast this with GaAs devices, which do show single-gate pumping at a high yield. We propose four mechanisms to explain the lack of plateaus in the Si devices in single-gate ratchet mode: operating the dot with a large number of electrons, a large ratio between the change in electrochemical potential energy and the change in the energy of the barrier (plunger-to-barrier ratio, Δ_{ptb}) compared to the charging energy (Δ_{ptb}/E_C), nonlinear tunnel barriers, and phase offset leading to nonequilibrium heating. Our analysis shows that each of these could contribute to the lack of plateaus in single-gate ratchet pumping on Si devices but allow two-gate pumping methods to work with robust plateaus. It is easier for GaAs pumps to avoid these failure mechanisms due to their different architectures and cleaner gate turnoff curves. We propose several methods to reduce these sources of error, including reducing cross capacitances between gates. These recommendations may prove useful to other researchers in producing more robust, higher yield single-gate ratchet pumps.

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I. INTRODUCTION

Transferring single electrons accurately is a key technology in developing image sensors with single photon sensitivity,[1] quantum information with quantum dots,[2] low-power single electron devices,[3] and closing the metrological triangle.[4] In particular, the ability to transfer electrons one-by-one offers the possibility of providing a fundamental standard for electrical current based on the charge of the electron.[5] In pursuit of a metrological standard, some groups have achieved very high accuracy single electron transfer using charge pumps.[6–10] The ideal charge pump creates current $I = nef$, where n is an integer, e is the electron charge, and f is the frequency of an applied electrical bias. One attractive mode for operating these charge pumps is known as the "single-gate ratchet;"[11–13] this mode provides the counterintuitive ability to get a DC current in the absence of a DC voltage, similar to Brownian motors.[14] This ability results in subtle dependences of this pumping mechanism on various parameters; some of these dependences have not been previously investigated in detail.

In addition to the basic scientific interest in the single-gate ratchet charge pumping mechanism, there are also significant technological reasons for studying this mechanism. To produce an appreciable current useful for metrology, we need n to be large, f to be large, or many of these pumps to be run in parallel. Most studies have found that increasing n also increases error rates,[15] so $n = 1$ is typically used. The highest reported frequency for integer pumping reported is over 7 GHz,[16] but most high accuracy publications report frequencies between 0.5 and 1 GHz.[7–10] This leaves parallel pumps as the most feasible option, of which several small scale devices have been demonstrated.[17–20] To reach a metrologically relevant current, one would need on the order of 100 pumps operating in parallel. Industrial scale manufacturing of silicon devices, combined with studies showing that Si single electron devices can be quite stable over time and demonstrate a low charge offset drift,[21] make Silicon a desirable material for charge pumps. GaAs pumps have a high yield (over 90% of fabricated devices produce expected pumping behavior), near the requisite for a large scale current standard, but the yield on Si single electron pumps appears to be much lower than this, around 20% based on our own group's experience and conversations with other research groups.

Basic failure modes include gate leakage, mistargeted gate capacitance, and unintentional quantum dots that can form under gates or within the channel.

Why this yield is so low remains a pressing question. Basic considerations, such as increasing charging energy and operating the device at proper biases, are well known.[22] Some design criteria have been presented, such as the plunger-to-barrier ratio Δ_{ptb}[23,24] ($\Delta_{ptb} = \tau \frac{d\varepsilon}{dt}$ where τ is the time for the barrier tunneling rate to change by a factor of Euler's number ≈2.718, and ε is the electrochemical potential level of the dot), or the closely related "g" factor[25] ($g = \frac{\alpha_I}{\alpha_{LG} - \alpha_I}$, where α_I is the capacitive lever arm of the pumping gate to the dot, and α_{LG} is the conversion factor from the gate voltage to barrier height). Biasing arrangements have also been discussed elsewhere, with custom AC control signals[8] and AC signal coordination[26] identified as methods to increase plateau width. None of these yield-related issues provide a satisfactory explanation for our results, leading us to explore other error mechanisms.

In this paper, we demonstrate successful pumping in our Si architecture with several two-gate pumping modes. However, we observe a total lack of plateaus when attempting to pump with a single gate in the same architecture. We investigate the absence of single-gate ratchet pumping through modeling to determine the dependencies on (i) the dot not fully unloaded, (ii) subtle dependence on energy parameters, (iii) nonlinear tunneling, and (iv) phase offset and nonequilibrium heating. We finally discuss various mitigation techniques to avoid these mechanisms in the future.

II. EXPERIMENTAL METHODS

In this work, we use Si devices fabricated in a silicon-on-insulator (SOI) architecture,[27] as seen in Fig. 1, as well as GaAs devices, whose fabrication has been covered elsewhere.[28,29] To summarize the Si process, we start with a silicon-on-insulator (SOI) wafer, with 100 nm of Si on top of a 200 nm buried oxide (BOX). After etching the Si layer, the resulting device consists of a 100 nm wide Si nanowire (NW), encapsulated by a 25 nm gate oxide. On top of the gate oxide is a layer of poly-Si patterned into three 100 nm long barrier gates spaced by 100 nm, used for pinching off the two-dimensional electron gas (2DEG). In this work, we only use two adjacent barrier gates and leave the third grounded. After growing a 25 nm layer of isolation oxide, another layer of poly-Si is deposited and patterned to cover the Si nanowire, labeled "Upper Gate" in Fig. 1. This layer is used to invert the nanowire and accumulate electrons in the 2DEG. By applying a positive voltage to the Upper Gate and negative voltages to two lower gates, we can isolate a small region of the 2DEG to create a quantum dot with a total capacitance in the range of 40–100 aF [$E_C = \frac{e^2}{C_\Sigma} = (1.6–4)$meV]. All measurements take place in a cryogen free dilution refrigerator with a base thermometer temperature of 8 mK. Effective electron temperatures caused by noise are estimated to be well above that, approximately 200 mK. AC signals were generated with a Tektronix AWG 70002a 2 channel 25GSa/s arbitrary waveform generator. Current was measured using a Femto DLPCA-200 current pre-amplifier. GaAs device measurement has been very thoroughly covered in a recent paper.[29]

III. EXPERIMENTAL RESULTS

Once the device has been properly biased with DC voltages to create the isolated quantum dot, verified by Coulomb blockade measurements and stability diagrams,[26] we proceed with AC charge pumping measurements. Several papers have already covered the detailed bias procedure for running a device as a single-gate ratchet,[30] two-gate ratchet, or two-gate turnstile.[26] Following the methods outlined there, we tuned up our Si device as a robust pump using two AC signals. We successfully demonstrated plateaus using two different two-gate pumping modes.

The Si two-gate results are shown in Fig. 2, with Fig. 2(a) showing ratchet results from a no-bias pumping mode similar to that shown in other work.[15,31] Here, we see flat plateaus and the number of pumped electrons, n, behaving as expected with respect to gate voltage and AC signal phase offset. In Fig. 2(b), we show results from a turnstile pumping mode[32,33] following the expected trend where n is determined by the gate voltage and bias voltage. These results confirm that AC signals are reaching the device as expected, $E_C \gg kT$, and that the device is functioning as a quantum dot.

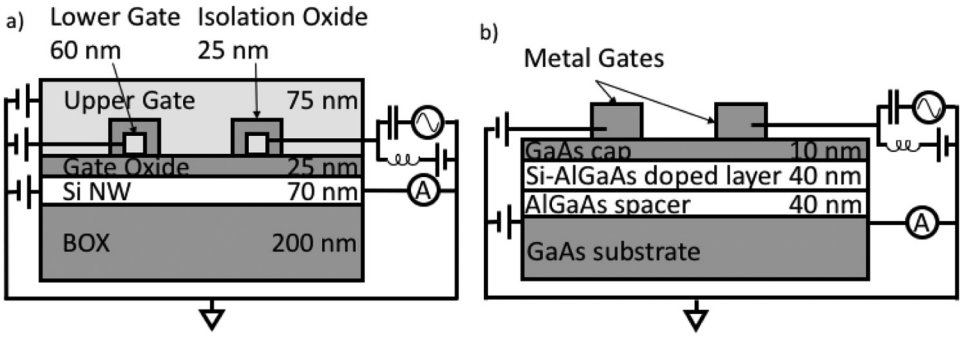

FIG. 1. Schematic of the devices and basic measuring circuits used in this study. (a) Si device, showing the two gates used in this work (a third was fabricated but is left grounded for this study and is not pictured here). The active region of the device is entirely made of Si (white), SiO_X (dark gray), and poly-Si (light gray). The 2DEG was induced in the Si nanowire (NW). (b) GaAs device, where the 2DEG exists in the top of the GaAs substrate and is confined to the region directly under the Si-AlGaAs doped layer, which is 1 μm wide. The two metal gates are used to pinch off the 2DEG and create a quantum dot between them.

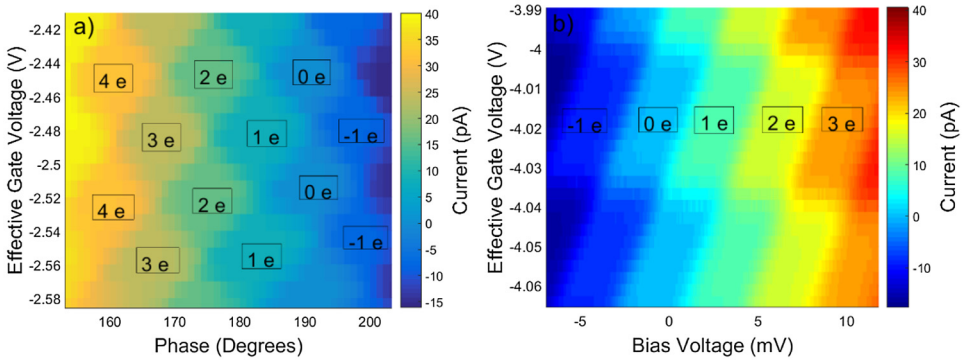

FIG. 2. 50 MHz pumping results for Si device 1, showing expected plateaus using (a) two-gate ratchet pumping with no bias, $P_{RF} = -10$ dBm, $V_{DC} = 0$ V, $V_{UG} = 2.3$ V, $V_{ent} = -2.7$ V to -2.41 V, and $V_{exit} = -2.99$ V, and (b) two-gate turnstile pumping with applied bias as shown and equal amplitude, 180° phase shifted AC signals, $P_{RF} = -10$ dBm, $V_{DC} = 0$ V, $V_{UG} = 2.3$ V, $V_{ent} = -2.63$ V to -2.52 V, $V_{exit} = -3.14$ V to -3.07 V, and T = 10 mK. Here, the effective gate voltage $V_{eff} = -\sqrt{V_{ent}^2 + V_{exit}^2}$.

After confirming that the Si devices were operating as expected with DC measurements and two-gate charge pumping measurements, we proceeded to operate the device with a single AC bias. When only one AC signal was applied, to operate the device as a one-gate ratchet as described in several papers,[12,13,24] we did not observe the expected plateaus. In Fig. 3, we see the pumping map formed by an RF sine wave applied to the entrance gate of a quantum dot. This should produce plateaus similar to the ones seen in Appendix Fig. 8. However, when attempting this measurement with several devices at a wide range of frequencies and RF powers, we were unable to observe any plateaus. Figure 3(a) shows a pumping map from the device used in Fig. 2, where gate voltage limitations prevented us from seeing the entire pumping map. A second device was also measured, which had a less negative turn-off voltage. This allowed us to apply larger amplitude signals and image the entire one-gate pumping region. Linecuts through the pumping maps of both devices show the expected linear trend along each axis [Figs. 3(b) and 3(d)]. GaAs devices did show good one-gate pumping results, with ideal pumping maps shown in other works.[7,30,34]

IV. ANALYSIS

The featureless current seen in Figs. 3(a) and 3(c) does not resemble the expected plateaus, seen in other publications using similar devices. In this section, we present evidence that the featureless current corresponds to the single-gate ratchet mode but without any quantization plateaus. To better understand this

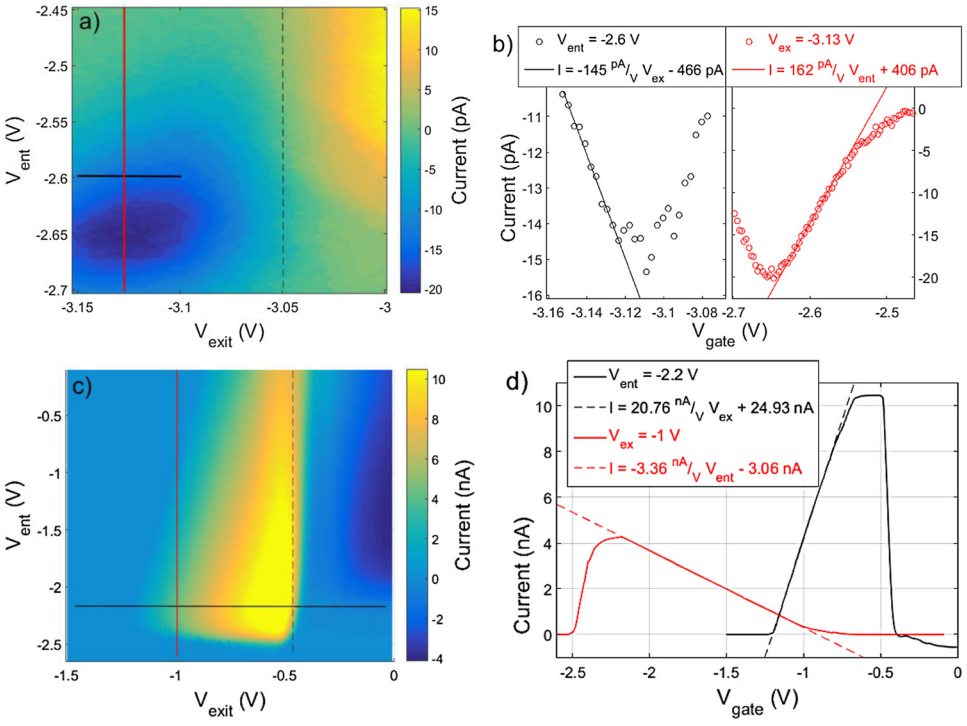

FIG. 3. One-gate ratchet pumping current: (a) Pumping map from device 1, showing the current from pumping in the lower left corner, and rectification current in the upper right corner with a −14 dBm 50 MHz sine wave applied to one gate, $V_{UG} = 2.3$ V. The dotted black line at $V_{exit} = -3.05$ V corresponds to the exit barrier turn-off point. (b) Linecuts through (a) showing the linear portions of the current and fits to the data. (c) Device 2 showing a pumping map from a 10 dBm 500 MHz sine wave, with lines showing where linecuts were taken. The current direction is opposite from device 1 due to connecting the current pre-amplifier to the entrance lead instead of the exit lead. The bright yellow flat region is due to the current preamplifier saturating above 10 nA. As in (a), the dotted black line corresponds to the barrier turn-off. (d) Linecuts from (c), showing linear regions in the pumping region, with the fits shown here.

current, we started by considering the ideal pumping map [shown in (A1)]. This was originally described by Kaestner and Kashcheyevs,[24] and the equations governing the plateau transitions were described by d'Hollosy *et al.*[35] This prediction of a one-gate ratchet pumping map has been observed many times in the literature,[30,36,37] and also holds true for other situations, such as pumping where the dot is not fully emptied[35] or where the swept gate is a plunger gate and not the exit barrier gate.[13] If the plateau width goes to zero due to some large error mechanism, we lose quantization and expect a sweep along either the entrance or exit barrier to be linear within the pumped current region. The expected slope of the linecut in the entrance direction can be described simply by

$$m_{V_{ent}} = \frac{dI}{dV_{ent}} = fC_{ent\text{-}dot}. \quad (1)$$

Here, $C_{ent\text{-}dot}$ is the capacitance between the entrance gate and the dot. Equation (1) was derived from standard expressions for the energy of a quantum dot, under the assumption that the single-particle energy spacing is much smaller than the electrostatic charging energy.[35,38] The expected slope of the linecut along the exit gate is also linear, and a full physical description can be found elsewhere.[35] Figure 3(b) shows the linecuts along the entrance and exit barrier compared to a linear fit, showing that the trend is linear.

To support our thesis that the featureless current corresponds to single-gate ratchet mode, but without any quantization plateaus, we have compared capacitances derived from DC measured values to those derived from the linecuts (Table I). The DC measured values of all capacitances are taken from Coulomb blockade oscillation measurements and diamond diagrams. These measurements were all taken using DC transport, which occurs in the range where both barrier gates allow conduction. As seen in Figs. 3(a) and 3(c), pumping occurs at more negative gate values, when no DC transport can occur. The "Pumping Fit Value" is obtained from Eq. (1), using data from two independent sets of experiments (in particular, by switching "ent" and "exit" directions). We expect the gate capacitances in the DC transport regime to differ from the values in the pumping regime; however, the apparent agreement between DC and Pumping Fit Values leads us to believe that the featureless current corresponds to single-gate ratchet mode, but without any quantization plateaus.

TABLE I. Comparison of capacitances and capacitive lever arms deduced from DC transport, and from linecuts of pumping data in Fig. 3. Pumping Fit Values α_{ent} and α_{exit} are derived from the charging energy measured with the two-gate turnstile, given by the plateau spacing along the bias voltage axis in Fig. 2(b). Relative errors are estimated to be less than 10%. The agreement supports the thesis that the featureless current corresponds to single-gate ratchet mode but without any quantization plateaus. We note that the agreement of α_{ent} and α_{exit} simply represents the agreement of E_C derived from DC and pumping data. E_C for devices 1 and 2 measured from DC data = 3.5 and 1.6 meV, respectively.

Variable	Device 1 DC measured value	Device 1 pumping fit value	Device 2 DC measured value	Device 2 pumping fit value
$C_{ent\text{-}dot}$	2.1 aF	3.2 aF	11.4 aF	6.7 aF
$C_{exit\text{-}dot}$	2 aF	1.9 aF	8.4 aF	6.2 aF
α_{ent}	0.045	0.07	0.12	0.11
α_{exit}	0.043	0.04	0.09	0.1

The reasonable device parameters extracted from the linecuts and the shape of the pumping map are both good evidence that the current is due to one-gate ratchet charge pumping but without quantization. Another requisite feature of the pumped current is its reaction to applied frequency. Figure 4 shows the current at a specific value of gate voltage as a function of frequency. While no plateaus were visible in the pumped current, the current still obeys the expected relation with frequency. Rectification current (discussed further in Appendix B) appears in Figs. 3(a) and 3(c) when the exit barrier becomes conductive (to the right of the vertical dashed line) but does not affect the current in the pumped region. This confirms that the current visible in Fig. 3(a) is due to charge pumping and not from some other effect.

We can augment these detailed results on lack of single-gate ratchet pumping with an additional statistical study, which does not include testing two-gate pumping. Part of our team has been making mesa-etched GaAs pumps with a single layer of surface gates.[34] After fabrication optimization of size and shape, we have tested a large number of devices for single-gate ratchet pumping. Out of approximately 135 devices tested at 4.2 K, approximately 125 (over 90%) showed correct pumping characteristics with current quantization plateaus (although generally the plateaus were not flat without applying a magnetic field). The most common failure is the presence of an additional pump, probably formed due to the disorder potential, in parallel with the lithographically defined pump.

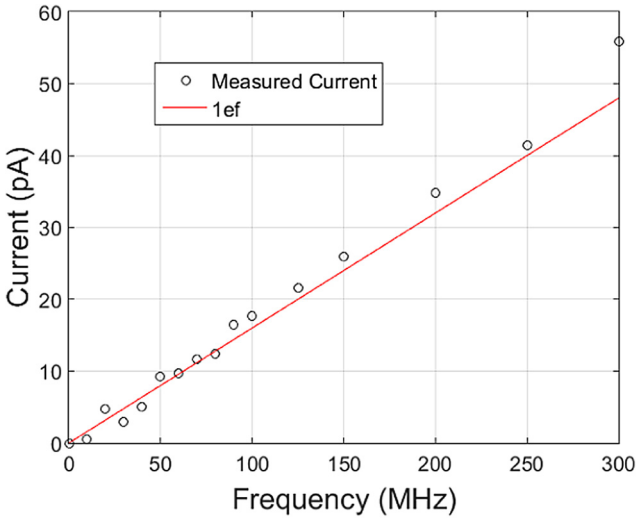

FIG. 4. Current vs frequency for device 1 under single gate operation, showing the expected linear trend and giving further evidence that current seen in Fig. 3(a) is due to charge pumping. The Upper Gate voltage for this data is lower than that used in Fig. 3(a): $V_{UG} = 2$ V, $V_{ent} = -2.18$, $V_{exit} = -2.88$ V, $P_{RF} = -14$ dBm.

In the later sections of this work, we will describe several mechanisms to explain the combination of our success in generating two-gate pumping but fail to see single-gate ratchet pumping in the Si devices, as described above. We did not test any of the approximately ten GaAs devices that failed to show single-gate pumping to see if they work in two-gate modes described above; however, we will also discuss how these mechanisms are consistent with over 90% of GaAs devices that show single-gate ratchet pumping. For this later discussion, some of the significant features of the GaAs devices are as follows:

(1) The GaAs base carrier density is determined by modulation doping, rather than an enhancement mode using a top gate. This requires only a single layer of gates.
(2) The GaAs devices generally have very smooth turnoff curves (i.e., the current is a smooth function of the gate voltage for a single tunnel barrier, rather than showing resonances). This is generally due to cleaner epitaxial interfaces, unlike oxide layers present in Si devices.
(3) The GaAs devices operate in the $N = 1$ limit and have a smaller number of electrons (~10) loaded onto the dot and then back-tunneling from the dot to the source; in the Si devices described in this paper, there are a larger number of electrons being loaded and unloaded.

V. ERROR MECHANISMS

While the linecuts and frequency behavior indicate that the device is operating as a charge pump, they do not suggest what is preventing plateaus from forming. The DC performance of the device, coupled with successful pumping using two separate AC signals as shown in Fig. 2, suggest that simple problems, such as E_C/kT being too low, poor AC transmission to the device, or the dot forming in an unintentional location, are not the limiting factor. Here, we explore several possibilities as to what is eliminating plateaus, investigating the plunger to barrier ratio Δ_{ptb}, cross capacitances in the device, and resonances in the tunnel barriers.

A. Dot not fully emptying

Due to the lack of a separate plunger gate and the large capacitive lever arm of the Upper Gate, the Si device is operating with a large number of electrons on the quantum dot. Most studies (as well as the GaAs devices in this study) have focused on the dot completely emptying during unloading (bottom of the pumping map in Fig. 8). This has several benefits, including a larger E_C due to the smaller capacitance at more negative barrier gate voltages and the lack of errors when unloading. A large number of electrons can also cause state preparation errors. Because of nonadiabatic state transition and electron–electron interactions, we cannot assume that the dot is always in the ground state in our dynamic system. Each time we capture multiple electrons, the configuration of their state occupation can be different from previous cycles. This results in a different total energy of the system between cycles and smears out the plateaus. The larger the number of captured electrons, the larger the smearing effect. This loading of excited states has been observed in previous studies.[34] However, all studies showing data similar to that in Fig. 3 show several plateaus where the dot is not fully unloading, and indeed one study seems to take place where no plateau fully empties the dot.[35]

Although studies such as d'Hollosy *et al.*[35] indicate that quantized pumping is possible without fully emptying the dot, it is possible that this single error mechanism is preventing visible plateaus. Regardless, this should not impact the analysis of other possible error mechanisms that follow. This error mechanism also does not affect two-gate pumping methods, as the loading of the dot can be controlled to always position the Fermi level of the lead in resonance with the first empty occupation level of the dot, preventing loading of excited states.

B. Dependence on energy parameters

Several papers have discussed Δ_{ptb} and its effect on pumping, investigating Δ_{ptb} vs the critical time τ,[23] the temperature kT,[30,39] and briefly discussing it with respect to the charging energy E_C.[24] For the one-gate ratchet pumping mechanism to work, we require some cross capacitance between the gate and the dot. The smaller this cross capacitance, the larger the necessary AC signal becomes to elevate the dot's electrochemical potential above the exit barrier. This sets a lower limit that $\Delta_{ptb} > 0$. In practice, a large AC signal produces local heating, and this sets a somewhat higher value for the lower limit on Δ_{ptb}. An upper limit on Δ_{ptb} however, has not been studied.

To better investigate the effect of Δ_{ptb} on pumping, we used a master equation approach[40–42] to determine how many electrons are left on the dot after the loading phase,

$$E_n(t) = -E_C\left(F - n - \frac{\Delta_{ptb}}{E_C}\frac{t}{\tau}\right) + eV_G, \tag{2}$$

$$\Gamma_n = \Gamma_{0,n}(1 + e^{-\beta E_n(t)})^{-1} e^{\frac{-t}{\tau}}, \tag{3}$$

$$\frac{dP_n(t)}{dt} = -\Gamma_n(t)P_n(t) + \Gamma_{n+1}(t)P_{n+1}(t), \tag{4}$$

where F is the Fermi level in units of E_C, V_G is the gate voltage, Γ_n is the tunnel rate of the nth electron out of the dot, $\beta = 1/\mathrm{kT}$, and P_n is the probability that the dot has n electrons (starting with the initial condition $P_n(0) = 0$, $P_N(0) = 1$). We also used a barrier width of 30 nm with a starting height of 100 meV in determining $\Gamma_{0,n}$. We calculated P_n by numerically integrating Eq. (4) to $t > 10\tau$ and then calculated the average number of captured electrons by using the expectation value. The number of expected electrons left on the dot after the loading step is shown in Fig. 5. Figure 5(a) shows the number of electrons captured as a function of a plunger gate voltage. This shows the expected plateaus, with more electrons being captured as the dot is plunged further. When we vary the ratio Δ_{ptb}/E_C, we see the plateaus begin to degrade, becoming nearly completely washed out by the time Δ_{ptb}/E_C is 0.4. In their device, Giblin *et al.*[30] estimated $\Delta_{ptb} = 1$ meV with a charging energy that appears to be larger than 10 meV, resulting in a ratio of less than 0.1.

The most relevant work in exploring error rates when loading is the universal decay cascade model, first outlined in 2010 by

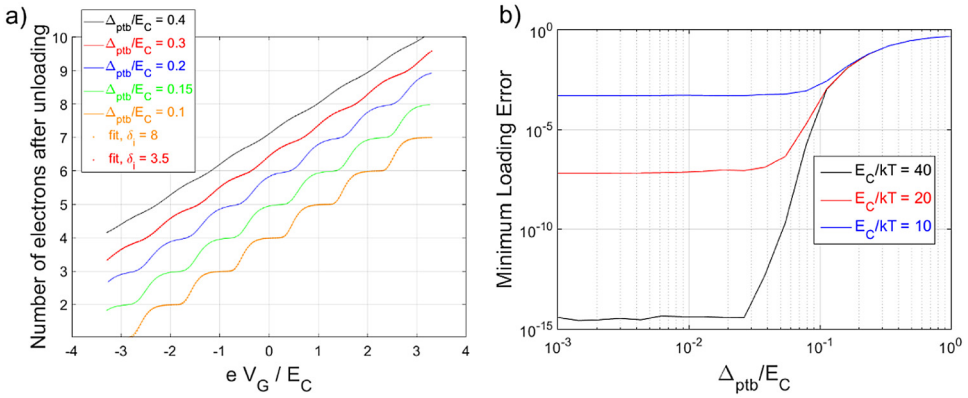

FIG. 5. The number of captured electrons depends on several parameters, including Δ_{ptb}. (a) Captured electrons vs plunger gate voltage at several values of Δ_{ptb}. The curves show a loss of quantization over a narrow range of Δ_{ptb}/E_C. Two curves have fits to Eq. (5), with excellent agreement between the equation and the data. $E_C = 1.4$ meV, T = 1.5 K. (b) Error rates during the loading phase, representing the minimum possible error at different temperatures.

Kashcheyevs and Kaestner.[41] We fit the plateaus seen in Fig. 5(a) to the universal decay cascade equation,

$$n = \sum_{m=1}^{N} \exp(-\exp(-\lambda V_G + \Delta_m)), \tag{5}$$

$$\delta_i = \Delta_i - \Delta_{i-1}. \tag{6}$$

N is the number of electrons initially on the dot, and both λ and Δ_m are fitting parameters, and Eq. (5) is fit to the plateaus shown in Fig. 5(a). Equation (5) is a close fit to the model output, with two fits shown in Fig. 5(a). We can also extract error rates from our model, shown in Fig. 5(b). These minimum error rates were found by taking $1 - P_n$, when n = the expectation value of the number of pumped electrons. These error rates are only for the loading step in our model, which only considers errors from the wrong number of electrons back-tunneling from the dot to the source while the barrier rises. Therefore, this is the minimum error rate possible during pumping with the given parameters. As can be seen in Fig. 5(b), at low values of Δ_{ptb}/E_C, errors are mostly thermal. Once Δ_{ptb}/E_C gets larger, the dominant error mechanism becomes capturing an incorrect number of electrons on the dot, due to many electrochemical potential levels being over the source's fermi level during the capture phase. Figure 5(b) shows that lowering Δ_{ptb}/E_C should be a priority and reaching a value of $\Delta_{ptb}/E_C < 0.1$ is necessary for a low error charge pump.

We can compare the estimated error rates in Fig. 5(b) to other studies. The comprehensive charge pumping review article by Kaestner and Kashcheyevs[24] provides two straightforward minimum error rate predictions that we can compare to our predictions,

$$\min P_{err} \approx 2\delta_2 \exp(-\delta_2), \tag{7}$$

$$\min P_{err} \approx 2e^{-E_C/(2kT)}. \tag{8}$$

Equation (7) provides a connection from the fitted curves in Fig. 5(a) to the error rates in Fig. 5(b), showing that δ_i of 3.5 and 8 ($\Delta_{ptb} = 0.3$ and 0.1) correspond to error rates of 0.2 and 5×10^{-3}, respectively. These error rates correspond well with the predicted error rates in Fig. 5(b) even though the models consider different error mechanisms. The thermal errors predicted by Eq. (8) do not correspond well with Fig. 5(b), with Eq. (8) predicting that $E_C/\mathrm{kT} = 40$ should result in a minimum error rate of 4×10^{-9}, which is significantly higher than predicted by our model. We can also compare these to recent results in the literature, with Zhao *et al.*[37] finding $E_C/\mathrm{kT} = 22$ in their device and predicting a minimum error rate of 4×10^{-12}, which is less than both our model and predictions from Eq. (8). This discrepancy is likely due to the use of a thermal-capture model in the study by Zhao *et al.*[37]

DC transport measurements of Δ_{ptb}/E_C on our device suggest that the value could be as high as 2, found using $\frac{dV}{d(\ln(I/I_0))}\frac{C_{ent}}{e}$ (where $I_0 = 1$ A). While this ratio may change when the dot is operating in the pumping regime, as seen in Table I, it is still much higher than $\Delta_{ptb}/E_C < 0.1$ required for low error pumping. A ratio as large as 2 can easily blur out plateaus and lead to the featureless, linear slope of current that we see in Figs. 3(b) and 3(d). This is a likely problem for our Si devices, but it may not be the only source of error.

C. Nonlinear barrier resonances

Another error mechanism we identified arises from resonances in the tunnel barrier. Figure 6(a) shows the turn-off curves for our entrance and exit gates from the device used in Fig. 3(a). Both gates show significant variations from the expected exponential turn-off, also shown in Fig. 6(a). These variations are attributed to unintentional quantum dots, forming under the gates as they pinch off the 2DEG and create a tunnel barrier. We observe similar non-monotonicity on nearly all of our Si single-gate turn-off measurements at low temperatures. These resonances create regions where the tunnel rate through the barrier will suddenly increase during turn-off. In effect, these resonances increase τ by making the barrier less steep, increasing Δ_{ptb} and increasing error rates. Modeling these resonances using the master equation approach outlined earlier, with resonances added to the gamma term, produces similar responses to variations in Δ_{ptb}, washing out plateaus. Similar issues with quantization caused by unintentional quantum dots were modeled and observed with a two-gate ratchet pumping method.[43] These issues did not affect pumping so long as gate voltages were properly chosen to avoid interactions with unintentional

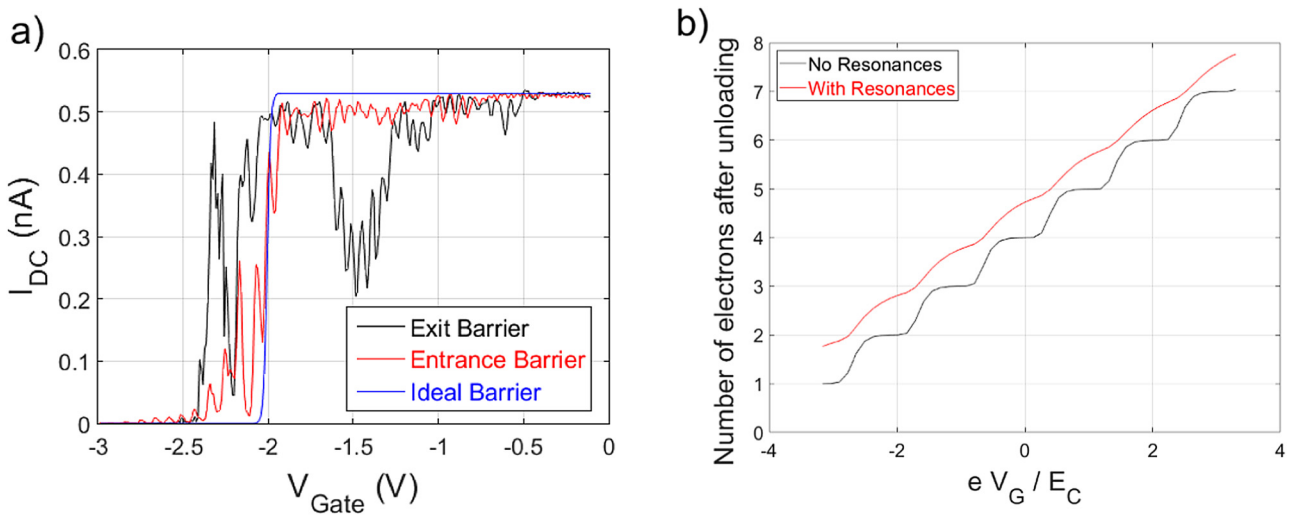

FIG. 6. (a) Single gate sweep from Si device 1, showing resonances as the gates turn-off conduction through the channel (For red and black curves, $V_{DC} = 0.8$ mV, $V_{UG} = 2.3$ V, and all other gates are grounded). The figure also shows, for example, an ideal exponential turnoff curve with no resonances and a steepness of 20 mV/decade. (b) Simulation using the master equation approach from Eq. (4) with an exponential tunneling rate (No Resonances), and an exponential tunneling rate with large resonances included (With Resonances). The curves in (b) are intentionally offset.

quantum dots but reduced or eliminated pumping quantization when an unintentional dot could be loaded or unloaded during the pumping steps. Resonances were also observed to complicate pumping with the one-gate ratchet method,[44] though this study found a regime of operation where the resonances did not impact accuracy.

D. Phase offset and heating

In Figs. 3(a) and 3(c), we can see a region where the sign of the current changes from negative to positive (right of the vertical dashed line). This current change is likely due to rectification current,[45] a result of cross capacitances in the device. We can use the rectification current model laid out by Giblin *et al.*[45] to gain some information about capacitances in our device. Further description of the model can be found in Appendix B. The rectification model reveals an induced bias of 8 mV_{pp} while pumping. This induced AC signal is still small compared to the barrier height used while pumping but indicates that the applied AC signal is capacitively coupling to other parts of the device.

To estimate the induced AC signal on different gates, we created a simple circuit of the device (shown in Appendix B, Fig. 10). This circuit used estimates of the capacitive coupling, inductances, and resistances, taken from the design of the device and DC measurements. We can use the circuit model to estimate the phase difference between the applied AC signal and the dot when taking into account the induced AC signal.

The phase difference between the applied AC signal and the dot is shown in Fig. 7, with the phase of the dot being greater than the phase of the barrier modulation. We assume the barrier height moves in phase with the applied AC signal. The source of this phase difference is capacitive coupling between the gate and the Upper Gate, and the Upper Gate and the dot, combined with resistances and inductances in the device. The capacitive coupling between the Upper Gate and the dot is two to three times larger than the coupling between the barrier gate and the dot, so any induced AC signal on the Upper Gate will cause a change in the

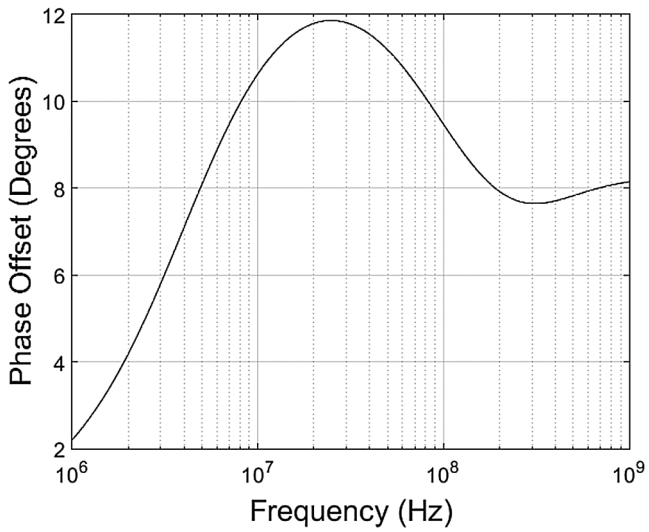

FIG. 7. An RC model of the system (Appendix B) predicts phase offset between the applied AC signal and the dot, with the phase of the dot being greater than the phase of the applied AC signal. This phase offset can lead to hot electrons loading onto the dot.

dot's electrochemical potential level during pumping. If there is a phase difference between the applied AC signal and the AC signal on the Upper Gate, it will cause some phase difference between the applied AC signal and the dot. This phase difference can cause problems while pumping if the phase of the dot's electrochemical potential level is different from the phase of the barrier.

If the phase of the dot is greater than the phase of the barrier modulation, the dot's electrochemical potential level will be well below the source's Fermi level before the entrance barrier tunneling rate becomes high enough to allow tunneling. This can result in a large energy loss for each electron that tunnels onto the dot, causing localized heating. For the large 10 dBm pumping signal shown in Fig. 3(c), a 12° phase difference would lead to the dot being 8 meV below the source Fermi level when $\Gamma_{\text{entrance}} < 1/\tau$. This will cause two to three electrons to rush onto the dot, converting $(3+2+1)$ $E_C \sim N^2/2E_C$ (~14 meV for our device) into phonons. The electron–phonon cooling is proportional to $(T_e^5 - T_{\text{latt}}^5)$,[40] resulting in an electron temperature increase of $T_e \sim N^{2/5}$, or 2.5× hotter than if the dot and barrier oscillated in phase. Following the procedure by Zimmerman *et al.*,[40] with a 10 dBm, 500 MHz signal, the 12° phase offset can result in an electron temperature of 3.5 K. This localized heating significantly raises kT, reducing plateaus and contributing to the featureless pumping map shown in Figs. 3(a) and 3(c). It should be noted that N in this analysis is the number of electrons originally loaded onto the dot, not the number captured, as electrons can tunnel back off the dot before the capture phase is complete.

If the dot lags behind the barrier, the main error mechanism would be the entrance barrier beginning to fall when the dot's electrochemical potential is still rising. If the entrance barrier is of similar height to the exit barrier when the dot's electrochemical potential is near the height of both barriers, then the electron could tunnel back to the source, causing a significant error. Whether the phase of the dot is greater or less than the phase of the barrier, error rates increase, and this capacitive coupling should be minimized. This capacitive coupling is not a limiting factor in the two-gate pumping schemes due to the second AC signal, which is of similar amplitude and shifted by nearly 180°. These two AC signals will cancel the induced AC signal in other parts of the device, eliminating potential issues and creating robust pumping plateaus. This capacitive coupling is also reduced in GaAs devices due to the lack of an Upper Gate.

E. Methods to reduce error mechanisms

The four error mechanisms we have laid out here can each independently increase errors or eliminate pumping altogether. Each of these mechanisms is reduced or eliminated in pumping modes using a second phase-shifted AC signal. They are also each reduced or eliminated in GaAs devices. In order to reduce these errors in devices using only a single AC signal, several design changes could be beneficial. The first is to reduce the number of electrons remaining on the dot after pumping, ideally to 0. This can be accomplished with a separate plunger gate, allowing the electrochemical potential of the dot to be modulated independent of the leads or the barriers. The second is to reduce Δ_{ptb}, which holds true regardless of the materials system. This can be accomplished in several ways, but the simplest is to reduce the oxide/spacer thickness between the barrier gate and the 2DEG. As this thickness decreases, it will increase the capacitive coupling between the barrier gate and the barrier, lowering Δ_{ptb}. Another possibility would be to increase the barrier gate length, which would decrease the "transverse energy"[24,40] and make the barrier turn-off steeper. However, we do not recommend increasing the barrier length, as it tends to increase the number of resonances due to unintentional quantum dots under the barrier in Si devices. In fact, to decrease resonances in the device, a shorter barrier gate is beneficial. This optimal barrier length, short enough to reduce/eliminate resonances and long enough to minimize the transverse energy, and thus Δ_{ptb}, depends greatly on device specifics and must be optimized for specific materials and fabrication methods.

The most apparent method to minimize issues due to cross capacitance (rectification, phase shifts of the dot, etc.) is to reduce capacitance between gates and between DC gates and the dot. GaAs devices, which have no Upper Gate and often have larger spacings between gates, naturally have a lower cross capacitance than Si devices. Nippon Telegraph and Telephone (NTT) has created Si devices with a similar design to our own, which have a ratio between the Upper Gate lever arm and the barrier gate lever arm of 0.3[13] and have demonstrated one-gate pumping. This lower capacitance helps to eliminate complications due to phase shifts in the dot. Alternatively, reducing the capacitance between the Upper Gate and the barrier gate will also help reduce the induced signal on the device. This can be achieved by splitting the Upper Gate into a plunger gate and two other gates to invert the ohmic leads to the device, resulting in a device similar to those fabricated at the University of New South Wales (UNSW), which have been shown to operate as robust pumps.[37,46] It also helps to lower Δ_{ptb} by reducing the extra plunger effect from induced AC signals on non-controlled gates.

Reducing the impedance to ground of DC controlled gates can also reduce the induced AC signal. This can be achieved by increasing capacitance between the gate and ground near the device or reducing the series impedance from the gate to the DC voltage source. Either of these approaches will reduce the unintentional AC signal at the device and should reduce errors in one-gate ratchet pumping mode (Table II).

TABLE II. Summary of main error mechanisms with suggestions to reduce these errors.

Type	Result	Parameter	Solution
I. Dot not emptying	Plateaus not visible	$N_{\text{electrons}} > 0$	Separate plunger gate
II. Δ_{ptb}/E_C	Plateaus not visible	$\Delta_{ptb}/E_C > 0.4$	Decrease $C_{\text{gate}-\text{island}}$
III. Resonances	Plateaus reduced by 90%	Many resonances	Reduce defects in Si barrier
IV. Phase offset	Plateaus reduced by 30%	$\Delta\Phi = 12°$	Decrease $C_{\text{gate}-\text{island}}$

VI. CONCLUSIONS

We have shown pumping results from Si devices fabricated in an SOI architecture, with plateaus using two AC signals, but no plateaus with only a single AC signal. The one-gate current produced by two of our devices agrees with the expected pumping current with no visible plateaus. This lies in contrast to GaAs devices, which have a much higher yield and have demonstrated one-gate pumping. We proposed four possible reasons for the lack of plateaus: a large number of electrons on the dot, a plunger-to-barrier ratio that is too high, resonances in the tunnel barrier, and cross capacitances in the device. Future Si devices will benefit from several design changes, notably reducing the gate oxide thickness, reducing the barrier length, and reducing capacitances in the device. These recommendations may prove useful to the community at large in producing more robust, higher yield one-gate ratchet pumps.

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APPENDIX A: ONE-GATE RATCHET PUMPING MAP

To determine what a pumping map should look like if the plateau width went to 0, we started by considering the ideal one-gate pumping map. When pumping a quantized number of electrons each cycle, plateaus should occur within the solid black lines shown in Fig. 8. As the AC signal shrinks or the plunger gate voltage increases, the loading line moves up to higher entrance gate voltages, and the tall plateaus in the figure shrink and eventually all plateaus become equal in size once we reach the large N limit. The slopes and equations governing the shape of this pumping map are described elsewhere[35] and typically describe step functions of current to trace out the expected plateaus. If some error mechanism is large enough to cause plateaus to completely disappear, so that current is linear in any direction, a gate sweep of the entrance or exit barrier would produce a linear change of current. That linear current would have the following slope along the entrance gate axis,

$$m_{V_{ent}} = fC_{ent\text{-}dot}, \tag{A1}$$

where $m_{V_{ent}}$ is the slope along the entrance barrier axis. Figures 3(b) and 3(d) in the main text show that these fits to a small portion of the pumping curve, limited by the gate voltages. If there were no error mechanisms, one would expect the pumping maps shown in Fig. 3 to closely resemble the sketch below in Fig. 8.

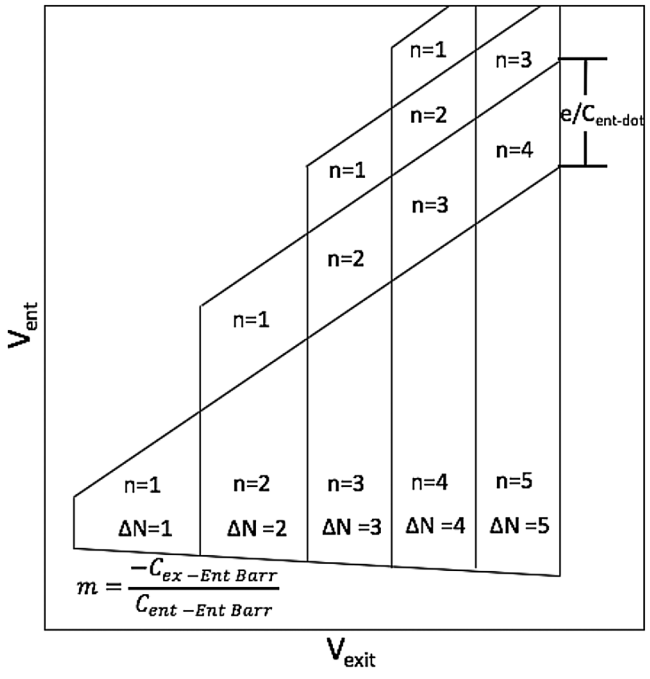

FIG. 8. Pumping map with plateau regions and slope of loading line indicated. The solid black lines indicate transition regions where the number of pumped electrons, n, changes. ΔN is the number of electrons captured after the loading phase ends, and n is the total number of pumped electrons.

APPENDIX B: RECTIFICATION CURRENT

The effect of cross capacitances in a charge pump has been explored previously by Giblin *et al.*,[45] where an AC signal applied

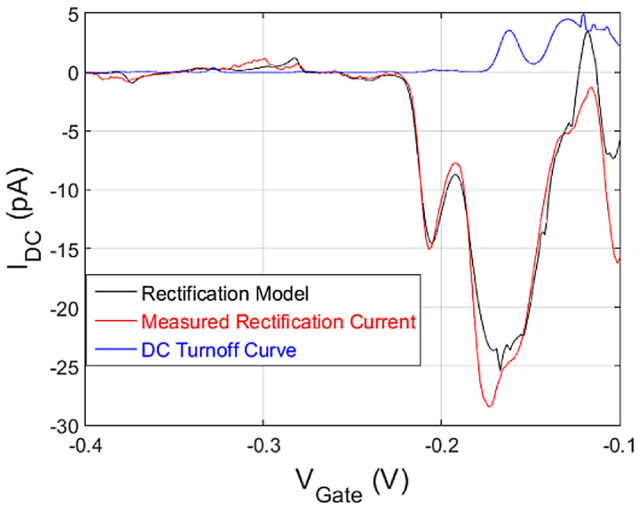

FIG. 9. Single gate turn-off sweeps, illustrating DC and AC response, from device 2. The blue curve shows the data from a single gate sweep scaled down by a factor of 100, with a small DC bias, where the current turns on once the gate voltage reaches a high enough value. The red curve shows a sweep of the same gate, with no DC bias and an applied AC signal. The black curve is the model, fit to the red curve, producing the fit parameters of $V_{DC} = 25\,\mu$V (expected value of 0 V), $V_{AC} = 95$ mV (expected value of 100 mV), and a coupling parameter k of -2.2×10^{-3}. Blue curve taken at $V_{DC} = 0.8$ mV, $V_{UG} = 2.5$ V, $V_{LGC} = V_{LGD} = 1$ V, no V_{AC}. Red curve taken at $V_{DC} = 0$ mV, $V_{UG} = 2.5$ V, $V_{LGC} = V_{LGD} = 1$ V, V_{AC} on LGS = 5 MHz 50 mVpp sine wave.

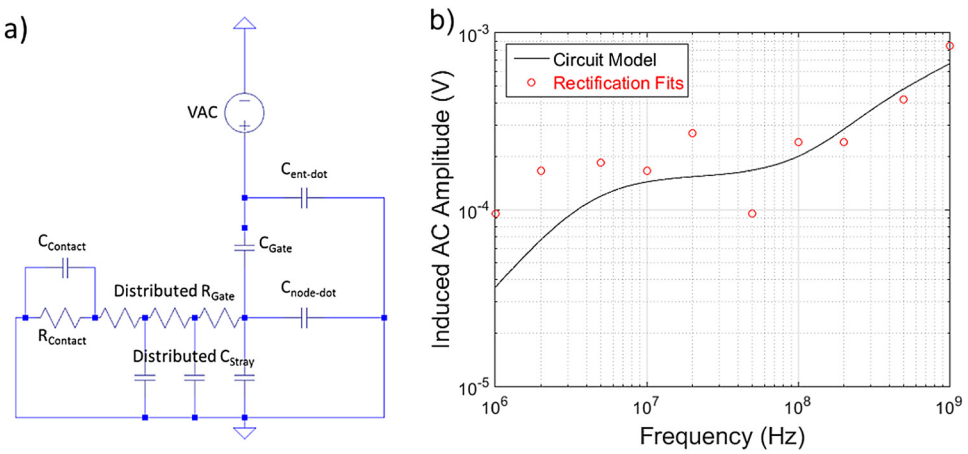

FIG. 10. (a) Circuit model of the device, including a capacitance to ground distributed among the gate resistance. (b) Fits from rectification data similar to Fig. 9 from device 2 showing voltage at the node indicated in (a) as a function of frequency, compared to the induced voltage measured with the rectification model, using the parameters $C_{Contact} = 1 \times 10^{-15}$ F, $R_{Contact} = 6 \times 10^{5}\ \Omega$, $C_{Gate} = 9 \times 10^{-16}$ F, $C_{Stray} = 6 \times 10^{-14}$ F, $R_{Gate} = v6 \times 10^{4}\ \Omega$.

to a single barrier can create current flow. This is a useful tool for exploring cross capacitances in a device, and we applied the model proposed by Giblin to our device. The model is applied to every point on the gate sweep and reduces to $I = \text{mean}(kV(t)G(t))$, where k is a fitting parameter to determine the capacitances, V is the applied AC voltage, and G is the conductivity of the barrier measured with DC transport. In Fig. 9, we see that the current changes significantly from the DC to the AC case, and that the rectification model fits the data very well. This suggests a large capacitive coupling at the device and a large induced AC signal (at least 8 mV under typical pumping conditions).

In Fig. 10(b), we compare the estimate from our circuit model [Fig. 10(a)] to the induced AC bias deduced from the rectification current model. The original estimates of the circuit parameters were used to set ranges, and the model was varied within that range to produce the best fit to the rectification data. We see that our circuit model follows the same trend as the data from the rectification current model, suggesting that our circuit model is a close estimate of the actual device. Resonances and reflections due to non-idealities in the device are the most likely culprit for the variations in the rectification current.

The agreement between the circuit model and the data measured from rectification current showed that our circuit model approximates the device. This allowed us to extract the phase of the dot compared to the AC circuit applied to the barrier. Since the AC signal on the node in Fig. 10(a) is phase shifted from the applied AC signal, and knowing the capacitance between various nodes on the device and the dot, we approximated the phase. This is discussed further in the main text.

Further details on the devices can be found here for future reference. Device 1: MS-3GGL4-25, 100 nm dot with 100 nm long gates, L:\internal\SET_data\dry DR I\Runs\MS-3GGL4-25, Entrance Gate = LGS, Exit Gate = LGC

Device 2: MS-3GGL4-36, 100 nm dot with 200 nm long gates, L:\internal\SET_data\dry DR I\Runs\MS-3GGL4-36, Entrance Gate = LGC, Exit Gate = LGD

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