Effect of device design on charge offset drift in Si/SiO_2 single electron devices

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We have measured the low-frequency time instability known as charge offset drift of Si/SiO_2 single electron devices (SEDs) with and without an overall poly-Si top gate. We find that SEDs with a poly-Si top gate have significantly less charge offset drift, exhibiting fewer isolated jumps and a factor of two reduction in fluctuations about a stable mean value. The observed reduction can be accounted for by the electrostatic reduction in the mutual capacitance C_m between defects and the quantum dot, and increase in the total defect capacitance C_d due to the top gate. These results depart from the prominent interpretation that the level of charge offset drift in SEDs is determined by the intrinsic material properties, forcing consideration of the device design as well. We expect these results to be of importance in developing SEDs for applications from quantum information to metrology or wherever charge noise or integrability of devices is a challenge.

I. INTRODUCTION

Single electron devices (SEDs) have many important applications due to their ability to localize and manipulate individual electrons' degrees of freedom. SEDs have been proposed as current standards in electrical metrology,[1–9] and as memory and logical devices in integrated circuits.[10–14] They have also been studied as qubits, when there are only a few electrons on the quantum dot.[15–19]

In further developing SEDs for use as qubits or in metrology, charge noise has emerged as a significant limitation. Noise due to two-level systems (TLSs) has been studied in superconducting qubit systems and shown to limit the coherence times.[20] Similarly, semiconducting qubits in GaAs[21], SiGe[22], and Si[23,24] are also limited by charge noise. In the pursuit of a single-electron current standard, charge noise has been shown to limit the number of devices which can be operated in parallel,[3,6] limiting the current generated and the applicability of the resulting standard. While some techniques[25? ,26] and architectures[27] have been developed to mitigate the effects of charge noise on qubit operation, noise remains a significant challenge.

Here, we focus on a long-standing, low-frequency aspect of charge noise known as charge offset drift $Q_0(t)$ which primarily prevents integrability of SEDs.[28] A prominent interpretation of charge offset drift viewed any drift as a consequence of intrinsic material properties.[28,29] This material system explanation is based on the experimental fact that SEDs made in two material systems have very different $Q_0(t)$: Al/AlO_x-based SEDs exhibit a large change in charge offset ($\Delta Q_0 > 1\,e$), while in mesa-etched Si/SiO_2-based silicon-on-insulator (SOI) devices the change of charge offset is small ($\Delta Q_0 < 0.01\,e$). Here e is the electron charge and the value of $Q_0(t)$ is normalized to the period of the Coulomb oscillations.[29] This experimental fact is interpreted microscopically as a distinct difference in the level of interaction between two-level system (TLS) defects present in the amorphous insulators, AlO_x and SiO_2. Specifically, TLS defects are not stable over time or gate voltage sweeps in Al/AlO_x devices, while they are stable in Si/SiO_2 devices.[28,29] Unsuccessful attempts to reduce ΔQ_0 in Al/AlO_x-based SEDs with different device geometries and structures lend additional weight to this materials-only explanation[30] which has had significant influence over the direction of SED research by emphasizing the expected performance edge implied for Si devices.[28] However, noise measurements have only been done in a very limited set of Si/SiO_2 based SED device structures: mainly mesa-etched SOI devices[31,32] and Si SEDs with metal gates.[33,34]

Workers at Sandia National Laboratories and the University of Sherbrook have pioneered fabrication of Si/SiO_2-based SEDs with a single layer of doped polysilicon gates.[35,36] Those devices present an opportunity to assess the robustness of the above explanation for $Q_0(t)$ because they do not have a blanket gate to function as an SED, and their $Q_0(t)$ behavior differs from the mesa-etched SOI devices while not altering the Si/SiO_2 material system.[36] In this manuscript, we present data showing that Si/SiO_2 single gate layer devices show significantly larger ΔQ_0 than their SOI counterparts and, moreover, that ΔQ_0 can be reduced with the addition of another gate covering the fine area of the device. This design change mimics the gate stack of the very stable SOI

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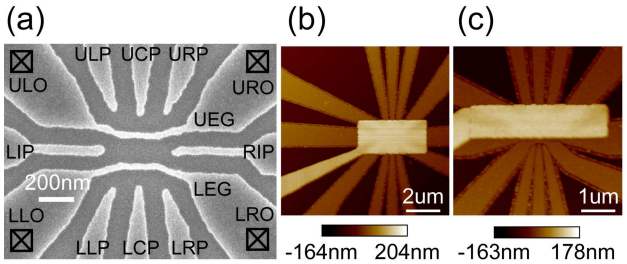

FIG. 1. The different types of devices employed in this study. (a) SEM image of a single gate layer device, showing poly-Si gates on gate oxide, referred to as "bare". Two individual single electron devices (SEDs) can be formed underneath positively biased enhancement gates UEG and LEG, while other plunger gates are used to define the quantum dot. (b) Atomic force microscope (AFM) image of an SED device with a full poly-Si top gate, referred to as "TG". (c) AFM image of an SED device with a half poly-Si top gate. The upper SED is covered by the poly-Si top gate ("TG"), and the lower one is not and is referred to as "oxide". Lower gates in these devices have the same geometry.

devices mentioned above. Our results show that $Q_0(t)$ is not entirely determined by the material system as previously thought.

II. SAMPLES AND EXPERIMENTAL DETAILS

We have fabricated and measured $Q_0(t)$ on three different types of devices shown in Fig. 1. A single layer of poly-Si gates were patterned on top of a 37 nm thick SiO_2 gate oxide. The gate arrangement shown in Fig. 1(a), similar to Ref. 35 and 36, produces two individual SEDs: one in the upper half of the image with the dot underneath the enhancement gate labeled UEG and one in the lower half of the image with the dot underneath the enhancement gate labeled LEG. On another wafer, after fabricating single layer devices, a 20 nm thick isolation oxide was grown on the poly-Si gates, and then a full poly-Si top gate (Fig. 1(b)) or a half poly-Si top gate (Fig. 1(c)) was patterned on them. Between the two wafers we have three different types of SEDs: SEDs without isolation oxide or a top gate but with native oxide (Fig. 1(a)), SEDs with isolation oxide and a top gate (Fig. 1(b) and the upper half of Fig. 1(c)), and SEDs with an isolation oxide but no top gate (the lower half of Fig. 1(c)). We will refer to these devices as "bare", "TG", and "oxide", respectively. In total, we have measured two "bare" devices, three "TG" devices, and one "oxide" device (Table I). This total includes a single die as depicted in Fig. 1(c), where different types of SEDs lie within 200 nm of each other.

All devices discussed here were fabricated at National Institute of Standards and Technology (NIST) on 150 mm boron-doped silicon <100> wafers with a resistivity of (5 to 10) Ω·cm. The main fabrication process is as follows. The source/drain contacts (ULO, URO, LLO, LRO in Fig. 1(a)) are formed by phosphorus ion implantation. Then, a 125 nm field oxide is grown in a wet oxidation furnace at 900 °C, and etched away in the device window (a 175 μm square) using buffered oxide etch.[37] Subsequently, a high-quality 37 nm gate oxide is grown in a dry oxidation furnace with trichloroethane at 950 °C, which is immediately followed by deposition of a 75 nm in-situ doped N^+ poly-Si layer at 625 °C. The poly-Si gates are patterned by e-beam lithography using XR-1541 negative tone resist and a Cl_2-based dry etch. For "bare" devices, the next step is aluminum metallization to form contacts with a 425 °C forming gas anneal as the last step. For "oxide" or "TG" devices, the first layer of gate lithography and etching is followed by growth of a 20 nm isolation oxide on the poly-Si gates in a dry oxidation furnace at 850 °C, and a second deposition of in-situ doped N^+ poly-Si. Then the top gate layer is defined using the same e-beam lithography process as for the lower gates. The final step is aluminum metallization and the 425 °C forming gas anneal.

To measure the charge offset drift, a positive gate voltage is applied to the enhancement gate UEG (LEG) to accumulate electrons at the Si/SiO_2 interface, while other plunger gates are biased to define the quantum dot. The SED is tuned so that Coulomb blockade oscillations can be observed while sweeping either the enhancement gate or one of the plunger gates. We then repeatedly measure the same Coulomb blockade oscillation curve approximately every 15 minutes to track the changes in the local charge environment of the dot. $Q_0(t)$ is extracted from each trace using two different methods. At large source-drain bias (about half of the charging energy), the source-drain current I_d oscillates sinusoidally when sweeping gate voltage V_P, and each trace is fit to a sinusoidal function: $I_d(V_P) = A_0 + A\sin[2\pi(V_P/\Delta V_P + Q_0(t)/e)] + BV_P$, where A_0 is a current offset, A is the amplitude of the oscillations, ΔV_P is the period of the oscillations, and B is used to account for any slope in the sinusoidal curve. If the trace is not sinusoidal, a Gaussian function is used to find the peak location $V_{Peak}(t)$, and $Q_0(t) = -e(V_{Peak}(t) - V_{Peak}(t=0))/\Delta V_P$, where ΔV_P is the average voltage difference between the peak of interest and the two neighboring peaks. We have used both methods to analyze sinusoidal traces, and found that the results are consistent within 10 %, predominantly due to the uncertainty associated with ΔV_P. For some devices, we also attempted to assess noise using other measurement techniques such as a measurement of the low-frequency power spectral density. Unfortunately, this measurement was dominated by extrinsic, colored noise away from the frequency of the data presented here which hampered any interpretation. Measurements performed at NIST were taken at about 2.5 K in a closed-cycle cryostat. To exclude the possibility that the experimental setup contributes to the measured drift, NIST measurements were performed with two different sets of electronics (discussed in Sect. III). Additional devices were

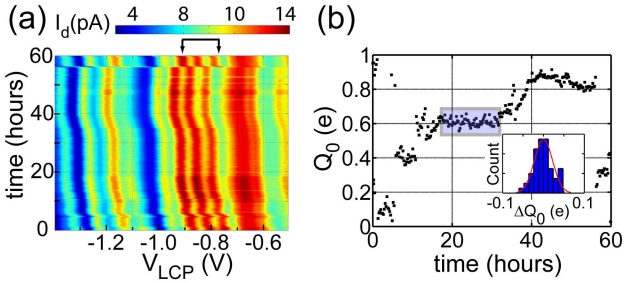

FIG. 2. $Q_0(t)$ for a "bare" device (4.7-41L). (a) Coulomb blockade oscillations taken with $V_{LEG} = 3\,\mathrm{V}$, $V_{LRP} = -1.8\,\mathrm{V}$, $V_{RIP} = -2.48\,\mathrm{V}$, all other gates at 0 V, DC bias $V_{d-DC} = -2.5\,\mathrm{mV}$ and AC bias $V_{d-AC} = 0.5\,\mathrm{mV}$, while sweeping V_{LCP} at T=2.5 K using the AC measurement system (see text). (b) Charge offset drift $Q_0(t)$ vs time, extracted from the Coulomb blockade oscillations using a sinusoidal function in the range indicated by arrows as shown in (a). The shaded area exhibits a stable period of $Q_0(t)$. The inset shows a representative histogram of the deviation of $Q_0(t)$ from the mean value.

also measured at California State University San Marcos (CSUSM) in another closed-cycle cryostat at about 2.5 K. The results (see Table I) from each set of measurements are qualitatively and quantitatively similar to those presented for the same device type.

The measured quantum dots are not necessarily intentional quantum dots. We select the bias conditions and the data fitting range so that the device operates as a stable single quantum dot device whenever possible. We confirm this through two-dimensional gate voltage sweeps and Coulomb diamonds.[38] When the oscillations are not periodic (see table 1 for Gaussian fits), this implies there is more than one dot involved in transport with a slightly different capacitive coupling to the swept gate. In these cases we track the position of a single peak. In all cases, Coulomb diamond sweeps give a charging energy for the dot of about 5 meV. As these quantum dots are used as local charge sensors of the environment, the detailed mechanism for the formation of the quantum dot is not expected to affect our conclusions.

III. RESULTS

Figure 2 shows a typical result for a "bare" (device 4.7-41L) using standard AC lock-in amplifier techniques. The charge offset drift $Q_0(t)$ has three distinct features, which were also observed in devices of the same design fabricated at Sandia National Labs.[36] First, over the course of the first two days, $Q_0(t)$ shows an evolution from rapid drift toward slower drift while winding $Q_0(t)$ through several e. This phenomenon has been previously referred to as transient relaxation.[29] (It should be noted that these single layer devices often become more stable at longer times.[36]) Second, the data show isolated discrete jumps or drifts, which are not stationary. Third, the device shows some stable periods where $Q_0(t)$ takes on a value within a stationary band. One such period is indicated by a shaded area in Fig. 2(b). We characterize local fluctuations about a stable mean with the standard deviation σ. We compute σ from the charge offset drift by first identifying regions of 50 points or more where a linear fit gives a slope of 0.01 e/day or less. For those devices with a linear trend in Q_0 (see Fig. 4), we first perform a linear fit to all of the data and subtract this dependence. We than calculate σ in the usual way within the identified stable regions and quote the average value in table I. While σ is useful in quantifying the differences between devices, it does not capture discrete jumps or long-term drift; all three metrics affect device integrability.

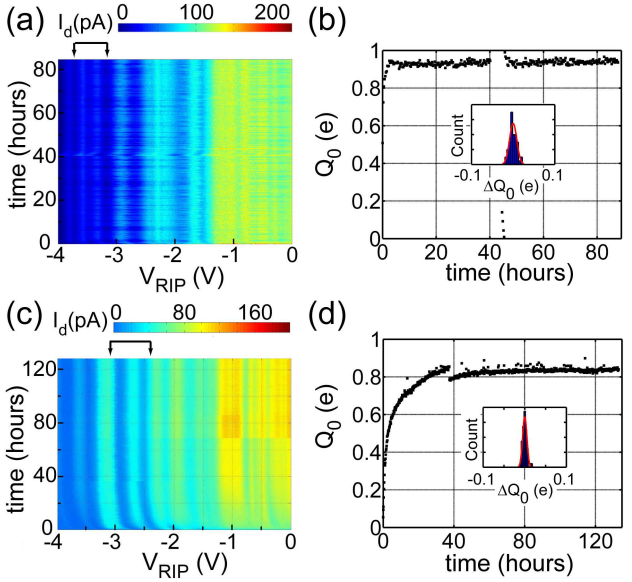

FIG. 3. $Q_0(t)$ for a "TG" device (5.4-25U) using the DC measurement system and the AC measurement system at NIST. Data taken (a) at $V_{UEG} = 1.42\,\mathrm{V}$, $V_{TG} = 0.2\,\mathrm{V}$, $V_{LIP} = V_{ULP} = V_{UCP} = V_{URP} = 0\,\mathrm{V}$, $V_{d-DC} = 3\,\mathrm{mV}$ using the DC measurement system and (c) at $V_{UEG} = 1.4\,\mathrm{V}$, $V_{TG} = 0.2\,\mathrm{V}$, $V_{LIP} = V_{UCP} = 0\,\mathrm{V}$, $V_{ULP} = V_{URP} = -0.9\,\mathrm{V}$ with $V_{d-DC} = 2\,\mathrm{mV}$ and $V_{d-AC} = 0.5\,\mathrm{mV}$ using the AC measurement system. Using sinusoidal functions in the ranges indicated by arrows, $Q_0(t)$ is extracted and shown in (b) and (d) respectively. The insets show representative histograms of the fluctuation ΔQ_0.

Figure 3 shows $Q_0(t)$ behavior measured in a "TG" device. There are four main differences from the data depicted in Fig. 2. First, while transient relaxation is still observed in the device with the top gate, $Q_0(t)$ winds through less than 1 e variation before becoming stable and, in the first cooldown data (Fig 3(b)), reaches a stable value in just a few hours. Second, after the transient evolution, $Q_0(t)$ essentially remains stable for the duration of the measurement in the device with the top gate. Third, $Q_0(t)$ in top-gated devices shows fewer and smaller discrete jumps. Fourth, the local fluctuations about the

stable mean value are reduced by more than a factor of two (to a level near or at the measurement resolution). All the devices of this type which we have measured show this behavior.

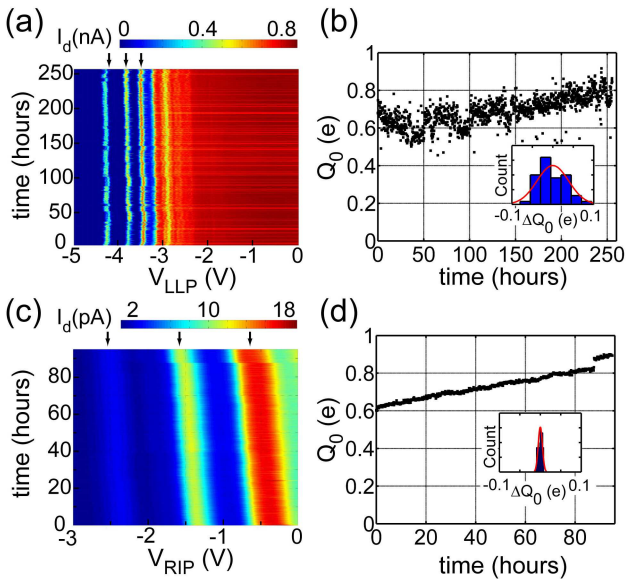

FIG. 4. Comparison of $Q_0(t)$ on neighboring "oxide" and "TG" devices. (a) Coulomb blockade oscillations for "oxide" SED 5.4-11L taken at $V_{LEG} = 5\,\mathrm{V}$, $V_{LIP} = -2.8\,\mathrm{V}$, all other gates at 0 V, $V_{d-DC} = 2\,\mathrm{mV}$ using the DC measurement system, and (c) for "TG" SED 5.4-11U at $V_{UEG} = 4\,\mathrm{V}$, $V_{TG} = 0.63\,\mathrm{V}$, all other gates at 0 V, $V_{d-DC} = 3\,\mathrm{mV}$ and $V_{d-AC} = 0.5\,\mathrm{mV}$ using the AC measurement system. (b) and (d) show the extracted $Q_0(t)$ using Gaussian functions. Arrows indicate the three peaks used in the fitting. The insets show representative histograms of the fluctuation ΔQ_0 after subtracting a linear-fit line.

Finally, in an effort to investigate the role of the isolation oxide, we also measured neighboring "oxide" and "TG" SEDs. This also enables a comparison of devices within 200 nm of each other in the same cooldown. Figure 4 shows the measurement results. Interestingly, transient relaxation is absent in both devices while a systematic (approximately linear) drift is observed instead indicating a non-stationary process. The origin of the linear drift is not clear and requires further investigation. Notwithstanding the linear drift, we again find a reduction in the frequency and amplitude of discrete jumps as well as fluctuations in the "TG" device. To facilitate a comparison of the fluctuations with the previous data we fit the data to a line and remove this dependence before plotting the histograms shown in the insets. The σ obtained this way shown in the "oxide" SED (device 5.4-11L) is about 9 times larger than that in the "TG" SED (device 5.4-11U). When assessed by this metric, the performance of the "oxide" device is the worst of those presented here even when compared to that of the "bare" device (see Fig. 2). This may be due to the dry etching process used to remove the top gate, leaving behind some charge defects in the oxide. When assessed by the long-term drift, the "oxide" device only shows small monotonic drift with few discrete jumps which is better than the "bare" device. In terms of both metrics, the "TG" device has the best performance.

A natural question when making these measurements is whether or not the measured drift is intrinsic to the device or from some extrinsic source in the measurement setup, especially since these measurements extend over days. To assess this question, measurements at NIST were performed with two separate sets of electronics and additional measurements were performed at CSUSM in a separate cryostat with a third set of electronics. The electronic systems at NIST are a DC measurement system using an Agilent 4156C precision semiconductor parameter analyzer, and an AC measurement system using standard lock-in amplifier techniques at 17 Hz. The DC measurement electronics return all electrodes to zero voltage between measurements of the Coulomb blockade curve while the AC electronics keeps a steady voltage on each electrode while returning the swept electrode to the beginning of the sweep between measurements. The measurement electronics at CSUSM keep every electrode at the voltage corresponding to the end of the measured voltage range between measurements. Both NIST systems record data as a sweep while the CSUSM system records data in voltage steps. No data is acquired in a backward sweep in any configuration. The NIST DC measurement protocol is chosen as it is the natural way to operate the parameter analyzer when performing sweeps and allows us to check if the sweep protocol affects $Q_0(t)$. A comparison of the NIST measurement electronics is made in Fig. 2 for an SED device with a top gate (device 5.4-25U). The DC system data are shown in Fig. 2(a)(b) and the AC system data are shown in Fig. 2(c)(d) as well as Table I. Although the DC data are noisier than the AC data, the extracted σ values are within the uncertainties. About a month passed between the DC measurements and the AC measurements. The longer transient relaxation time observed in the AC data is likely due to the intervening thermal cycle (which necessitated different applied voltages) rather than a difference induced by the different measurement protocols. It also seems unlikely that the CSUSM measurement protocol affected the measured results as the results for bare devices all have overlapping uncertainties.

IV. DISCUSSION

The data are summarized in Table I (additional data is shown in the Supplementary Material S3). In the context of the material-only explanation for $Q_0(t)$, all the devices listed should show similar drift; however, the data show that for Si/SiO_2-based SEDs, $Q_0(t)$ is influenced by factors other than the material system. We can characterize our empirical conclusions as follows: i) Long-term drift: "bare" devices (Fig. 2) show random

No top gate					
Device	Type	Isolation Oxide	Measurement	Fitting	σ of $Q_0(t)(e)$
4.7-41L	"bare"	No	NIST AC	Sine	0.023 ± 0.006
4.7-33U	"bare"	No	CSUSM DC	Gaussian	0.035 ± 0.008
5.4-11L	"oxide"	Yes	NIST DC	Gaussian	$0.05e \pm 0.01$

With top gate "TG"			
Device	Measurement	Fitting	σ of $Q_0(t)(e)$
5.4-23U	NIST DC	Sine	0.007 ± 0.002
5.4-25U	NIST DC	Sine	$0.010e \pm 0.002$
5.4-25U	NIST AC	Sine	$0.008e \pm 0.002$
5.4-11U	NIST AC	Gaussian	$0.005e \pm 0.001$

TABLE I. Summary of measured charge offset drift $Q_0(t)$. Devices with a top gate exhibit about a factor of two lower σ than those devices without a top gate. Uncertainty corresponds to a 95 % confidence interval and is estimated based on a χ^2 distribution of $N-1$ degrees of freedom where N corresponds to the number of data points. $\sigma = 0.01\,e$ (in the unit of the charge offset drift) corresponds to approximately 50 μeV (in the unit of the chemical potential variation at the quantum dot) with a charging energy of about 5 meV.

large-amplitude drift over the course of hours or days, similar to the Al/AlO_x system,[29,30] "oxide" (Fig. 4(b)) and "TG" (Figures 3 and 4(d)) devices show no drift or monotonic, predictable drift with fewer and smaller discrete jumps, similar to previous results in SOI devices;[32] ii) Local fluctuations, i.e. σ: "bare" and "oxide" devices show substantially larger σ than "TG" devices. Below we list possible mechanisms driving the difference in behavior shown in this manuscript.

There are clear electrical differences between the two types of devices. The top gate allows for the application of an electric field across the gate oxide in addition to the field resulting from the work function difference between the gate and the silicon. These fields could freeze defects out. The gate also acts as a ground plane which increases the total capacitance C_d of charge defects in the SED, and at the same time decreases the mutual capacitance C_m of defects coupled to the quantum dot. Considering a simplified case where one effective defect is coupled to the quantum dot, $Q_0(t) \approx (C_m/C_d)\Delta Q_d(t)$ (see the Supplementary Material S1), where $\Delta Q_d(t)$ is the variation of the defect charge. Both increasing the total capacitance of charge defects and decreasing the mutual capacitance to the quantum dot can reduce the charge offset drift $Q_0(t)$. To estimate the magnitude of the change in C_m and C_d (see the Supplementary Material S2), we have used FastCap to simulate "bare" and "TG" devices.[39] For charge defects located 90 nm away from the dot laterally and at the midpoint of the gate oxide thickness, the top gate reduces C_m by 55 % and increases C_d by 16 %. This reduces C_m/C_d by about a factor of two which gives the same order of magnitude as the observed reduction in σ. For defects located nearer to the Si/SiO_2 interface, the reduction in C_m/C_d is more muted, while it is more pronounced for defects near the SiO_2/gate interface. Similarly, for defects located nearer the quantum dot or other gates, the reduction in C_m/C_d due to the top gate is more muted. The detailed spatial distribution of defects will impact the size of the change in σ, however, these calculations show that the observed reduction of σ in $Q_0(t)$ can be accounted for by the electrostatic reduction in C_m and increase in C_d, with the change in C_m being dominant. Moreover, it is plausible that the lack of an exposed gate oxide surface for SOI devices and "TG" devices as compared to "bare" or "oxide" single-layer devices can effectively reduce the charge offset drift by reducing the number of defects near the gate oxide surface, where moisture or other ion defects may adsorb to the surface.

While our explanation that the additional gate modifies C_m and C_d to reduce σ is plausible, we cannot rule out a role for additional electrical differences between the devices at this time. First, the top poly-Si gate can act as a Faraday cage, which would shield the dot in the device from external electrical disturbance. The gate also necessarily implies additional strain in the device. Finally, though we have worked to minimize them, the gate cannot be introduced without some fabrication differences. These include second layer e-beam exposure, exposure to the dry etch process, and isolation oxide growth.

Whatever the reason for the reduction in $Q_0(t)$, these data indicate the interpretation of charge offset drift as only a material property is incomplete. We hasten to add, however, that the material stacks are still an important factor. In particular, as noted above, it appears that $Q_0(t)$ in "bare" devices (with a low-quality native oxide on the gates) have larger random drift and discrete jumps, similar to previous Al/AlO_x results,[29,30] whereas the devices with deliberate high-quality isolation oxide show monotonic, predictable drift with few or no discrete jumps similar to previous SOI results.[32] This may indicate that the native oxide, which can also pick up moisture from the surrounding air, has the same type of interacting defects that we have previously discussed.[29] In addition to the intrinsic TLS defects, the long-term drift in the native oxide could also be due to such mech-

anisms as the movement of dissolved hydroxyl ions from adsorbed moisture. Further experiments are necessary to confirm this suggestion. Moreover, experiments on atomically precise structures indicate that removing the dot from the Si/SiO_2 interface where traps are certain to be present leads to a reduction in the noise.[27]

Earlier work on $Al/AlO_x/Al$ based SEDs with a nano-Faraday cage did not show any improvement in the charge offset drift.[30] In fact, enclosing the device in additional AlO_x/Al increased ΔQ_0 by approximately a factor of two, in striking contrast to the results presented here. The likely reason is that unlike the AlO_x/Al stack, the SiO_2/poly-Si top gate does not introduce a significant number of new unstable charge defects, so that the benefit of adding the gate as outlined above (which should not otherwise differ between the two material systems) outweighs the negative effect from additional charge defects.

V. CONCLUSIONS

We have shown that introducing a poly-Si top gate can effectively reduce the level of the charge offset drift in Si/SiO_2-based single gate layer SEDs. This clearly demonstrates that the level of charge offset drift measured depends on factors other than simply the material systems used, and the device design plays an important role. Not only do these results provide researchers the opportunity to tune the level of stability performance in their devices, it provides an avenue toward further understanding the origin of noise in devices in various material systems.

SUPPLEMENTARY MATERIAL

See supplementary material for the equivalent circuit model to deduce the relationship $Q_0(t) \approx (C_m/C_d)\Delta Q_d(t)$, and the FastCap simulation. It also includes addition data not presented in the main text.

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DISCLAIMER

Certain commercial equipment, instruments and materials are identified in order to specify experimental procedures as completely as possible. In no case does such identification imply a recommendation or it imply that any of the materials, instruments or equipment identified are necessarily the best available for the purpose.

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