Measurement Tools for Substation Equipment: Testing the Interoperability of Protocols for Time Transfer and Communication

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***Abstract*— A test harness was designed and developed at the National Institute of Standards and Technology (NIST) to study the interoperability of the Precision Time Protocol (PTP) Power Profile and other communication standards for substation automation. Particular focus of the harness is on protocols that purport to comply by standards established by the Institute of Electronics and Electrical Engineering (IEEE) and the International Electrotechnical Commission (IEC). The test harness is intended for field evaluation of substation equipment and includes 3-phase electrical waveform generation capabilities, timing reference signal sources, measurement hardware for network clocks and software for monitoring and analyzing communication and time transfer protocols.**

The test harness was used at a Universal Communications Architecture International Users Group (UCAIug) Interoperability Plugfest (IOP) in 2017 where over 200 participants gathered to evaluate the interoperability between their products and tools.

Keywords—Precision Time Protocol, PTP Power Profile, Interoperability Testing

I. Introduction

As is the case with many distributed systems, the electric power system relies on assured timing and interoperability of communications. Integrated technologies in a ‘Smart Grid’ expect seamless and predictable data flow among a myriad of sensors and controllers which in turn places ambitious expectations on the ubiquitous knowledge of time. Clock synchronization requirements to Coordinated Universal Time (UTC) range from ±1 µs for synchrophasor measurements and ±100 ns for fault location in the transmission grid [1]. The UTC reference provides a traceable standard to compare timestamps between remote locations.

The IEC 61850 series of standards aim to address communication interoperability across substation automation equipment by specifying common protocols so devices may exchange information amongst each other. The standards also intend to assure system level performance within industry defined requirements by addressing time synchronization requirements between devices. In furtherance of this goal, the UCAIug organized an interoperability plugfest (IOP) where vendors of software tools, communication equipment and Intelligent Electronic Devices (IEDs) were able to physically connect their equipment to one another, exchange information, and meet application performance goals in order to verify the multi-vendor systems are in fact interoperable. IEDs are controllers with integrated microprocessors for onboard sensing and analysis to enable dynamic control optimization of power flows in the electric grid. Examples of IEDs include inverters, circuit breakers, relays, transformers, and capacitor banks.

One of NIST’s key roles, as a metrology institute within the Department of Commerce, is to aid in the development of test methodologies for advancing device and system interoperability and performance. The NIST Smart Grid Program, in turn, is focused on the needs of the power industry and consequently has been working on measuring the timing and other communication performance of networks and devices used in the power system. In alignment with the goals to cooperate with industry to improve upon the test methodologies and tools to support events for state of the art commercial technologies, NIST developed prototype hardware and software to support the IOP test event as a neutral, third party. The lessons learned from the test event will be applied towards improving NIST’s test and measurement tools and in the guidance NIST provides to the power industry as it evolves its standards and performance benchmarks.

This paper presents the design of the prototype test harness NIST developed for the UCAIug IOP test event. Both commercial- and NIST-designed and developed hardware and software were included in the test harness for online monitoring of time errors and conformity of PTP parameters. An offline analysis software tool was also developed for conformity to IEC 61850 Sampled Value (SV) messages.

II. Timing and Communication Interoperability Test

The IOP event comprised of several test areas including *Integrated Applications*, *Timing* and *Cybersecurity* [2]. NIST participated in the *Integrated Applications* and the *Time Synchronization* interoperability tests.

A. *Interoperability Testing Challenges*

Among the key aspects of interoperability testing is the capability to reliably and accurately assess the performance

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of given devices, from heterogeneous vendors, working in concert to satisfy requirements. The performance of the system as a whole must be assessed under operating conditions through functional tests, stress tests, and adversarial tests. To support this, the NIST Smart Grid team developed a portable test harness capable of assessing system interoperability within the NIST testbed as well as at interoperability test events and in the field. The tool suite is comprised of measurement and simulation capabilities with requisite signal emulation and distribution hardware to reliably reproduce reference signals (electrical signal waveforms, time signals). Measurements of interest include the clock offsets of system devices, protocol packet conformance, and network delay performance. The tool suite also includes a set of device configuration files to ensure repeatability and reproducibility of tests. This section provides the technical design and implementation details for each of the capabilities. Fig. 1 presents an overview of an interoperability test showing the test signals input to IEDs under test and corresponding measurand monitored by the NIST harness. The signal types and monitoring systems are designed to work with as wide a variety of substation automation devices (IEDs) as possible.

Fig. 1. Overview of an interoperability test where where test signals are applied to a set of IEDs and key ouptuts are measured.

The key interoperability testing challenges are accurate and simultaneous propagation of reference test signals, real-time execution of test scenarios, scale, and diversity of electronics with which to physically interface.

B. *Interoperability Test Harness*

The tool suite developed by NIST is illustrated with call out boxes in Fig. 2 showing where in the interoperability test they were used. For example, the NIST PTP dashboard application was used to monitor network timing (PTP) packets. The hardware and software test harness is comprised of both commercial-off-the-shelf test and measurement equipment and simulators as well as integration of NIST developed hardware and software components to enable a portable test harness for interoperability test events and field testing.

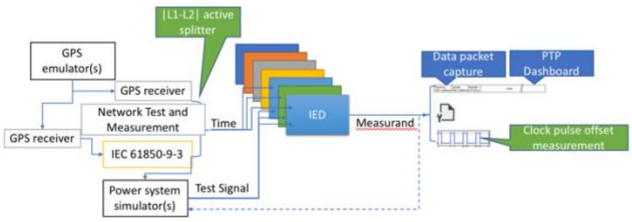

Fig. 2. Hardware and software tools comprising the NIST test harness for interoperability testing

III. Integrated Application Interoperability Testing

A. *Reference electrical waveform signals*

NIST provided simulated test signals for relays and merging units (MUs). Since the primary purpose of the plugfest was to evaluate the interoperability between substation equipment, a simulation was developed to provide reference signals to all the interacting devices to ensure neutrality and reproducibility. To this effect, a model of a substation circuit was executed on a real time digital simulator (RTDS), and emulated signals from the model were distributed to the participating IEDs. Nominally, this simulator produced pseudo-sinusoidal waveforms that recreated dynamic events that might be expected in a substation. Events like voltage and current transients that would trigger logic within relays and merging units were of interest to the plugfest organizers. Many of these events do occur in response to stimuli, for example in the case of switching transients following a tap change or a circuit breaker relay action. Recreating these closed-loop events required the use of a hardware-in-the-loop (HIL) simulator to produce the simulated signals. The real-time simulation was executed on an Opal-RT OP4510 Real-time Digital Simulator.

B. *Reference substation simulation*

Several test scenarios were developed in conjunction with participating engineers in the ‘Simulation Group’ of the IOP test event. The base case used for producing simulated test signals was a reference substation design provided by participating power system designers and power utilities.

The design was based on a 230 kV distribution substation and was modified to focus on differential protection, load tap changers, banked circuit breakers (load control) and voltage support components on each load transformer. The design was then instrumented with measurement devices (merging units (MUs)), differential protection (process bus relays), relay controllers, Load Tap Changers (LTCs) and Supervisory Control and Data Acquisition (SCADA) applications. The setup captured the base case of operation allowing repeated tests of substation operations and communication in an advanced substation measurement and control system comprised of devices from multiple vendors.

C. *Simulated dynamics*

A section of the substation called the ‘transformer bay’ was set aside as a ‘simulation island’. Essentially, it represented a section of a physical substation that featured control functions and software logic that push the performance envelope for substation equipment and system level operations. For example, the transformer bay featured a differential protection scheme that used merging units communicating directly to relays over an IEC 61850 process bus. This is a future capability that substation operators would like to see implemented but are limited by current deployments. During the IOP, the transformer bay was implemented as a simulation interacting with other bays in the substation.

Another high-performance substation application implemented as a simulation was that of a bus tie breaker. An electromagnetic transient simulation was used to capture the transient recovery voltage (TRV) of a full load transfer between two substation buses. TRV is the voltage transient that occurs across the terminals of a pole of a switching device upon interruption of the current. The TRV is a function of the Thevenin equivalent inductance in series with the breaker, where in our simulation the transformer inductance was the major source of the Thevenin equivalent inductance. When the fault current is interrupted by the circuit breaker, the source voltage supply will also supply current to stray capacitance in the breaker assembly to bring the capacitor voltage to the system voltage. TRV response timescale is in the order of a few tens of microseconds.

D. Hardware in the loop testing

The simulated transformer bay as well as the bus tie breaker generated voltage and current signals were connected to a physical MU hardware. Discrete switching actions were triggered when a Generic Object-Oriented Substation Event (GOOSE) message 'XCBR' was transmitted by a relay or a human operator. XCBR is a GOOSE logical node used to represent functions of physical devices and define objects and attributes for data exchange of information from circuit breakers. The alignment of switching command to the transient signals was achieved by locking the simulator to the timing infrastructure used by the MU and the circuit breaker controller/relay. This was achieved by instantiating client drivers for PTP messages (Fig. 3) and for GOOSE messages on the RTDS and synchronizing the digital to analog converter to a precise Global Positioning System (GPS) locked clock. The schematic diagram in Fig. 4 shows the HIL operation of the RTDS with several MUs all operating in lock step with a single time reference.

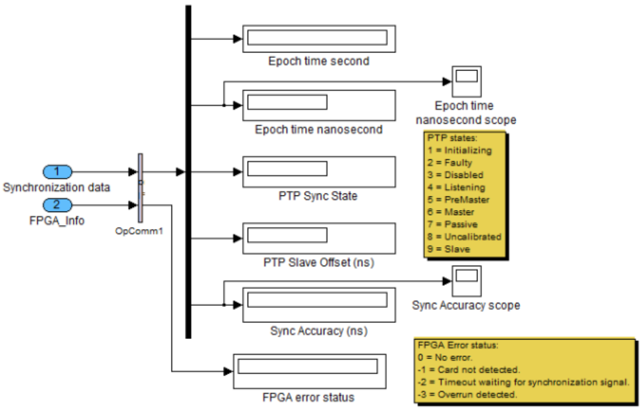

Fig. 3. PTP driver instantiation in the OP4510 showing timing performance variables evaluated during testing.

The test procedure required the evaluation of the tripping action comparing a simulated or virtual merging unit (VMU) against a physical MU. This is an interesting challenge since the differential phase measurement made by the relay is based purely on the SV messages from the MU, which means that the phase of the signals must be calibrated so as to be indistinguishable between the physical MU and the simulated VMU, including the test cases with transient events.

The signal generator (SigGen) connected to a real-time digital simulator system simulated a tap changing transformer subjected to varying loads. Measurements from the transformer primary and secondary windings were output as analog waveforms on Signal Channels B and A, respectively. In the base case, differential measurements between MU_1 and MU*_1 were used by the relay to trip a circuit breaker when appropriate. When MU*_1 was present, the VMU operated in calibration mode and measured the latency of the transduction process in MU*_1. Then VMU set its internal delay to match so that in the absence of MU*_1 the VMU could serve as a seamless replacement by simply disabling its "simulated" bit in the SV message. This simulation requires prior knowledge of the SigGen sequence, and precise synchronization between the two real-time digital simulators, which was achieved by transferring the clock from the SigGen simulator to the VMU simulator over a dedicated optical synchronization link.

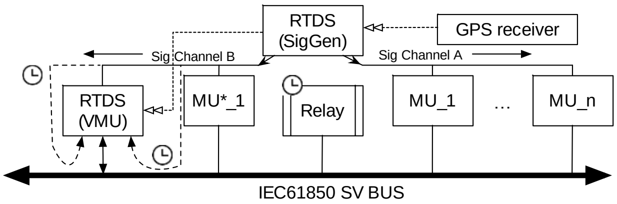

Fig. 4. Synchronization of multiple simulation systems.

E. Substation Automation Communications

Fig. 5 shows the interoperability test system for the IEC 61850-9-2[3] standard-based MUs. The system consists of a MU tester, two Devices Under Test (DUTs), a network switch, a network sniffer, and a MU interoperability analyzer. The MU tester is SVScout [4], a commercially available IEC 61850-9-2 testing tool that automatically identifies and subscribes to data streams from the DUTs. The network sniffer, Wireshark [5], is an open source network packet analyzer, which can capture network packets over an Ethernet interface. Wireshark was used in conjunction with the MU tester to capture all IEC 61850-9-2 packets from the DUTs and save them in the packet capture (PCAP) format. The IEC 61850-9-2 packets recorded by both SVScout and Wireshark were converted into Packet Detail Markup Language (PDML) format. The MU interoperability analyzer shown in Fig. 6 was developed at NIST to analyze PDML data logs and determine the degree of MU interoperability.

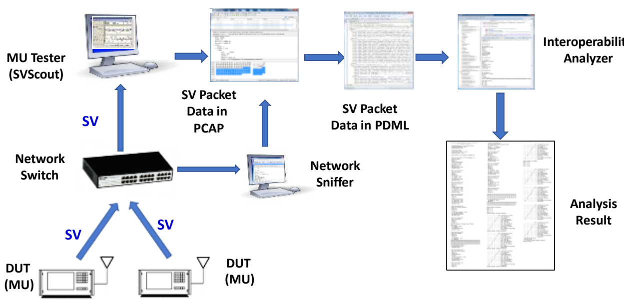

Fig. 5. Interoperability Test Method for IEC 61850-9-2 based MUs.

Packet data were captured for both real and simulated MUs present at the IOP test event. Interoperability assessments were performed offline on a subset of devices fom seven individual manufacturers [6].

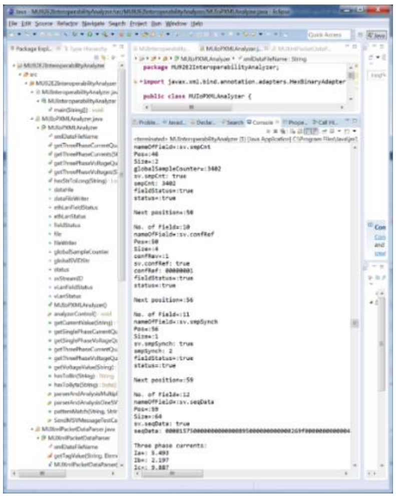

Fig. 6. A screenshot of the NIST MU interoperability analysis software.

IV. PTP Power Profile Interoperability Testing

A. GPS Reference Distribution

Time was distributed among the devices via multiple modes including a 10 MHz frequency source, a 1 Pulse Per Second (PPS) source, Inter-rage Instrumentation Group's, IRIG-B time code transmissions and PTP based network time. Some of the tests proposed by the timing subgroup of the plugfest also proposed manipulating the GPS signal to replicate time discontinuity or anomaly events such as the leap second and issues related to sporadic fading of the GPS signal strength due to cable or antenna malfunction. A GPS simulator, the Spectracom GSG-5 in conjunction with an 8-port GPS signal splitter, was used to produce and propagate GPS signals to the devices. The simulator includes a 1 PPS output calibrated to within 10 ns of the simulator's Radio Frequency (RF) output to serve as the reference in verifying the DUTs' time uncertainty.

Since the simulated signal would diverge from the baseline GPS signal being used by many devices on the floor, it was critical to not allow the simulated signal to leak into plugfest room. Once the simulator was installed and connected to a test device, a site survey was conducted using a micro strip antenna with low directivity connected to a GPS receiver with a C/N_0 display to ensure there was no signal interference in the room between the true GPS signal and the simulated one. In cases where we observed spurious leakage from connectors and amplifiers in line with the simulator, we applied adhesive shielding and attenuators to minimize radio leakage into free space.

As described in Section III-C with the differential line protection scenario, some test cases require the DUTs to take discrete actions at specified times while operating synchronously with each other. Ensuring sub-microsecond time alignment between devices required tight control over the relative phase offset between ports in the GPS signal splitter used. Following an observation of phase lag differences between ports of some commercial splitters and concern the power supply circuitry could introduce variability in the test results, NIST provided a splitter to the test event. The splitter used a phase matched impedance bridge to split the output of a MA11M Military Qualified Amplifier eight ways with a Channel Gain ≥ 14 dB. The amplifier was coupled to the 50 Ω impedance bridge ganged to express eight ports calibrated at L1(1575.42 MHz) and L2(1227.60 MHz) each with a standing wave ratio (SWR) ≤ 1.8, and phase matched to ≤ 1°.

The GPS receivers used by the devices being tested in the plugfest typically used an antenna with a low-noise amplifier (LNA) unique to their manufacturer. All receivers used DC power injectors of different specifications and used safety or line short logic to test the antenna wiring prior to start up. In order to ensure maximum compatibility, all the ports on the splitter were DC blocked with a blocking capacitor and a 200 Ω@0 Hz dummy load.

B. Phase offset measurement

In substation devices where sampled data are used to computationally derive state measurements, upcoming data quality standards require that samples be aligned and traceable to UTC. The clocks used to drive the sampling process in such cases are derived from a disciplined oscillator synchronized to a source of UTC time. GPS is the common source of this time reference for synchronization.

Most substation devices tested output a 1 Hz signal derived from the disciplined oscillator. This frequency product is output via a 1 Hz impulse train meeting CMOS or TTL interface specifications. The 1 PPS signal was used as a test signal to measure the device's alignment to the time reference. When the device is locked to a GPS receiver or to a network time server, it outputs a PPS signal where the rising edge is the DUT's top of the second. The time offsets between the rising edges from test devices, therefore, was used as a reliable measure for synchronization error and stability of time under fringe operation states. In order to simultaneously assess the synchronization performance of the system comprised of multiple end devices, NIST built a 1 PPS signal acquisition tool to measure the relative time error at 2 ns resolution to the time reference and edge detection with sub-nanosecond jitter measuring the offsets of up to 8 DUTs concurrently. The acquisition tool accepts 1 PPS outputs complying to different logic levels and impedances in order to ensure compatibility in testing multi-vendor networks. The tool can also self-calibrate the distance in order to handle different cable lengths of devices spread out across the testing facility.

Calibrating the cable lengths was essential as the variation in the electrical distance introduced delays exceeding 100 ns. Further, each device had different electrical interconnects requiring cables and connectors to be provided by the vendor in some cases. This diversity in cables and connection hardware further introduced variance between the measurements. To compensate for line delay, a time domain reflectometer (TDR) was designed on a National Instruments PXI-8196. Prior to start of a data capture event, an arbitrary waveform generator was triggered by a National Instruments PXI-6682 to produce a truncated exponential pulse injected into the cable system at the measurement end. The far end of the cable was left disconnected when the impedance of the PPS output from the measured device was unknown. The open end of the cable presented a high impedance to the incident pulse. The change in the characteristic impedance (impedance discontinuity) would cause some of the incident signal to be reflected back towards the source. The time delay of the reflected pulse was measured using the PXI-6682 and applied as correction to all future measurements. Clearly, time domain reflectometry requires good impedance matching at all the interfaces, impedance measurements were taken on the final test harness after fabrication at NIST to ensure minimal spurious reflections during the TDR calibration in the field.

The time offset test harness included a Tektronix MDO4104 logic analyzer controlled using NI LabView over a USB interface. The logic analyzer was setup to perform a time triggered capture and synchronized externally to a 10 MHz frequency reference derived from an Oven-Controlled Crystal Oscillator (OCXO) on the trigger source. Input impedances and voltage trigger threshold levels were configurable for each channel. The trigger source used software controlled direct digital synthesis to produce scan trigger in order to capture all rising edges within a 1 s window. Since multiple capture periods were potentially required to capture all the channels in the 1 s window, tight coordination was needed between the trigger process, the sampling process on the logic analyzer, and in the control software used to compile the data obtained. An OCXO reference clock was used for all the measurement hardware and software processes in order to ensure that there was no accrued timing error between subsystems.

To ease configuration and integrate the measurement, control and data acquisition systems, a user interface was developed as shown in Fig. 7.

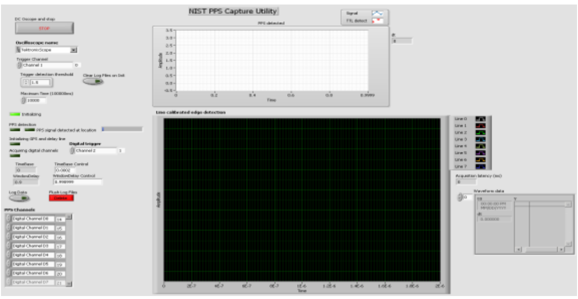

Fig. 7. The user interface for configuration and real-time monitoring of the time offset measurement utility for all the hardware components.

Fig. 8 provides 500 s interval of 8 DUTs' time offsets to give a view of a steady state baseline accuracy of the synchronized network. The stochastic variation between different clocks (inter-channel) and within the same clock (intra-channel) over the capture interval can be observed. Significant deviations from the baseline accuracy between the inter-channel variance and intra-channel variance serve as an indicator of malfunctioning clocks or malfunctioning network equipment.

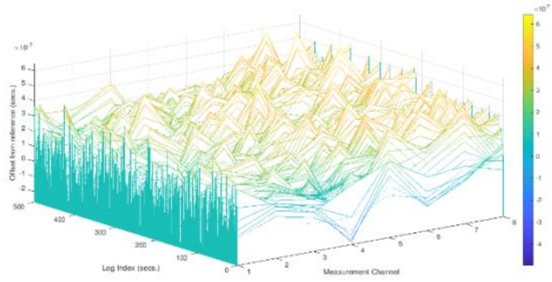

Fig. 8. Phase offset measurement of interoperability test devices.

Figure 9 provides a one minute trace of all eight channels. A 2nd order spline fit on the data for each channel describes the frequency variation between the devices. The interpolated spline fit provides visual illustration of the dynamics of synchronization within each clock even when the system is nominally at steady state. The variations in behavior are dependent on the clock quality and the PLL stabilization loop.

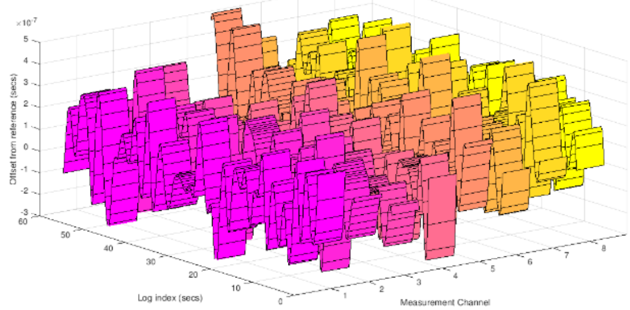

Fig. 9. Phase offset measurement of interoperability test devices.

C. PTP Dashboard

The design of the PTP Dashboard is based on the key application requirements for use in interoperability test events and field testing. To alleviate the need for manual configuration, a key requirement is device discovery. The second key requirement is real-time packet capture, processing and analysis.

The PTP Dashboard is a software application capable of self-discovery of PTP devices on a network and monitoring of PTP device conformance through observation of attributes and timeliness of attribute changes during Best Master Clock Algorithm (BMCA) selection, holdover, leap second insertion, and topology changes. The architecture of the software enables distributed monitoring and conformance testing within a local area network and devices at remote sites. The PTP Dashboard is a real-time web application using a combination of Python, Django and PostGresSQL to process PTP messages and visualize changes in the PTP parameters to ensure devices update the attributes within the required time intervals. The application can also display how these clocks are responding to timing events and configurations changes based on the test cases detailed by the Time Synchronization sub-group.

The application is capable of discovering PTP Grandmaster Clocks, Ordinary Clocks (OCs), Boundary Clocks (BCs) and Transparent Clocks (TCs) on the network. *Pyshark*, a network packet parser, enabled live captures of Announce, Sync, Follow_Up, Peer Delay Request and Peer Delay Response messages from the PTP network interface. Using the *Pyshark* library enabled rapid development of methods for verifying specific identifiers in each PTP message to determine whether it was an Announce Message, Peer Delay Request Message, Peer Delay Response Message, Sync Message, or a Follow Up Message.

Fig. 10 shows the components of the PTP Dashboard, which is comprised of the Django web application development framework, a network packet capture library, Pyshark, a PostGresSQL persistent data store, along with ReactJS to drive the front-end. The integration of Python based technologies enabled rapid prototyping of the conformance and interoperability test software. The application was designed, developed and tested within a 3-month period.

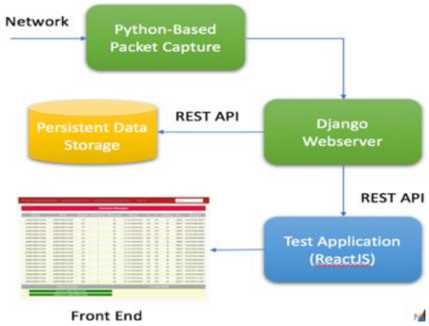

Fig. 10. PTP Dashboard architecture

Fig. 11. BMCA dataset comparison

By monitoring the PTP message attributes during the execution of the tests, such as a holdover or leap second event, the tool supports conformance testing of each PTP DUT to ensure the relevant attributes change in a timely manner. The application also monitors parameter changes of how multiple PTP clocks select a master clock based upon the BMCA as shown in Fig. 11.

V. Conclusion

We have described a test harness developed by the NIST Smart Grid Program for integrating substation communications, timing and measurement interoperability testing capabilities. One of the key improvements would be integration of the test and measurement devices used in the current system. For example, the dashboard can be extended to control the GPS simulator, network test equipment, and logic analyzer to provide a more streamlined test harness for field operations.

With the trend toward optical substations, the test harness would also need to support optical–based output signal testing including measurements of time error between clocks using 1 PPS, as well as PDV, PD of one-way PTP messages. Specific device firmware functionalities such as watchdog implementation, aspirations for bug-free code such that the system never requires a power cycle are all desired functionalities but require more sophisticated software assurance testing.

Support of additional performance metrics include:

- PDV as a function of network traffic saturation to improve testing of the network nodes.
- Software assurance metrics to determine system robustness to security or disruptive networks.
- Resiliency metrics, such as duration of link loss, time interval for link recovery, and continuous hardware-based time error monitoring during the link loss and link recovery events to capture results of redundancy testing.

Through the IOP participation, and development of the test tools presented here, NIST received valuable feedback that will be incorporated into the design of its Smart Grid Testbed. The NIST Smart Grid Testbed is intended to develop and validate prototype measurement and test tools to support industry interoperability and standards development. The key areas of the testbed include wide area sensing (PMUs, MUs, Wire Monitoring Sensors, Smart Meters) and control (relays, current and voltage transformers) which require a base information infrastructure for timing, communications, and cybersecurity to support the dynamic and critical nature of power systems. The development of the tool suite also sets the foundation for the testbed and Smart Grid program to continue to support industry standards development as well as test and certification efforts for the IEEE/IEC 61850-9-3 (2016) and IEEE C37.238-2017 PTP Power Profiles and IEC 61850-9-2 communication standards.

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References

[1] Time synchronization in Electric Power Systems. *NASPI Technical Report*, March 2017. https://www.naspi.org/sites/default/files/reference_documents/tstf_electric_power_system_report_pnnl_26331_march_2017_0.pdf.

[2] IEC 61850 IOP Use Cases and Test Cases for IEEE 1588 using IEC/IEEE 61850-9-3:2016 and IEEE C37.238:2017. http://iec61850.ucaiug.org/2017IOP-NOrleans/IOP%20Documents/TimeSync_Subgroup/2017_Test_Cases/IOP%20PTP%20Test%20Cases%20for%209-3%20and%2037.238_V1.0.docx, *(Accessed April 2018)*.

[3] IEC 61850-9-2:2011, Communication networks and systems in substations – Part 9-2: Specific Communication Service Mapping

(SCSM) – Sampled values over ISO/IEC 8802-3. Available online at: https://webstore.iec.ch/publication/6023.

[4] SVScout. https://www.omicronenergy.com/en/products/svscout/.

[5] Wireshark. Available online, https://www.wireshark.org/.

[6] UCAIUG IEC 61850 IOP 2018 Report, April 2018.

[7] IEC/IEEE International Standard - Communication networks and systems for power utility automation Part 9-3: Precision time protocol profile for power utility automation," in *IEC/IEEE 61850-9-3 Edition 1.0 2016-05* , vol., no., pp.1-18, May 31 2016.

[8] IEEE Standard Profile for Use of IEEE 1588 Precision Time Protocol in Power System Applications," in *IEEE Std C37.238-2017 (Revision of IEEE Std C37.238-2011)* , vol., no., pp.1-42, June 19 2017.

[9] IEEE Draft Standard Requirements for Time Tags Created by Intelligent Electronic Devices - COMTAG(TM)," in *IEEE PC37.237/D0.8, April 2018* , vol., no., pp.1-56, Jan. 1 2018.