Optimal Series Resistors for On-Wafer Calibrations

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***Abstract*—The series resistor is a common on-wafer device typically used in the series-resistor calibration and for estimating the capacitance per unit length of coplanar waveguide transmission lines. While much work has been done using series resistors, this paper addresses the design of the resistor itself, considering both its dc resistance value and geometry, and evaluates which resistor is the best resistor. We fabricated 48 different series resistors with dc resistances ranging from approximately 1 Ω to over 6 kΩ and tested their utility in the series-resistor calibration and in extracting the capacitance per unit length of coplanar waveguide transmission lines. We found that a dc resistance near 100 Ω produces the best series-resistor calibration when compared to multiline thru-reflect-line. For extracting the capacitance per unit length, resistors with a dc resistance near 150 Ω and shorter than 20 µm long gave the capacitance values with the lowest uncertainty. Additionally, we provide some guidance on choosing frequency bounds for the capacitance estimation. These results are of interest to anyone who performs on-wafer calibrations.**

***Index Terms*—Calibration, capacitance, microwave, on-wafer, scattering parameters, series resistor**

I. Introduction

SCATTERING parameter (S-parameter) calibrations are a cornerstone in microwave metrology. Accurate calibrations help circuit designers validate new components for high-frequency electronics and wireless communications. Typically, we measure the complex S-parameters of a device-under-test (DUT) with a vector network analyzer (VNA). However, raw S-parameters are generally of little value and must be corrected with an error model [1]–[3]. This correction is required at microwave frequencies because the wavelength of the microwave signals is often on the same or smaller length scale as the cables, connectors, and probes used to interface with a DUT. Calibrations correct for these effects, translating the reference planes of the measurement to the DUT and ensuring an accurate measurement of a device's true response or performance despite the less-than-perfect VNAs we use to characterize them.

There are a variety of commonly-used on-wafer calibrations, including the thru-reflect-line (TRL) [4], the multiline thru-reflect-line (mTRL) [5], [6], the short-open-load-thru (SOLT) [7], [8], the short-open-load-reciprocal (SOLR) [9], [10], the line-reflect-match (LRM) [11], [12], the line-reflect-reflect-match (LRRM) [12], [13], the line-reflect-line (LRL) [14], and the series resistor [15]–[17] calibrations. Many of these calibrations share a reliance on lumped-element approximations for some of their constituent standards. Unlike its counterparts, mTRL depends on distributed circuit models and measures the traveling-wave solutions to Maxwell's equations directly, making it more accurate. This accuracy makes mTRL an ideal choice for benchmarking new calibration algorithms [5], [16], [18]. Indeed, the parasitics in lumped element models are often characterized with mTRL calibrations [16], [17]. In such cases, benchmarking against lumped element models is redundant with a benchmark against mTRL. However, even for mTRL calibrations on low-loss substrates with negligible dielectric dispersion, one must provide an estimate for the capacitance per unit length of the transmission line standards to set the reference impedance.

There are several approaches to estimate the transmission line capacitance per unit length on low-loss substrates. These approaches include measurements of shunt resistors [19], measurements of the per-unit-length resistance of transmission lines [19], direct measurement of transmission line capacitance [19], conformal mapping [20], finite-element simulations [21], and measurements of series resistors [16]. Both conformal mapping and finite-element simulations require detailed information about the transmission lines, including the dimensions, conductivities, electrical permittivities, and magnetic permeabilities of all constituent materials that comprise the transmission line. Simulations also typically require validation through comparison to measurements. It is therefore critical to have accurate measurement-based estimates of the transmission line capacitance. Unlike conformal mapping

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and finite-element simulations, transmission line capacitance extraction from a shunt or series resistor only requires dc measurements, S-parameter measurements, and the assumption that the resistor is accurately described by a lumped-element model. While previous work focused on fabrication and circuit models of some shunt resistors [22], there are several outstanding questions for series-resistor design. Specifically, this paper addresses which dc resistances and resistor geometries are optimal for estimating the capacitance per unit length, and for providing the highest-accuracy series-resistor calibration when compared to mTRL.

The series-resistor calibration has several advantages that make it an attractive option for on-wafer calibrations. First, since it is based on a lumped-element model, it is well-conditioned at lower frequencies. In contrast, mTRL is increasingly ill-conditioned as the phase shift between the longest and the shortest line drops below a quarter wavelength. Second, the series-resistor calibration only requires three standards (a short-circuit reflect, a thru, and a series resistor). The small number of standards consumes much less space on a chip than mTRL calibration standards, making it a good candidate when on-wafer area is limited. The series-resistor standard also contains only a single resistive element, as opposed to the two different elements for shunt resistors. This eliminates the possibility that the shunt resistors on port 1 and port 2 are slightly different, as may be the case in SOLT calibrations. We note that for planar geometries, this slight difference between the resistors on port 1 and port 2 may be smaller than for vertically integrated resistors that employ vias. In either the planar or vertically integrated case, the shunt resistors have the potential to be different, which can affect the accuracy of a calibration especially at high frequency as parasitics increase. Finally, series-resistor calibration standards are stable both over time and over a wide temperature range [15], [16].

The resistors used in previously published work had a resistance value of 56.69 Ω, and were 10 µm long and 10 µm wide [16], or had a resistance value of 223.7 Ω, and were 128 µm long and 64 µm wide [15]. Shunt resistors used in SOLT calibrations are typically close to 50 Ω. In this work, our objective was to test whether the previously employed resistor values and dimensions were the best values to use for extracting the capacitance per unit length and in the series-resistor calibration itself.

In the following sections, we begin with a discussion of the design, fabrication, and measurement of our devices (Section II). Next, we describe the estimation of the capacitance per unit length for mTRL calibrations (Section III) and compare the various series resistors in the context of the series-resistor calibration (Section IV). We show the results of finite-element simulations of the series-resistor devices (Section V), discuss potential future directions (Section VI), and conclude (Section VII). For the interested reader, we also offer an appendix with a full uncertainty budget for the extracted capacitance per unit length for both a typical series resistor (~50 Ω) and the best series resistor in the data set.

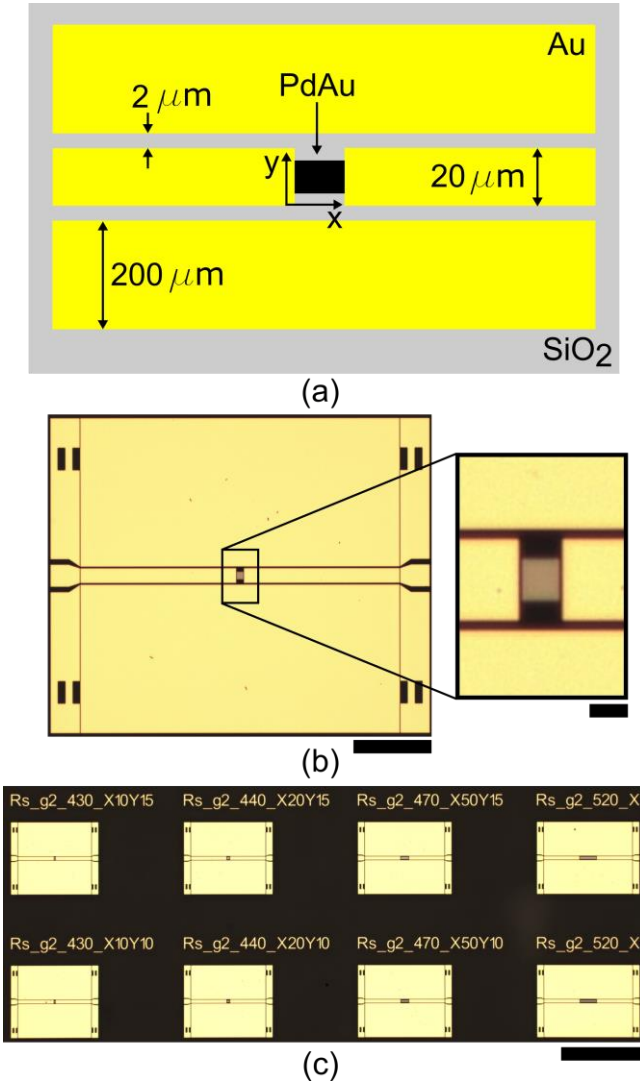

Fig. 1. (a) Top-view schematic representation of a series resistor device showing nominal device dimensions. Resistor lengths are in the x-direction and widths are in the y-direction. (b) Photograph of a series-resistor device. Scale bar is 100 µm. Scale bar for magnified region is 10 µm. (c) Photograph of a few series-resistor devices showing varying resistor geometries. Scale bar is 500 µm.

II. Methods

A. Fabrication

To test which resistor yields the best results in extracting the capacitance and for the series-resistor calibration, we fabricated 48 different resistors integrated into coplanar waveguide (CPW) transmission lines along with a complementary set of mTRL calibration artifacts. We note that while we chose materials that were readily available in our internal clean room, the techniques developed here are not strictly limited to the

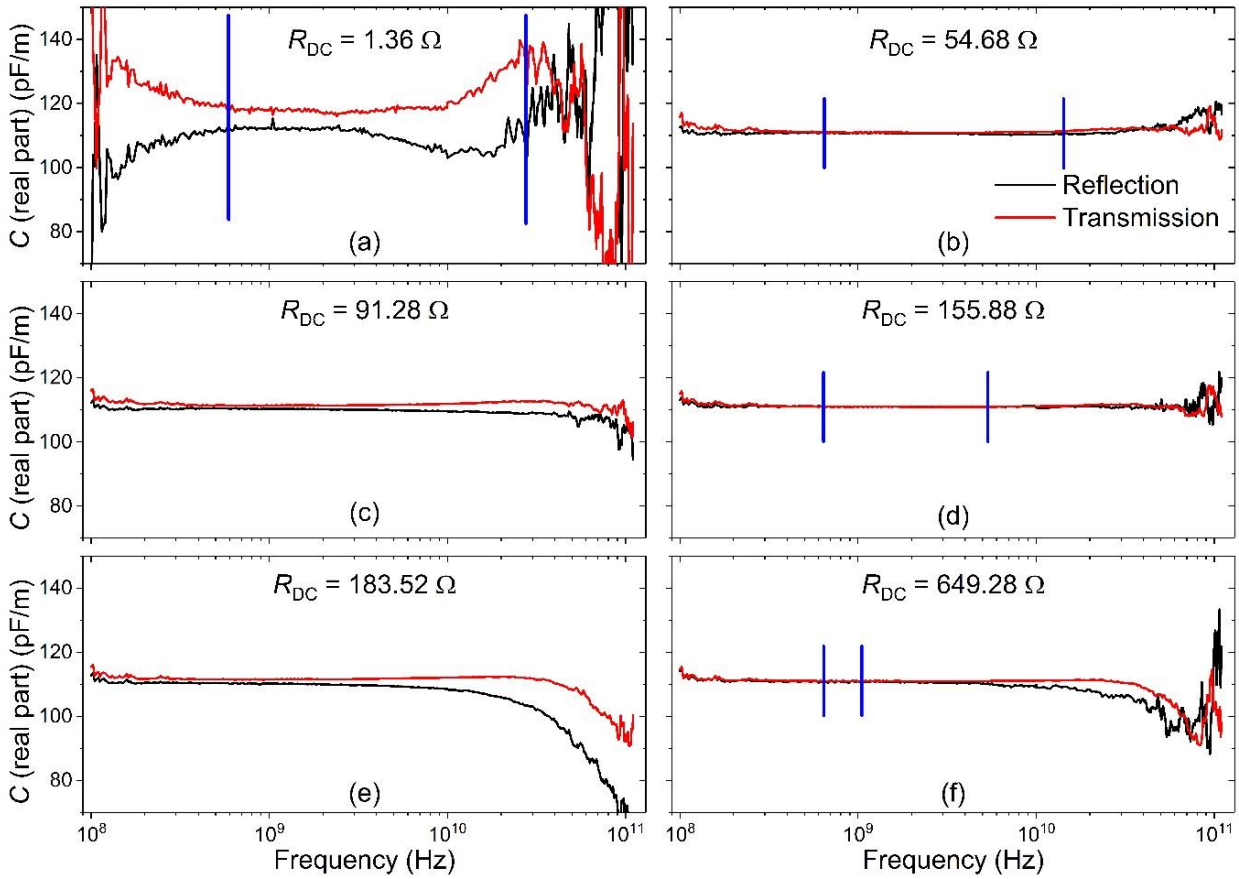

Fig. 2. Real part of capacitance per unit length (C) vs. frequency for a representative set of series resistors showing C approximated from transmission (red) and reflection (black) S-parameters. The blue vertical lines indicate the frequency window defined by our proposed criteria for extracting C_0. Panels (c) and (e) have no blue bars because these resistors had no acceptable frequency window.

conductor, resistor, and dielectric materials that we chose, but are broadly applicable to on-wafer calibrations that require the accuracy, precision, and traceability of multiline TRL.

We fabricated the devices on a (500 ± 25) µm-thick fused silica substrate. Fused silica has a relatively low dielectric constant, negligible dispersion, and a low loss tangent, making it an excellent choice for on-wafer calibrations. Given our choice of fused silica, it is possible that our conclusions may not generalize to Si-CMOS or III-V substrates. However, one can follow our procedure to optimize the series-resistor design for other low-loss substrates.

For fabrication of the resistor element, we coated the substrate with a lift-off photoresist and an imaging photoresist, exposed it with i-line stepper photolithography, and developed the photoresist. We then electron-beam evaporated a (2 ± 1) nm Ti adhesion layer and a (12.5 ± 1) nm layer of $Pd_{53}Au_{47}$ without breaking vacuum. This thickness of $Pd_{53}Au_{47}$ has a sheet resistance of approximately 50 Ω/□, which is a common sheet resistance in commercial foundry processes. The PdAu deposition rate was approximately 0.3 nm/s and was automatically controlled with a commercial quartz crystal monitor deposition controller. The base pressure of the deposition chamber was approximately 6.7×10^{-6} Pa. After depositing the PdAu, we performed a lift-off step, forming the resistor layer. We then repeated this process with a 10 nm layer of Ti and a 500 nm layer of Au to define the CPW structures. We note that the choice of Au in lieu of Cu or some other conductor only affects the distributed circuit parameters of the transmission lines that lead up to the series resistor. Replacing the Au with Cu should not alter the conclusions of our manuscript. The CPW designs had a 20 µm-wide center conductor, a 2 µm-wide gap between the center conductor and ground plane, and 200 µm-wide ground planes. The mTRL standards included eight CPW transmission lines with lengths of 0.420 mm, 0.670 mm, 1.010 mm, 1.580 mm, 2.450 mm, 4.000 mm, 6.210 mm, and 9.620 mm, as well as a short-circuit reflect with 0.210 mm-long transmission lines on each port, symmetric about the termination. All transmission line lengths had an uncertainty of 0.25 µm, but the dominant uncertainty mechanism was the wafer-probe landing position, approximately 4 µm.

A schematic of a representative series-resistor device is

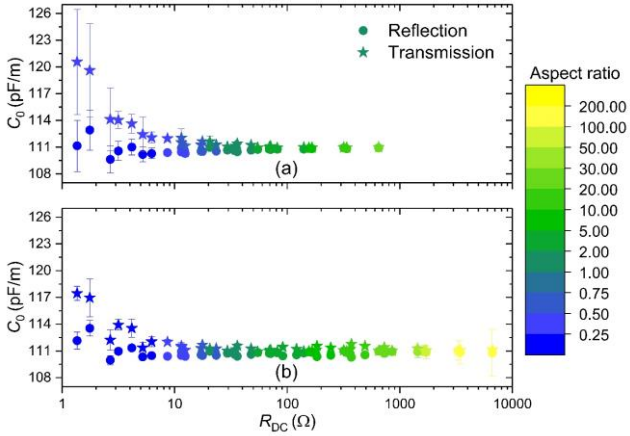

Fig. 3. C_0 vs. R_{DC} found using (a) our proposed frequency window criteria and (b) manual frequency bounds. The aspect ratio is the length of a resistor divided its width. The error bars represent the standard deviation of C across the frequency bounds. Aspect ratio is resistor length/width.

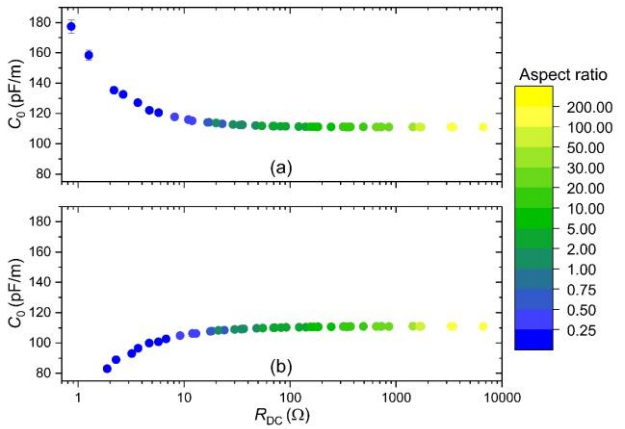

Fig. 4. C_0 vs. R_{DC} using manual frequency bounds for R_{DC} artificially adjusted by (a) -0.5 Ω and (b) +0.5 Ω. Aspect ratio is resistor length/width.

shown in Fig. 1(a). Transmission lines of length 0.210 mm connect each port to series-resistor structures of varying sizes. We fabricated resistors with lengths (x-direction) of 1 µm, 2 µm, 5 µm, 10 µm, 20 µm, 50 µm, 100 µm, and 200 µm and widths (y-direction) of 1 µm, 2 µm, 5 µm, 10 µm, 15 µm, and 20 µm in an array for a total of 48 different resistors. The uncertainty in the resistor dimensions was 0.25 µm. The dc resistances (R_{DC}) ranged from 1.36 Ω to 6641.09 Ω, after subtracting the resistance of the 0.420 mm thru to compensate for the transmission line leads on the resistors. The uncertainty of all the R_{DC} values reported throughout this manuscript is discussed in Appendix A and is ± 0.06 Ω. A close-up picture of one of the devices is shown in Fig. 1(b) and a picture of several of the series resistors is shown in Fig. 1(c).

B. *Measurements*

The R_{DC} values and complex, frequency-dependent S-parameters of all devices were evaluated with devices mounted on a temperature-controlled stage set to (25 ± 2) °C. We measured the S-parameters using a VNA, from 100 MHz to 110 GHz with 402 frequency points on a logarithmic spacing. The VNA had an intermediate-frequency bandwidth of 50 Hz and a source power of -20 dBm. The on-wafer probes had a 50 µm pitch. To ensure the best probe landing repeatability, we used a semi-automated probe station for the measurements and each device had alignment marks. First we measured a set of mTRL calibration standards, next we measured each of the series-resistor devices, and finally we repeated the measurements of the mTRL calibration standards. The reference planes for all series-resistor measurements were at the boundary between the PdAu resistive element and Au center conductor in the CPW structure.

III. Extracting the Capacitance Per Unit Length

A. *Theory*

Our typical algorithm for correcting on-wafer measurements begins with a mTRL calibration to correct the measurements to the (unknown) characteristic impedance $Z_0(\omega)$ of the transmission lines and to find the propagation constant $\gamma(\omega)$. The propagation constant is given by $\gamma(\omega) = \sqrt{(R(\omega)+i\omega L(\omega))(G(\omega)+i\omega C(\omega))}$ and the characteristic impedance is $Z_0(\omega) = \sqrt{\frac{R(\omega)+i\omega L(\omega)}{G(\omega)+i\omega C(\omega)}}$, where R is the resistance per unit length, L is the inductance per unit length, G is the conductance per unit length, and C is the capacitance per unit length of the transmission lines.

The next step in our typical algorithm is to estimate $Z_0(\omega)$ and transform the reference impedance from $Z_0(\omega)$ to 50 Ω. Given the low dispersion and loss tangent of the substrate, we make the approximations that the capacitance is constant across frequencies and that the substrate is lossless (i.e. $C(\omega) = C_0$ and $G = 0$ S/m). Given these approximations, we estimate $Z_0(\omega)$ from $\gamma(\omega)$ and C_0 as $Z_0(\omega) = \gamma(\omega)/i\omega C_0$. Thus, we require an estimate of C_0 in order to impedance transform the error correction matrices (error boxes) to a reference impedance of 50 Ω [16].

We estimate C_0 by combining S-parameters measurements of a series resistor with the propagation constant obtained from the mTRL algorithm. The S-parameters for a series load Z_L are given by [16]

$$S = \frac{1}{1+\frac{Z_L}{2Z_0(\omega)}}\begin{pmatrix} \frac{Z_L}{2Z_0(\omega)} & 1 \\ 1 & \frac{Z_L}{2Z_0(\omega)} \end{pmatrix}. \quad (1)$$

If we assume that the series load impedance Z_L is real and

equal to R_{DC} and that G = 0 S/m, we can solve (1) for $C(\omega)$ [16]

$$C_{11,22} \approx \left(\frac{2\gamma(\omega)}{i\omega R_{DC}}\right)\frac{S_{11,22}}{1-S_{11,22}} \quad (2)$$

$$C_{12,21} \approx \left(\frac{2\gamma(\omega)}{i\omega R_{DC}}\right)\frac{1-S_{12,21}}{S_{12,21}} \quad (3)$$

where $\gamma(\omega)$ is the propagation constant, S_{ij} are the scattering parameters, $\omega = 2\pi f$ is the angular frequency, and R_{DC} is the measured dc resistance. C_{ij} is the capacitance extracted from the ij^{th} S-parameter (S_{ij}). To find the value for C_0, authors have previously used a criterion where they took the median of the real part of C values below 1 GHz [16]. While this approach avoids high-frequency parasitics, it also gives increased weight to low frequencies, where TRL may not be well conditioned. Based on our observations in this work, we propose a new procedure for determining the frequency bounds to find the constant value of C_0. To avoid ill-conditioned mTRL measurements, we choose the low frequency bound to be where the magnitude of the normalized standard deviation $\sigma(\omega)$ [5] is less than 2, which, in our case, is the average of σ_α and σ_β, where

$$\sigma_{\alpha.\beta} = \frac{1}{\sqrt{\sum_{ij}(V^{\alpha,\beta})_{ij}^{-1}}} \quad (4)$$

and the $\left(V^{\alpha,\beta}\right)_{ij}^{-1}$ denotes the inverse of $V_{ij}^{\alpha,\beta}$, and

$$V_{ij}^{\alpha} = \frac{E_1^{1i*}E_1^{1j}+\delta_{ij}^K\left|E_2^{1i}\right|^2+(1+\delta_{ij}^K)\left|E_1^1\right|^2E_1^{i*}E_1^j}{\left(E_2^{1i}-E_1^{1i}\right)^*\left(E_2^{1j}-E_1^{1j}\right)} \quad (5)$$

$$V_{ij}^{\beta} = \frac{E_2^{1i*}E_2^{1j}+\delta_{ij}^K\left|E_1^{1i}\right|^2+(1+\delta_{ij}^K)\left|E_2^1\right|^2E_2^{i*}E_2^j}{\left(E_2^{1i}-E_1^{1i}\right)^*\left(E_2^{1j}-E_1^{1j}\right)} \quad (6)$$

are the covariance matrices. Additionally,

$$E_1^{ij} = e^{-\gamma(l_j-l_i)} \quad (7)$$

$$E_2^{ij} = e^{+\gamma(l_j-l_i)} \quad (8)$$

$$E_1^{i} = e^{-\gamma l_i} \quad (9)$$

$$E_2^{i} = e^{+\gamma l_i} \quad (10)$$

where l_1 is the length of the thru, i and j index the line lengths l_i used in the mTRL calibration excluding the thru, Σ_{ij} indicates a sum over the line pairs, δ_{ij}^K is the Kronecker delta, * denotes the complex conjugate, and γ is the propagation constant. In general, the index 1 denotes the common line and which line this is should be chosen and optimized at each frequency. Because here we are interested only in the low frequency behavior for a low frequency capacitance cutoff, we choose index 1 to denote only the shortest line, or the thru, because it gives the best performance at low frequency.

This normalized standard deviation is computed only from the propagation constant, the frequency range, and the line lengths in mTRL and is a measure of how well mTRL works as a function of frequency. In general, a higher normalized standard deviation results in a poorer calibration. For comparison, an LRL calibration with lossless lines would have a normalized standard deviation of 1 when the transmission phase is π/2 rad and a normalized standard deviation of 2 when the transmission phase difference between the lines is $\frac{\pi}{6}$ rad or $\frac{5\pi}{6}$ rad. This is a slightly more conservative phase window than the common recommendation that one should limit the use of a line pair so that the phase difference is between $\frac{\pi}{9}$ rad and $\frac{8\pi}{9}$ rad [5]. For the devices considered here, a threshold value of 2 for the normalized standard uncertainty yielded a low frequency cutoff of approximately (631 ± 15) MHz.

We constructed a high-frequency condition on the physical length of the series resistor by imposing the phase condition

$$\frac{\beta\ell}{\pi} < \frac{1}{3000} \quad (11)$$

where β is the imaginary part of the propagation constant and ℓ is the length of the resistor. This condition rejects frequencies where there is a non-negligible phase shift along the resistor, assuming the propagation constant in the resistor region is unperturbed by the resistor's electrical properties and dimensions. The uncertainty in the phase of the transmission for a typical network analyzer is approximately 0.03 degrees around 1 GHz [23]. If we assume that non-negligible phase must be at least twice the uncertainty, then a resistor exhibiting non-ideal behavior would have approximately 0.06 degrees of phase shift in transmission. Converting this value into radians and dividing by pi yields a value of 1/3000. Modeling such a phase shift would require a series-resistor model that either includes parasitic lumped elements or distributed effects, neither of which are accounted for in (2) and (3). Interestingly, this phase condition excludes any resistors longer than 28 µm for our parametric study up to 110 GHz, which we found to be a good criterion for selecting a resistor to use to extract the correct value for C_0 with low uncertainty. As we discuss later, we validated the phase condition by examining the lumped-element model of the series resistor and noting where the parasitic inductance due to the length of the resistors becomes significant (see Section IV and Appendix B).

To be clear and concise throughout the rest of the manuscript, we will refer to the capacitance per unit length vs. frequency (f) computed from the resistor S-parameters as C and to the constant (frequency-independent) value estimated from these data as C_0. We found C_0 by taking the average value of the real part of C across the frequency bounds of all four S-parameters.

TABLE I
PARAMETERS OF THE BEST RESISTORS IN OUR DATA SET FOR EXTRACTING C_0

R_{DC} (Ω)	C_0 (pF/m)	Standard deviation of C (pF/m)	Length, x-direction (μm)	Width, y-direction (μm)	Aspect ratio (length/width)
140.28	110.88	0.15	20	5	4
155.88	110.88	0.15	5	1	5
165.84	110.88	0.13	10	2	5

We expect that selecting an optimal frequency range for the measurement of C ultimately reduces the uncertainty in the estimate of C_0 by rejecting noisy measurements due to ill-conditioned TRL calibrations at low frequencies or systematic errors due to parasitics at high frequencies.

B. *Step-by-Step Procedure for Estimating C_0*

1) Measure the switch terms [2] and uncorrected S-parameters of the mTRL standards.
2) Measure R_{DC} and S-parameters for all series-resistor devices.
3) Perform a mTRL calibration to get the propagation constant $\gamma(\omega)$ and error boxes corrected to the unknown characteristic impedance Z_0.
4) Correct the S-parameters of the series resistors with the mTRL error boxes.
5) Use (2) and (3) to estimate $C(\omega)$.
6) Apply frequency bounds and average the real part of $C(\omega)$ within the bounds to get C_0.

C. *Results for Estimating Capacitance Per Unit Length*

Fig. 2 shows a selection of C vs. f plots for different series resistors. The frequency range defined by our criteria that was used to extract a value of C_0 is indicated by the blue lines. Fig. 2(a) shows C vs. f for the resistor with the lowest R_{DC} value measured, 1.36 Ω. The resulting C vs. f data for this 1.36 Ω resistor appear noisy, and the transmission and reflection values do not agree, making it a poor choice for a series-resistor artifact. Fig. 2(b) shows the C for a "traditional" series resistor, whose resistance is close to 50 Ω. This 50 Ω resistor is 2 μm long and is a reasonable choice for a resistor to extract C_0. Fig. 2(c) shows the C for the resistor that produced the best series-resistor calibration (see section IV), 91.28 Ω. This 91.28 Ω resistor is 50 μm long and is not as good of a choice for finding the C as some of the other resistors that we measured. Fig. 2(d) shows the C for one of the best resistors for extracting the C_0 with an R_{DC} value of 155.88 Ω. Here, C is flat, with little variability within the frequency window, and the transmission and reflection values are the same. Fig. 2(e) shows the C for a resistor with an R_{DC} value of 183.52 Ω. This resistor has an R_{DC} value close to the best resistor, but it is long (100 μm) compared to the guided wavelength and C decreases significantly at higher frequencies, which we speculate may be attributed to parasitic inductance or the onset of distributed effects. Fig. 2(f) shows the C for the resistor with the highest R_{DC} value that is also 28 μm or shorter and thus has a non-zero frequency window according to our conditions. This resistor had an R_{DC} value of 649.28 Ω and despite its relatively high R_{DC}, the C_0 extracted from within our frequency bounds agrees well with the other optimal resistors. The key result is that our frequency bounds reject frequencies where the C begins to depart from a constant value due to ill-conditioned mTRL measurements at low frequencies, parasitic inductance, parasitic capacitance, or distributed effects at high frequencies.

Fig. 3 shows C_0 vs. R_{DC} for the resistors we measured. Fig. 3(a) are the data where "bad" resistors were excluded by our phase criterion. As an additional check, it proved informative to manually select frequency bounds for capacitance extraction for all the resistors measured, including the ones longer than 28 μm. We did this by selecting and averaging approximately one decade of frequency of the C vs. f data with the lowest variation. Fig. 3(b) shows all the extracted capacitance values with manual frequency bounds. The values are split into those extracted from transmissive and reflective S-parameters. The optimal resistors are ones that have accurate C_0 values around the consensus value of ~111 pF/m, low uncertainty, and where the transmission and reflection data points are approximately the same.

It is interesting to note that C_0 extracted from transmissive (S_{12} and S_{21}) S-parameters is consistently slightly higher than the values extracted from reflective S-parameters (S_{11} and S_{22}). We speculate that this difference could be due to systematic errors in the port match error term, or probe contact resistance errors on one of the on-wafer probes. Regardless of this difference, these values are typically equal for "good" resistors, but tend to differ for especially long resistors or those with a low R_{DC} value (typically < 40 Ω). For the long resistors, the approximation that the load resistance Z_L is equal to R_{DC} [16], [19] may not be valid, due to a non-negligible parasitic inductance. For the small resistors, these resistors tend to be shorter and wider and thus have a small aspect ratio that could result in a parasitic capacitance due to the CPW center conductors being very close together. For small R_{DC} resistors, this effect could also be due to the S-parameters showing high transmission. If the uncertainty on the reflective and transmissive S-parameters is the same, the uncertainty is a much larger fraction of the magnitude of the reflective S-parameters that are close to 0.

After estimating C across all measurements and frequencies, we found C_0 by averaging C across the selected frequency window. The error bars presented in Fig. 3 and Table 1 are the

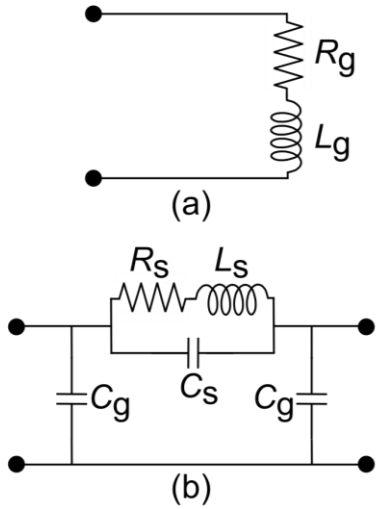

Fig. 5. (a) Circuit diagram for the lumped-element model of the short standard. (b) Circuit diagram for the lumped-element model of the series-resistor standard.

standard deviation of the C values that we averaged to compute C_0. For the "bad" resistors, there is a large spread in C even within the frequency window and the standard deviation of these values is a valid representation of the uncertainty in C_0. For the optimal resistors, we can compute a more rigorous uncertainty by error propagation, which we found was less than the standard deviation of the C values. We show this calculation explicitly for the 155.88 Ω and 54.68 Ω resistors in Appendix A. Overall, we found that the best resistors in our data set for measuring C_0 have R_{DC} values near 150 Ω, are 5 µm, 10 µm, or 20 µm-long, and have aspect ratios (length/width) around 4 or 5. The exact parameters for these resistors are found in Table 1, where we averaged both the transmissive and reflective values of C to get a single number for C_0 to use in our calculations and algorithms.

In applying (2) and (3), it is important that the measured R_{DC} value is accurate and precise. A small error in the R_{DC} measurement can result in an incorrect C_0 value, as the $1/R_{DC}$ in (2) and (3) gives an overall scale factor to the C data. As the resistance of the thru is also used to calculate R_{DC}, this measurement must be accurate and precise as well. Smaller R_{DC} values are more affected by measurement errors as the fractional uncertainty is greater. To demonstrate this, we artificially changed R_{DC}, keeping everything else the same, and computed C_0 in the same way as in Fig. 3(b). These data are shown in Fig. 4(a and b) for artificially adjusting R_{DC} by -0.5 Ω and +0.5 Ω, respectively. Subtracting 0.5 Ω has a larger overall effect, because the already small denominator shifts closer to zero. In both cases, we find the adjustment causes incorrect C_0 values for smaller R_{DC} resistors, especially below 100 Ω. Accurate and precise R_{DC} values are important; however, choosing a series resistor with an R_{DC} value around 150 Ω will make the data more robust against errors in the R_{DC} measurements that are caused by small variations in probe placement and probe contact repeatability.

IV. Series-Resistor Calibration

A. Theory

In some on-wafer measurement scenarios, mTRL calibrations are either not available or not ideal. These scenarios include low-frequency calibrations where it is impractical to fabricate transmission lines that are long enough for mTRL. They also include measurements with fixed probe-to-probe distances (*e.g.*, measurements with a probe card, and cryogenics), where it is not possible to measure lines with different lengths. In these scenarios, it is advantageous to employ lumped-element calibration standards, which includes the series-resistor calibration. In this section, we explore the question of which series-resistor design is best for the series-resistor calibration.

We evaluated each of the 48 resistors for their utility in the series-resistor calibration [15] and compared the quality of the calibration to mTRL [18]. The series-resistor calibration requires raw S-parameter measurements of at least three standards—a thru, a reflect, and a series resistor—and a corresponding model for each. For the thru, we used an ideal model (perfect transmission with no reflection). For the short-circuit reflect and the series resistor, we used the models shown in Figs. 5(a) and 5(b), respectively.

To estimate the values of the parameters in the models for the short-circuit reflect and the series resistor, we corrected the raw S-parameter measurements of the short-circuit reflect and the series resistor with the error boxes from a mTRL calibration, then fit the models to the error-corrected, frequency-dependent S-parameters. The error boxes obtained from mTRL were transformed to a reference impedance of 50 Ω, where C_0 was estimated with the procedure outlined in Section III, and we always employed the same resistor to both estimate C_0 and serve as the resistor in the series-resistor calibration.

After correcting the S-parameters of the series resistor, we observed ripples in the impedance of the series resistor. We suspect that these ripples (Fig. 6) are due to crosstalk between the on-wafer probes and moding, which could be further decreased with crosstalk correction [24] and or the addition of dielectric spacer [13].

Once the parameters of the models were estimated for each series resistor, we employed the models as standard definitions in the series-resistor algorithm [15] and computed error boxes for each of the 48 series resistors.

To assess the accuracy of the error boxes from the series-resistor calibration for each series resistor, we compared these error boxes to the error boxes from mTRL by computing the maximum error between the calibrations.

B. Step-by-Step Procedure for Series-Resistor Calibration

1) Measure the switch terms and uncorrected S-parameters of the mTRL standards.
2) Measure R_{DC} and S-parameters for all series-resistor
3) constant $\gamma(\omega)$ and error boxes corrected to the unknown characteristic impedance Z_0.
4) Correct the series resistors' S-parameters with the mTRL error boxes.
5) Use (2) and (3) to estimate $C(\omega)$.
6) Apply frequency bounds and average the real part of $C(\omega)$ within the bounds to get C_0.
7) Use C_0 to get the characteristic impedance from $Z_0(\omega) = \gamma/i\omega C_0$.
8) Use Z_0 to impedance transform the mTRL error boxes to 50 Ω.
9) Use the mTRL error boxes corrected to 50 Ω to correct the raw S-parameters of the short and the series resistors.
10) For each series resistor, fit the frequency-dependent S-parameters of the short and series resistor, corrected to 50 Ω, to the circuit models shown in Fig. 5. Scattering parameters data and associated fits for some representative series resistors are shown in Fig. 6.
11) Generate the series-resistor calibration error boxes for each series resistor [15], [16], taking the raw S-parameters of the short, series resistor, and thru as the measurement data and the fits of the short, series resistor, and an ideal model for the thru as standard definitions.
12) Compare the series-resistor calibration error boxes for each series resistor to the mTRL error boxes corrected to 50 Ω [18].

C. Results for Series-Resistor Calibration

Fig. 7 shows the S-parameters of a transmission line of length 1.010 mm corrected to 50 Ω with mTRL and with series-resistor calibrations using different resistors. We found that very low and very high R_{DC} did not produce as good calibrations as resistors with more intermediate values between 50 Ω to 200 Ω. Fig. 8 shows the calibration comparison [18] of series-resistor calibrations with different resistors to mTRL as well as mTRL repeatability as a function of frequency. We found that series-resistor calibrations with the best resistors tended to perform almost as well as the mTRL repeatability, comparable to the instrument drift in our measurements. This result is also highlighted in Fig. 9(a), which shows the average calibration comparison value for each of the 48 resistors as well as mTRL repeatability. Fig. 9(b) shows the same data, but with the average separated into a low-frequency (<10 GHz) and high-frequency (≥10 GHz) average. We observe the same trends no matter how we average over frequency. From this data, we conclude that resistors with R_{DC} near 100 Ω produce the best series-resistor calibrations. We also note that all these resistors are 50 μm long or shorter. Table 2 has the exact parameters for the best resistors in our data set for the series-resistor calibration.

V. Finite-Element Simulations

We performed finite-element simulations of our series-resistor devices to validate our measurements. The structures we simulated were the same sizes and geometries as our actual devices. We used the conductivity we experimentally measured for the PdAu and Au in the simulations. The simulation volume included the 500 μm thick quartz substrate and a symmetric 500 μm layer of air above the CPW structures. We used a radiative boundary conditions and wave port excitations with a single CPW mode normalized to 50 Ω. We used a full 3D simulation with the CPW leads included. A picture of the simulation geometry is shown in Fig. 10. The reference planes were at the edge of the resistive element, as in our measurements. We used 100 frequency points on a linear grid from 100 MHz to 110 GHz. The maximum mesh element length was 1.5 μm and we used broadband adaptive solving over the full frequency range with a maximum Delta S of 0.001 and a maximum of 35 adaptive passes. We selected a first order direct solver and simulated the S-parameters of all 48 of our series resistor geometries. Overall, we found very good agreement between our simulations and experimental data. Fig. 11(a and b) show the S-parameters data and simulation results for the 54.68 Ω resistor and Fig. 11(c) shows the maximum difference (S-parameter error) vs. frequency between the data and simulations for this resistor. Fig. 11(d) plots the maximum S-parameter error averaged over the frequency range for all the resistors studied. From this figure, we conclude that the simulations and experimental data agree very well. While the finite-element simulations successfully replicated the corrected S-parameters, we cannot assume this level of accuracy without high quality measurements. In Appendix B we also show the circuit model parameters extracted from the simulations match those from the experimental data.

We note that in addition to circuit parameters in Fig. 5, one could include other additional circuit parameters to capture the in the corrected S-parameters. However, the agreement between the model and the finite-element simulations support only including the circuit parameters in Fig. 5 for the conditions in this experiment.

VI. Discussion

Despite sampling a large parameter space, this work was not exhaustive. We fabricated and measured a variety of series resistors and evaluated their performance for extracting capacitance and performing the series-resistor calibration. Still, there are many other possible resistors with different geometries that were not included, and we evaluated only one resistor material and thickness.

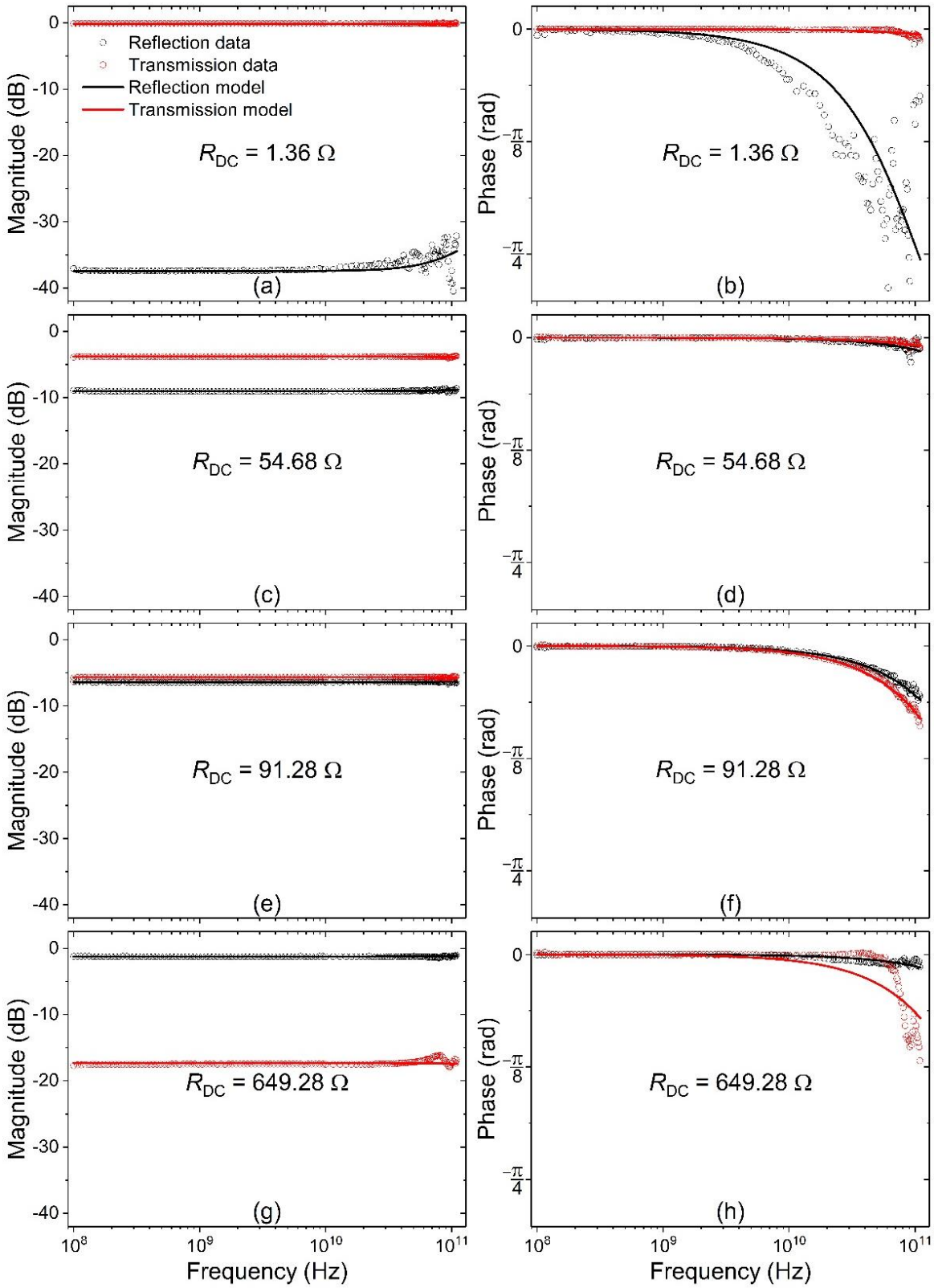

Fig. 6. S-parameter data (magnitude and phase) vs. frequency, and model fits for representative series resistors with R_{DC} of (a) and (b) 1.36 Ω, (c) and (d) 54.68 Ω, (e) and (f) 91.28 Ω, and (g) and (h) 649.28 Ω.

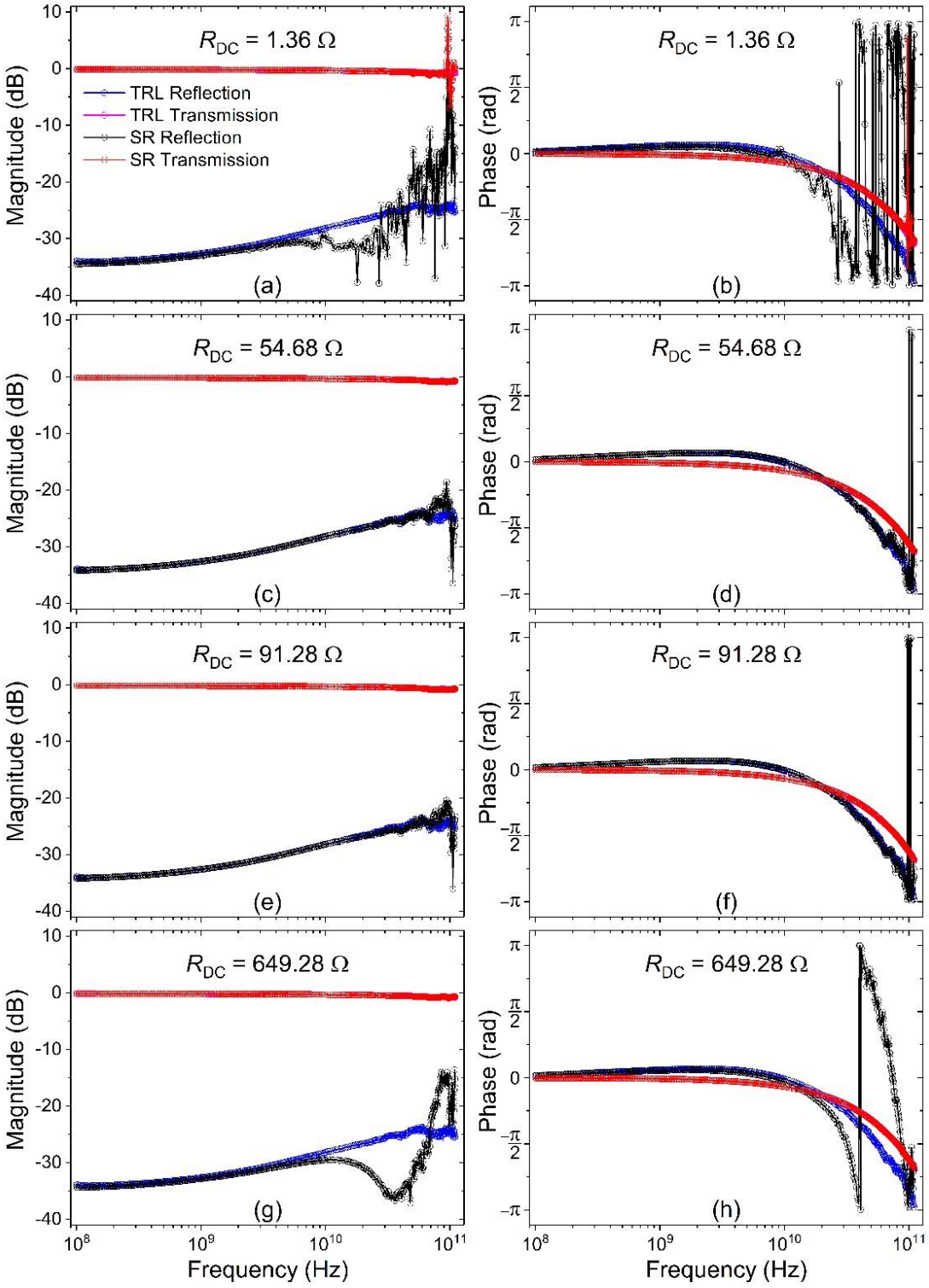

Fig. 7. S-parameter data (magnitude and phase) vs. frequency for a transmission line of length 1.010 mm corrected with mTRL and the series-resistor (SR) calibration with series resistors having dc resistance values R_{DC} of 1.36 Ω (a) and (b), 54.68 Ω (c) and (d), 91.28 Ω (e) and (f), and 649.28 Ω (g) and (h). The lines are guides for the eye.

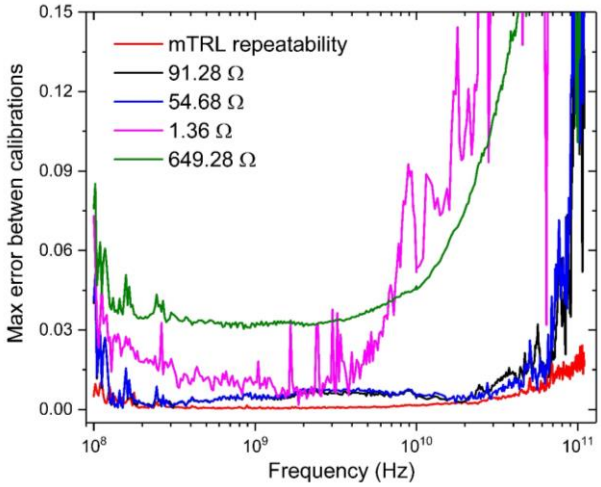

Fig. 8. Maximum error between series-resistor calibrations and a mTRL calibration vs. frequency for a representative set of series resistors, as well as mTRL repeatability vs. frequency.

Decreasing the thickness of the PdAu will increase the overall resistance, and that will yield higher resistances for the shorter length resistors which meet the 'less than 28-µm criterion'. These would be interesting to investigate to see if they yield similar trends and results to those presented in this work. A potential issue with resistors that are thinner than 12.5 nm is variability in the deposition thickness. It can be harder to control deposition thickness as it gets smaller as there is some uncertainty as the evaporator shutter opens and the quartz crystal monitor begins to register a deposition rate and total thickness. The rate of PdAu deposition is also important as this can affect grain size and the resistivity of the films deposited. For consistency, it is probably better to aim for thicker resistor layers, so that small variations in deposition thickness still result in consistent and useful resistors across a typical wafer diameter.

A different material with higher intrinsic resistivity could potentially be beneficial to make resistors with higher resistance, but still thicker and shorter in length. Studies along these lines could help to separate the optimal aspect ratio of the resistor—which controls the balance between the parasitic inductance of the resistor and the parasitic capacitance between the leads connecting to the resistor—and the optimal dc resistance of the resistor. However, PdAu is known to have two properties that make it advantageous as an on-wafer resistor. First, it consists of only noble metals, so the resistance does not drift due to surface effects like oxidation. Second, it has a low temperature coefficient of resistance, making its R_{DC} nearly constant as a function of temperature [25]–[27]. This makes PdAu resistors especially appealing for calibrations and experiments at low temperatures, where accurate and compact calibrations are valuable. Nevertheless, it would be interesting to compare our current results to future work with a material

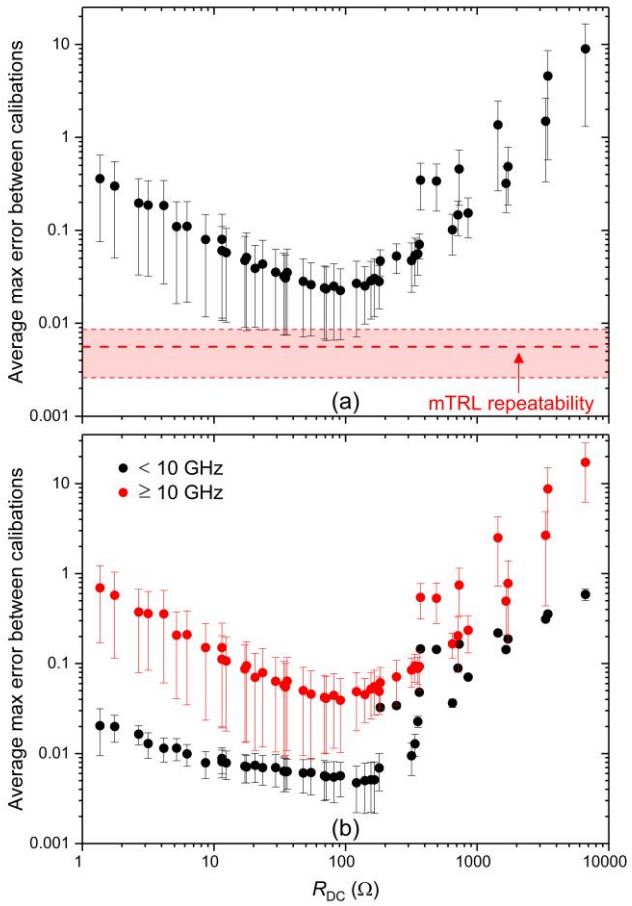

Fig. 9. (a) Average maximum error between mTRL and series-resistor calibrations using series resistors with different R_{DC} values. The maximum error is averaged over the full frequency range of the calibration. The value for mTRL repeatability is indicated as well. The error bars are the average deviation from the median value of the maximum error, and indicate the spread in the data rather than a true uncertainty. The shaded region is the average deviation from the median value of the maximum error for mTRL repeatability. (b) Same as in (a) but with the data separated into averages below 10 GHz and above 10 GHz.

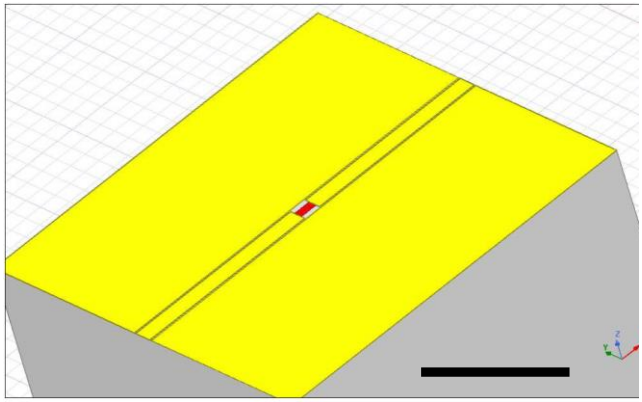

Fig. 10. Schematic of the geometry used in the finite element simulations. The reference planes of the data are at the edges of the resistive element as in the measured data. Scale bar is 200 µm.

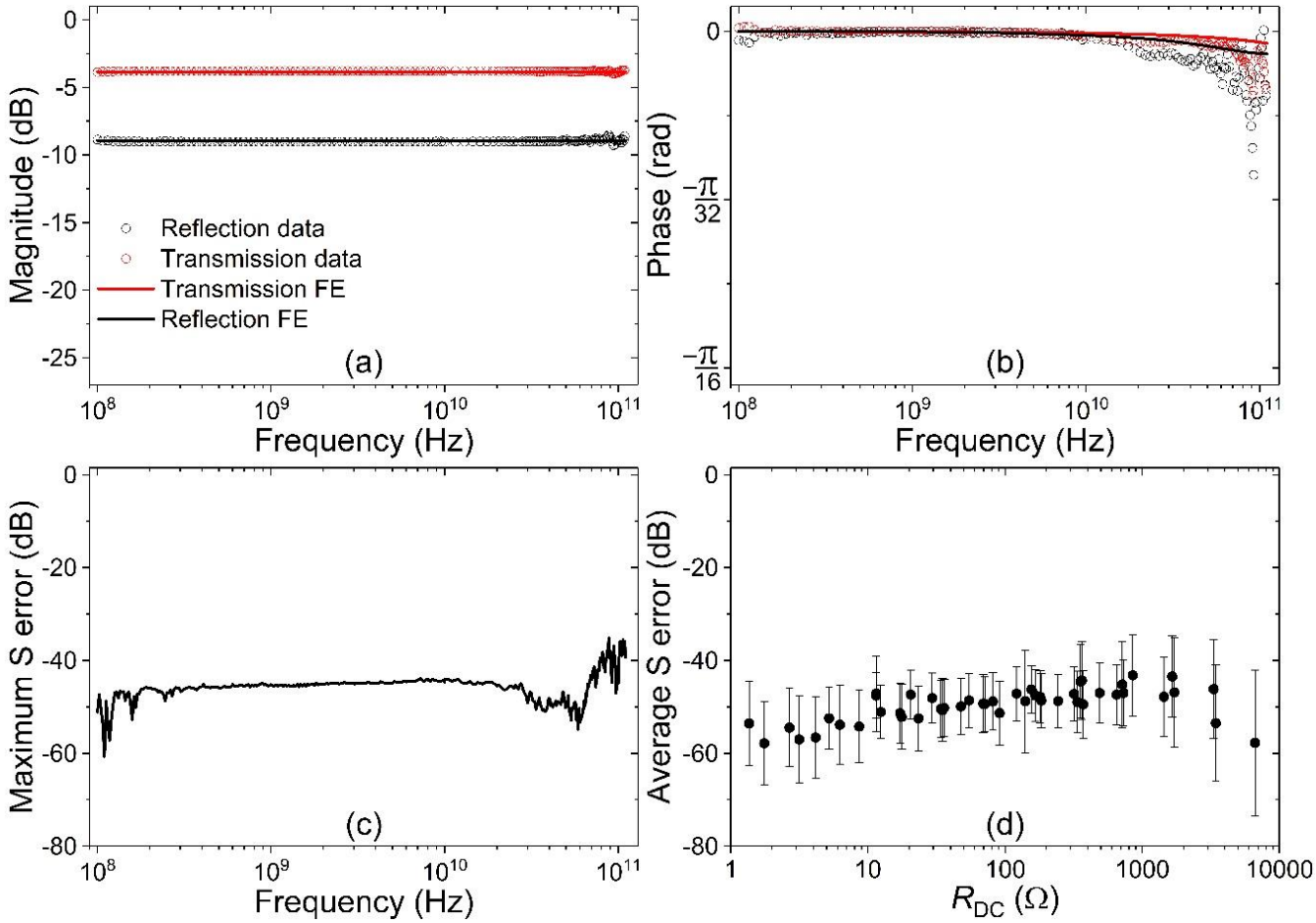

Fig. 11. Finite-element simulation results. Data and finite-element simulation results for the 54.68 Ω resistor showing S-parameter magnitude (a) and phase (b) vs. frequency. (c) S-parameter error vs. frequency between the data and simulations for the 54.68 Ω resistor. (d) Average S-parameter error over all frequencies between the data and simulations for the 48 resistors studied. The error bars are the standard deviation of the S-parameter error vs. frequency.

TABLE II
PARAMETERS FOR THE BEST RESISTORS IN OUR DATA SET FOR USE IN THE SERIES-RESISTOR CALIBRATION

R_{DC} (Ω)	Average max error	Average deviation from the median	Length, x-direction (μm)	Width, y-direction (μm)	Aspect ratio, length/width	*Rs* (Ω)	*Ls* (pH)	*Cs* (fF)	*Cg* (fF)
54.68	0.0260	0.0188	2	1	2	54.84	14.9	4.47	0.51
69.16	0.0240	0.0172	10	5	2	69.34	18.0	2.13	0.81
71.08	0.0234	0.0169	20	10	2	71.25	19.6	1.49	1.19
81.48	0.0250	0.0185	5	2	2.5	81.67	20.6	2.37	0.64
91.28	0.0225	0.0159	50	20	2.5	91.52	24.6	< 0.01	3.14
121.08	0.0268	0.0197	50	15	3.33	121.23	33.6	< 0.01	2.57
140.28	0.0252	0.0154	20	5	4	140.44	31.6	0.55	1.10
TRL repeatability	0.0056	0.0030							

Circuit fit parameters *Rs*, *Ls*, *Cs*, and *Cg* are defined in Fig. 5. The averages are over all frequencies.

with higher resistivity.

For this work, we selected fused silica to use as a lossless substrate. While some of our conclusions about optimal series resistors may not generalize to other substrates, we see no physical or mathematical reason why our conclusions are not extensible to other low-loss substrates. For lossy substrates, one approach to performing calibrations is to start with a calibration on a lossless substrate that has the same geometry CPWs and then to assume that the resistance per unit length and inductance per unit length on the lossy substrate are the same [28]. This approach provides a mechanism to perform accurate calibrations on lossy substrates.

VII. CONCLUSION

In summary, we fabricated and measured a variety of on-

wafer series-resistor devices to understand which resistor is optimal for finding C_0 in a mTRL calibration and which resistor is optimal to use in an on-wafer series-resistor calibration. We evaluated 48 series resistors that covered a wide range of lengths, widths, and resistances. We found that resistors with R_{DC} values near 150 Ω and 20 µm long or shorter were optimal for measuring C_0. We also found that resistors with R_{DC} values near 100 Ω were optimal for use in the series-resistor calibration. We note that these resistances are higher than the 50 Ω resistance typically employed for resistors in an SOLT calibration. We expect the identification of optimal series-resistor values will improve the accuracy of on-wafer calibrations, offering improved insights into the behavior of novel devices and materials for high-frequency electronics and wireless communications applications.

Prior to this work it was unclear what dc resistance value of a series resistor produced the most accurate and precise on-wafer calibrations with the lowest possible uncertainty. Based on empirical evidence and the detailed analysis presented here, we can recommend series resistors with a dc resistance between 100 Ω and 150 Ω and aspect ratio in the range of 2 to 4 for optimal capacitance extraction and optimal on-wafer series-resistor calibrations.

Acknowledgement

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Appendix A
Treatment of Uncertainty

Equations (2) and (3) are used to estimate C_0, a quantity that is necessary for correcting raw S-parameter measurements to a reference impedance of 50 Ω. The exact value of C_0 has a strong influence on the accuracy of both the mTRL and series-resistor calibrations. It is thus useful to rigorously analyze the uncertainty on the value of C_0 we estimated in Section III.

We calculated C_0 from the series resistor's reflective and transmissive S-parameters separately as the equations are slightly different (see (2) and (3)). We will treat the reflective and transmissive uncertainties separately as well. Let $C(\omega)$ have some uncertainty, σ_{C_i} for each value of ω_i within our frequency window criteria defined in Section III. To find C_0, we average over the range of $C(\omega_i)$. The variance on C_0 is given by,

$$\sigma^2_{C_{o,Refl}} = \left(\frac{1}{2n}\right)^2 \left(\sum_{i=1}^{n} \sigma^2_{C_{i,S_{11}}} + \sigma^2_{C_{i,S_{22}}}\right) \quad (A.1)$$

$$\sigma^2_{C_{o,Trans}} = \left(\frac{1}{2n}\right)^2 \left(\sum_{i=1}^{n} \sigma^2_{C_{i,S_{12}}} + \sigma^2_{C_{i,S_{21}}}\right) \quad (A.2)$$

where $i = 1, 2, \ldots, n$ indexes the data points within the frequency window from ω_1 = the low frequency limit to ω_n = the high frequency limit. For the 155.88 Ω resistor, $\omega_1 = 2\pi \times$ 645 MHz and $\omega_n = 2\pi \times$ 5.37 GHz with $n = 93$. For the 54.68 Ω resistor, $\omega_1 = 2\pi \times 645$ MHz and $\omega_n = 2\pi \times$ 14.5 GHz with $n = 129$.

From (2) and (3) and the propagation of uncertainty,

$$\sigma^2_{C_{i,S_{jk}}} = \left|\frac{\partial C_{S_{jk}}}{\partial \gamma}\right|^2_{\omega_i} \sigma^2_{\gamma_i} + \left|\frac{\partial C_{S_{jk}}}{\partial \omega}\right|^2_{\omega_i} \sigma^2_{\omega_i} + \left|\frac{\partial C_{S_{jk}}}{\partial R_{DC}}\right|^2_{\omega_i} \sigma^2_{R_{DC}} + \left|\frac{\partial C_{S_{jk}}}{\partial S_{jk}}\right|^2_{\omega_i} \sigma^2_{S_{jk,i}} \quad (A.3)$$

where the ω_i on the partial derivates indicates the derivative is evaluated at ω_i.

The partial derivatives with respect to the propagation constant are

$$\frac{\partial C_{S_{11,22}}}{\partial \gamma} = \frac{2}{\omega R_{DC}} \frac{S_{11,22}}{1 - S_{11,22}} \quad (A.4)$$

$$\frac{\partial C_{S_{12,21}}}{\partial \gamma} = \frac{2}{\omega R_{DC}} \frac{1 - S_{12,21}}{S_{12,21}}. \quad (A.5)$$

We used StatistiCAL [29] to calculate the error boxes and effective dielectric constant (ε_{Eff}) in the mTRL algorithm [6]. StatistiCAL exported these quantities along with a standard error associated with each quantity at each frequency point. We calculated the propagation constant from the effective dielectric constant as

$$\gamma = \frac{\sqrt{-\varepsilon_{Eff}}\,\omega}{c} \quad (A.6)$$

where ω is the angular frequency and c is the speed of light. The uncertainty in the propagation constant is then

$$\sigma^2_{\gamma_i} = \left|\frac{\partial \gamma}{\partial \varepsilon_{Eff}}\right|^2_{\omega_i} \sigma^2_{\varepsilon_{Eff,i}} + \left|\frac{\partial \gamma}{\partial \omega}\right|^2_{\omega_i} \sigma^2_{\omega_i} \quad (A.7)$$

where

$$\frac{\partial \gamma}{\partial \varepsilon_{Eff}} = -\frac{1}{2} \frac{\omega}{\sqrt{-\varepsilon_{Eff}}\, c} \quad (A.8)$$

$$\frac{\partial \gamma}{\partial \omega} = \frac{\sqrt{-\varepsilon_{Eff}}}{c}. \quad (A.9)$$

$\sigma_{\varepsilon_{Eff}}$comes directly as an output from StatistiCAL. The frequency accuracy of our VNA was $10^{-6}\, f$ Hz, where f is the frequency, thus

$$\sigma_\omega = 2\pi * 10^{-6} * f \text{ rad/s}. \quad (A.10)$$

The derivatives in (A.3) with respect to ω are

TABLE III
RELATIVE UNCERTAINTY CONTRIBUTIONS

Component of (A.3)	Average reflective uncertainty contribution over frequency window (ω_i) for R_{DC} = 155.88 Ω, (pF/m)	Average transmissive uncertainty contribution over frequency window (ω_i) for R_{DC} = 155.88 Ω, (pF/m)	Average reflective uncertainty contribution over frequency window (ω_i) for R_{DC} = 54.68 Ω, (pF/m)	Average transmissive uncertainty contribution over frequency window (ω_i) for R_{DC} = 54.68 Ω, (pF/m)
$\sqrt{\left\lvert\frac{\partial C_{S_{Refl,Trans}}}{\partial \gamma}\right\rvert_{\omega_i}^2 \sigma_{\gamma_i}^2}$	0.05	0.05	0.13	0.13
$\sqrt{\left\lvert\frac{\partial C_{S_{Refl,Trans}}}{\partial \omega}\right\rvert_{\omega_i}^2 \sigma_{\omega_i}^2}$	<< 0.01	<< 0.01	<< 0.01	<<0.01
$\sqrt{\left\lvert\frac{\partial C_{S_{Refl,Trans}}}{\partial R_{\mathrm{DC}}}\right\rvert_{\omega_i}^2 \sigma_{R_{\mathrm{DC}}}^2}$	0.05	0.04	0.36	0.36
$\sqrt{\left\lvert\frac{\partial C_{S_{Refl,Trans}}}{\partial S_{jk}}\right\rvert_{\omega_i}^2 \sigma_{S_{Refl,Trans,i}}^2}$	0.30	0.18	0.77	0.71

TABLE IV
UNCERTAINTIES IN C_0 USING PROPAGATION OF UNCERTAINTY

Quantity	Value (pF/m)	Uncertainty (pF/m)
$C_{0,Tot,R_{\mathrm{DC}}=155.88\,\Omega}$	110.88	0.01
$C_{0,Tot,R_{\mathrm{DC}}=54.68\,\Omega}$	110.84	0.04

$$\frac{\partial C_{S_{11,22}}}{\partial \omega} = \frac{-2\gamma}{\omega^2 R_{\mathrm{DC}}}\frac{S_{11,22}}{1-S_{11,22}} \quad \text{(A.11)}$$

$$\frac{\partial C_{S_{12,21}}}{\partial \omega} = \frac{-2\gamma}{\omega^2 R_{\mathrm{DC}}}\frac{1-S_{12,21}}{S_{12,21}}. \quad \text{(A.12)}$$

The derivatives in (A.3) with respect to R_{DC} are given by

$$\frac{\partial C_{S_{11,22}}}{\partial R_{\mathrm{DC}}} = \frac{-2\gamma}{\omega R_{\mathrm{DC}}^2}\frac{S_{11,22}}{1-S_{11,22}} \quad \text{(A.13)}$$

$$\frac{\partial C_{S_{12,21}}}{\partial R_{\mathrm{DC}}} = \frac{-2\gamma}{\omega R_{\mathrm{DC}}^2}\frac{1-S_{12,21}}{S_{12,21}}. \quad \text{(A.14)}$$

The uncertainty in R_{DC} comes from the digital multimeter (DMM) used to measure the resistance and from the on-wafer probe contact landing repeatability. The data presented in this manuscript are from the first instance of landing probes on pristine Au CPWs. The intrinsic uncertainty of the DMM is 0.04 Ω and we estimate the probe contact uncertainty to be 0.02 Ω. R_{DC} of the individual resistors is found from taking the total resistance of a series-resistor device integrated into a CPW and subtracting the resistance of the thru, equivalent to the resistance of the CPW leads up to the resistive element. The variance on each R_{DC} value is thus

$$\sigma_{R_{\mathrm{DC}}}^2 = \sigma_{DMM,Thru}^2 + \sigma_{DMM,SR}^2 + \sigma_{Probes,Thru}^2 + \sigma_{Probes,SR}^2 = 0.004\ \Omega^2 \quad \text{(A.15)}$$

and

$$\sigma_{R_{\mathrm{DC}}} = 0.06\ \Omega. \quad \text{(A.16)}$$

The derivatives in (A.3) with respect to the S-parameters are

$$\frac{\partial C_{S_{11,22}}}{\partial S_{11,22}} = \frac{2}{\omega R_{\mathrm{DC}}}\left[\frac{1}{1-S_{11,22}} + \frac{S_{11,22}}{\left(1-S_{11,22}\right)^2}\right] \quad \text{(A.17)}$$

$$\frac{\partial C_{S_{12,21}}}{\partial S_{12,21}} = \frac{-2\gamma}{\omega R_{\mathrm{DC}}}\frac{1}{S_{12,21}^2}. \quad \text{(A.18)}$$

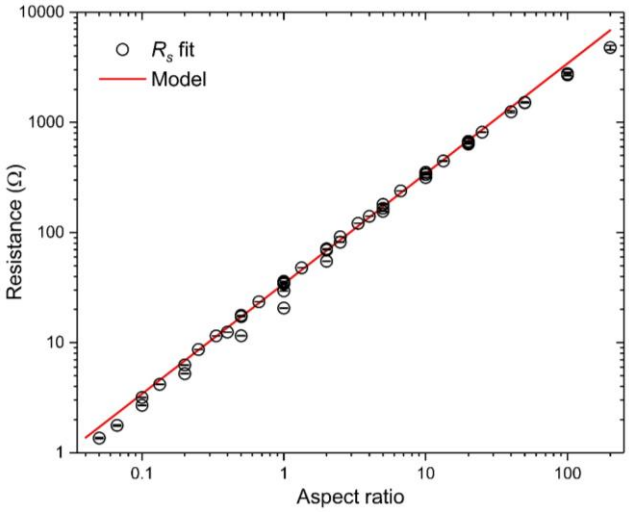

Fig. 12. Resistance vs. aspect ratio for the extracted circuit model fit parameters R_s and for the model is (B.1). Aspect ratio is resistor length/width. The error bars represent a 95 % confidence interval on the fit.

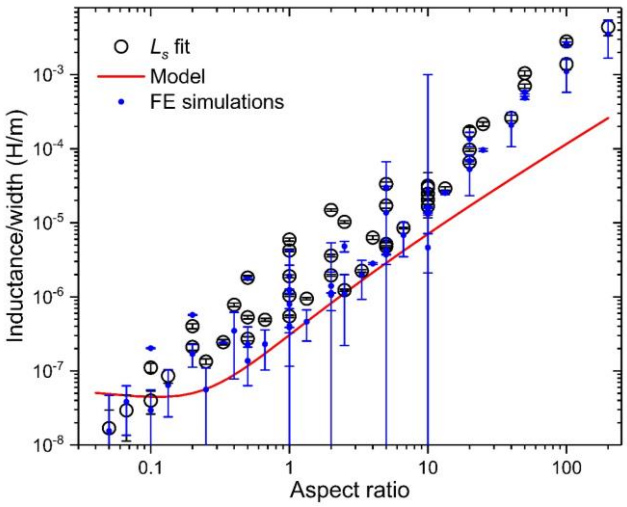

Fig. 13. Inductance/width vs. aspect ratio for the extracted circuit model fit parameters L_s, circuit model fits to the finite-element (FE) simulations, and for the model in (B.2). Aspect ratio is resistor length/width. The error bars represent a 95 % confidence interval on the fit.

Like ε_{Eff}, we used StatistiCAL to compute the calibration error boxes and the uncertainty in the error box components. We performed a sensitivity analysis using the error box uncertainties to compute the uncertainty in the S-parameters for the 155.88 Ω and 54.68 Ω resistors. We varied the error box components one standard deviation higher and lower than their nominal values and calculate the corresponding variation in the corrected S-parameters. We then took the difference between the nominal S-parameters and the S-parameters computed with the shifted error boxes as the uncertainty in the S-parameters as a function of frequency.

Now we can compare the relative contributions of the terms in (A.3) to the uncertainty in C_0 and compute the total uncertainty in C_0. The relative contributions are found in Table III and the total uncertainty in C_0 is found in Table IV.

We found that the uncertainty in the S-parameters was the dominant contribution to the uncertainty in (A.3). Now we can average together all the C values from all four S-parameters within the frequency window to get a single number to use for C_0 in our algorithms and calculations.

$$C_{0,Tot} = \left(\frac{1}{4n}\right)\left(\sum_{i=1}^{n} C_{i,S_{11}} + C_{i,S_{12}} + C_{i,S_{21}} + C_{i,S_{22}}\right) \quad \text{(A.19)}$$

with

$$\sigma^2_{C_{0,Tot}} = \left(\frac{1}{4n}\right)^2 \left(\sum_{i=1}^{n} \sigma^2_{C_{i,S_{11}}} + \sigma^2_{C_{i,S_{12}}} + \sigma^2_{C_{i,S_{21}}} + \sigma^2_{C_{i,S_{22}}}\right). \quad \text{(A.20)}$$

The $C_{0,Tot}$ values were the same as the ones reported in Table 1.

We found that the uncertainties calculated using propagation of errors are smaller than the standard deviations of the C values averaged and reported in Table 1. While an optimal resistor design minimizes the structure in C, in cases where a sub-optimal resistor is chosen and there is substantial structure in C within the frequency bounds (for example, as in Fig. 2a), the standard deviation of the C values would serve as a better estimate of the uncertainty in C_0.

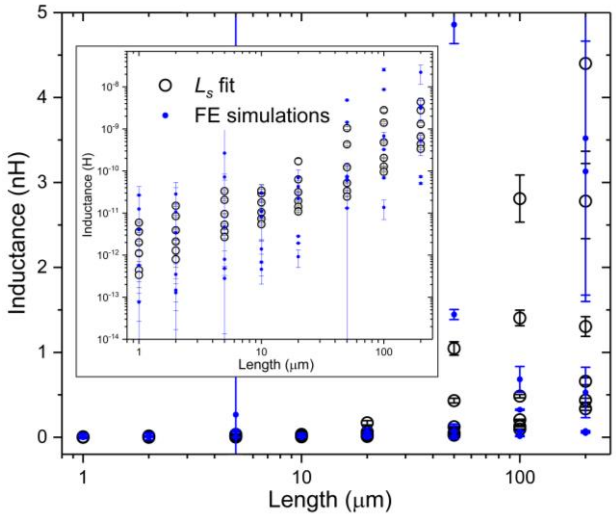

Fig. 14. Inductance vs. length for the extracted circuit model fit parameters L_s and the finite-element simulations. The error bars represent a 95 % confidence interval on the fit. The inset shows the same data on a logarithmic scale.

Appendix B
Lumped-Element Circuit Model Fit Parameters

We fit the series-resistor S-parameters to the circuit model in Fig. 5 as part of Step 10 in the procedure in outlined Section IV-B. We extracted the lumped-element circuit parameters from the fit for each of the 48 series resistors and examined them further. We expect the lumped series resistance R_s to follow the well-known geometric relation

$$R = \frac{\rho l}{A} \quad \text{(B.1)}$$

where ρ is the resistivity of the PdAu in Ω·m, l is the length of the resistor in m, and A is the cross-sectional area in m^2. We find that the R_s extracted from our data agree well with the model in (B.1) for $\rho = 3.75*10^{-7}$ Ω·m, which we show in Fig. 12.

We also extract the series inductance L_s from our data and from our finite-element simulations. Steinberg *et al*. [30] provide an analytical model for the microwave inductance of thin metal strips. Since, in our resistors, the width w is much greater than the thickness t, their model reduces to

$$L \approx 0.2 * 10^{-6} * l * \left[ln\left(\frac{2l}{w}\right) + 0.5 + \frac{w}{3l}\right] \quad \text{(B.2)}$$

where the inductance L is in H, l is the length in m, and w is the width in m. If we divide (B.2) by the width w, all the dimensions enter in terms of the aspect ratio (l/w) of the resistor. In Fig. 13, we show the extracted L_s divided by the width of the resistors vs. their aspect ratio. We find that the model in (B.2) is reasonably close to our data, but slightly underestimates the inductance. We believe this deviation arises because to the length scales in our resistors are significantly smaller than the length scales examined in [30], as well as the large step edge at the transition between the Au CPW center conductor and the PdAu resistor in our devices which was not considered in [30]. The finite-element simulations match our data well, and the L_s extracted from the simulations also agree with those from the measured data.

Fig. 14 plots the extracted L_s vs. the length of our resistors. Here, we clearly see that when the resistor gets too long ($\gtrsim$ 30 µm), the total parasitic inductance can become significant. This length cutoff agrees well with our phase condition (11) that excludes resistors longer than 28 µm.

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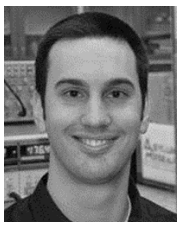

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