Epitaxial Graphene p-n Junctions

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***Abstract*—We report the fabrication and measurement of top gated epitaxial graphene p-n junctions where exfoliated hexgonal boron nitride (hBN) is used as the gate dielectric. The four terminal longitudinal resistance across a single junction is well quantized at $R_{\mathrm{K-90}}$ ($= 25812.807\ \Omega$) with a relative uncertainty of 10^{-7}. Our work opens the possibility to realize programmable electrical resistance standards using external gating.**

***Index Terms*—Epitaxial graphene, graphene p-n junction, quantum Hall effect, resistance standard.**

I. Introduction

Epitaxial graphene has been identified as an excellent platform for resistance standards based on the quantum Hall effect (QHE) because of the wide plateaus and the large breakdown current [1]. Such resistance standards exclusively operate at the filling factor $\nu = 2$, resulting in the resistance value of $\frac{1}{2}R_{\mathrm{K-90}}$. Nevertheless, realization of resistance standards at other values is an important task in resistance metrology. A traditional approach is to connect multiple Hall bars in parallel or series to create resistance values of $qR_{\mathrm{K-90}}$ where q is a positive rational number, despite technical difficulties [2] - [3].

The linear energy spectrum of graphene and charge neutrality at the Dirac point allow graphene to be doped symmetrically into the p (holes) or n (electrons) regime easily with external gates. Graphene p-n junctions can be fabricated to conveniently scale QHE-based resistance standards [4]. With the unique properties of graphene, p-n junction devices may eliminate some technical difficulties caused by metallic contacts and multiple device interconnections. Here we demonstrate highly accurate resistance quantization at $R_{\mathrm{K-90}}$ in an epitaxial graphene p-n junction, measured with a direct current comparator (DCC) resistance bridges.

II. Sample fabrication

Methods of high quality epitaxial growth of graphene and novel fabrication processes avoiding organic contaminations can be found in [1] and [5]. In short, graphene is grown on the silicon face of SiC substrate at high temperatures and protected by Pd (10 nm) / Au (10 nm). After few steps of contact fabrication, the protective Pd/Au layer in the channel area is finally removed in aqua regia. The sample is then tested to select the desired devices.

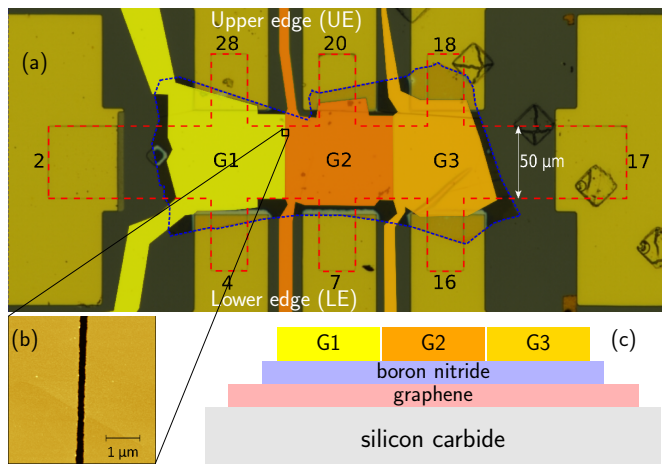

Fig. 1. (a) Optical image of the device with graphene Hall bar and the encapsulating hBN layer outlined by red and blue dashed lines respectively. The numbers label the graphene contacts and G1, G2 and G3 are labeling the top gates with pseudo-colors of yellow, orange and bronze, respectively. (b) Atomic force microscope image of the junction for the black square in (a). (c) Schematics of the cross section of the device.

To fabricate top gates, hexgonal boron nitride (hBN) flakes are exfoliated onto polydimethylsiloxane (PDMS) and their quality and size are carefully examined by a dark field optical microscope and atomic force microscope (AFM). The PDMS carrying the selected hBN flake is then mounted on a glass slide arm for accurate alignment (within a few μm) with the graphene device using our homemade flake transfer stage. The hBN flake approaches the graphene surface slowly until they are fully engaged. The device is then heated to 110 °C to detach hBN from PDMS. A standard electron beam lithography process is used to fabricate metal gates. The width of graphene Hall bar (red dashed line in Fig. 1a) is 50 μm. The thickness of hBN (blue dashed line in Fig. 1a) is 45 nm. The AFM image in Fig. 1b over the black square in Fig. 1a indicates that the gap width between two gates is about 150 nm, small enough to create a single p-n junction.

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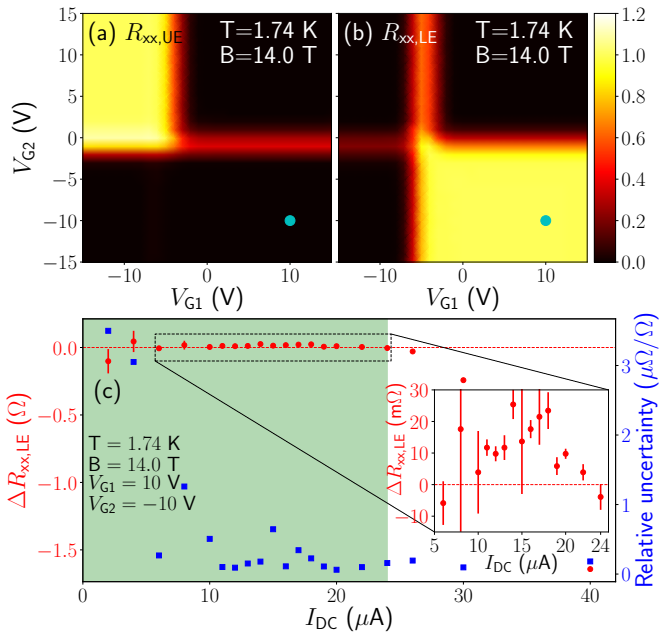

Fig. 2. Color map of the longitudinal resistances $R_{\mathrm{xx,UE}}$ and $R_{\mathrm{xx,LE}}$ vs. gate voltages V_{G1} and V_{G2} measured at the upper edge (UE) (a) and lower edge (LE) (b), in units of $R_{\mathrm{K-90}}$. (c) Current dependence of $\Delta R_{\mathrm{xx,LE}} \equiv R_{\mathrm{xx,LE}} - R_{\mathrm{K-90}}$ for gate voltages at the cyan dots in Fig. 2a and 2b. Data points in the dashed box in (c) is zoomed in and plotted as the inset in (c).

III. Measurement results

We characterized the quality of the hBN dielectric by measuring the leakage current between top gate and graphene, which is less than 1 nA for up to 15 V DC voltage applied between them. The leakage current rapidly increases for voltages beyond 15 V. We thus limit the magnitude of gate voltages to 15 V. For the particular device in Fig. 1a, the gate G3 leaks at substantially lower voltages, therefore we focused on single p-n junction between gates G1 and G2 on which the gate voltages V_{G1} and V_{G2} are applied when graphene is grounded.

Due to the charge transfer between epitaxial graphene and buffer layer in SiC [6], the carrier density in graphene is about (5 to 10) $\times$ 10^{11} cm^{-2} at gate voltage of 15 V, which is nearly one order of magnitude smaller than the carrier density predicted from the capacitance model. Therefore only the $\nu = 2$ plateau can be observed for magnetic fields beyond 6 T when graphene is charge neutral near zero gate voltage. We only present data collected at magnetic field of 14 T and temperature of 1.74 K.

The color map of the longitudinal resistances across the junction between G1 and G2 vs. V_{G1} and V_{G2} at the upper and lower edge are shown in Fig. 2a and 2b respectively. For example, $R_{\mathrm{xx,LE}}$ is the resistance when current is applied between contacts 2 and 17 while voltage is measured between contacts 4 and 7 in Fig. 1a. The four terminal resistance at the upper edge is well quantized at $R_{\mathrm{K-90}}$ (zero) while the lower edge is at zero resistance ($R_{\mathrm{K-90}}$) when the graphene under gate G1 is p-type (n-type) and the graphene under G2 is n-type (p-type). For the other regimes, both resistances are close to zero.

The lower edge resistance is measured with a DCC resistance bridge against a 10 kΩ standard resistor traceable to $R_{\mathrm{K-90}}$ and the results are shown in Fig. 2c. Both the deviation from $R_{\mathrm{K-90}}$ (left axis and red dots) and relative uncertainty (right axis and blue squares) are plotted as a function of the DC current I_{DC}, at gate voltages of $V_{\mathrm{G1}} = -V_{\mathrm{G2}} = 10$ V, indicated by the cyan dots in Fig. 2a and 2b. For the current in the shaded green area, there is no QHE breakdown and the critical current is identified to be 24 μA which is determined by the condition that $|\Delta R_{\mathrm{xx,LE}}|/R_{\mathrm{K-90}}$ is less than the relative uncertainty. Further examinations indicate that the critical current is throttled by the p-type regime which has a significantly lower critical current than the n-type regime. The relative uncertainty is on the order of 10^{-7} for a reasonable measurement time of about 15 minutes.

IV. Conclusion and discussion

We have fabricated and measured epitaxial graphene p-n junctions using hBN as gate dielectrics and demonstrated that it can be accurately quantized at $R_{\mathrm{K-90}}$ with a relative uncertainty on the order of 10^{-7} measured from a DCC resistance bridge. This enables the accurate scaling of QHE based resistance standards for future metrology applications. In fact, we can connect in parallel N samples with $N_i \geq 2$ ($i = 1, \cdots, N$) top gates for each of them after reducing the effect of contact and other resistances by using the double- or triple-series connection techniques [7]. The two terminal resistance for the j-th sample can be $\frac{n_j+1}{2} R_{\mathrm{K-90}}$ if the N_j gates are programmed to create n_j ($< N_j$) junctions. If the voltage probes are placed on one edge of the i-th sample and there are $m_i - 1$ junctions between them, we can obtain the following scaling factors

$$q = \frac{1}{2} \frac{m_i}{n_i + 1} \frac{1}{\sum_{j=1}^{N} \frac{1}{n_j+1}}, \tag{1}$$

where $2 \leq m_i \leq n_i$. This offers numerous possibilities and allows the design of programmable resistance standards with values in the range of $\frac{1}{N}$ to $\frac{1}{2} \max_{1 \leq i \leq N} N_i$ for large N and N_js.

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